Ultra-low Leakage ESD Protection Achieving 10.5 fA Leakage

Corentin Pochet, *Student Member*, IEEE, Haowei Jiang, *Student Member*, IEEE, and Drew A. Hall, *Senior Member, IEEE*

2021 IEEE International Symposium on Circuits and Systems (ISCAS) | 978-1-7281-9201-7/20/$31.00 ©2021 IEEE | DOI: 10.1109/ISCAS51556.2021.9401369

***Abstract*—This paper presents an electrostatic discharge (ESD) protection circuit and reviews best practices to interface a CMOS analog front-end (AFE) with off-chip high impedance (>1 GΩ) and high precision (<1 pA resolution) current sensors. The proposed circuit uses an amplifier at the input/output (I/O) pin to drive the voltage across the ESD protection diodes to a near-zero value, thus enabling sub-pA leakage. Implemented in a 180 nm CMOS process, the proposed circuit reduces the leakage current by 7.5× (to <15 fA) compared to conventional techniques at 25 °C. The proposed circuit's resilience to ESD events was tested using the human-body model (HBM) standard and demonstrated similar ESD protection capabilities when compared to standard ESD protection circuits and improved protection over other low-leakage techniques. This technique achieves sub-pA leakage across the commercial temperature range (0 – 85 °C) while consuming just 15 µW and 0.002 mm².**

***Keywords*—Current sensing, ESD, ultra-low leakage**

I. Introduction

Specialized applications like electrometers and high-precision current front-ends require low leakage for high input impedance (> 1 GΩ) or to measure sub-pA currents [1]–[4]. Designing the analog front-end (AFE) is challenging in and of itself, but the best designer's effort can be ruined if proper low leakage techniques are not implemented when interfacing the AFE with the off-chip sensor or test equipment. There are several sources of leakage that jeopardize the measurement accuracy if preemptive measures are not taken, as illustrated in Fig. 1(a). Using a standard FR4 printed circuit board (PCB) with chip-on-board packaging, the main sources of leakage between the sensor and AFE are: 1) surface contaminants (*e.g.*, flux residue), 2) surface charge (often in the solder mask), 3) substrate leakage, and 4) ESD leakage. In total, these can easily be on the order of the tens of pAs, thereby limiting the input impedance for an electrometer or the detection limit for a current sensing AFE. Worse yet, this leakage is process, voltage, and temperature (PVT) dependent, which makes it difficult to calibrate. As will be described in Section II, several techniques exist to reduce the PCB leakage; however, to eliminate the ESD leakage, the ESD protection circuits are often omitted or replaced with inferior structures that are inherently less robust [2]. This is an issue because ESD protection is critical to ensure chip reliability and these practices greatly increase the risk of failure, reducing the expected yield and lifetime of the chip, ultimately making their use unlikely outside of a controlled laboratory setting.

This paper presents and analyzes an ESD technique for designs requiring fA-level input leakage, which can seamlessly be embedded in a standard pad ring and maintains robust protection against ESD events. The rest of this paper is organized as follows: Section II reviews standard PCB and ESD techniques used to achieve low leakage. In Section III, the design of an ultra-low leakage ESD circuit is presented, analyzed, and design guidelines are given. This is followed by measurement results in Section IV comparing the proposed and standard techniques. Section V summarizes the teachings of this paper.

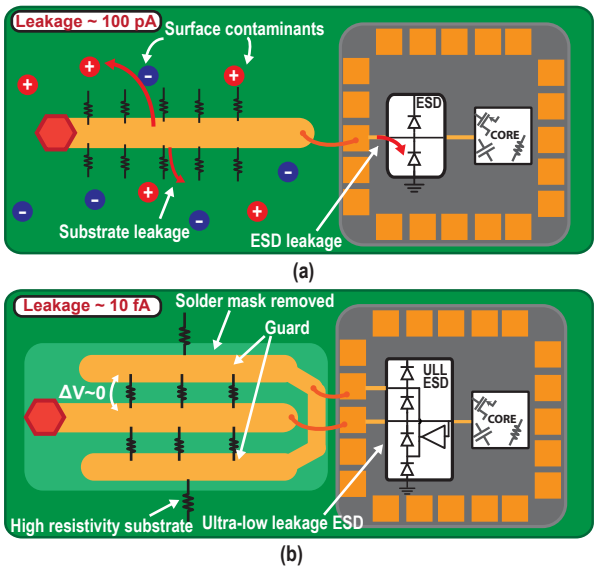

Fig. 1. Overview of leakage sources from: (a) Standard FR4 PCB and ESD; (b) Guarded low-leakage PCB and proposed ESD structure.

II. Best Practice and Techniques For Low Leakage

A. Low-Leakage PCB Design

Great care needs to be taken in the PCB design to achieve sub-pA leakage. The main techniques that must be put in place on- and off-chip to achieve fA-level leakage are illustrated in Fig.1(b). First, each sensitive trace should be surrounded by guard traces that are driven by a replica of the voltage on the signal trace. This reduces the voltage difference between the signal trace and its surroundings to a near-zero value, thereby greatly reducing the trace leakage. In a lab setting, the guard signal is usually provided by the measurement equipment, whereas in a practical deployment, the guard signal needs to be provided by a circuit on-chip and delivered off-chip through a pad. Second, solder mask should be removed from the guard and sensitive traces to avoid surface charge trapping. Alternatively, the trace can be buried on an inner layer and surrounded on the top and bottom by guard traces. Third, the PCB substrate should be chosen to be a high-resistivity material (*e.g.*, Rogers 4003C, which has 1,000× higher resistivity than FR4) to reduce substrate leakage. Lastly, to remove surface contaminants, the PCB should be aggressively scrubbed with isopropanol alcohol, rinsed with deionized water, and baked for 2 hours at 85 °C prior to use. The combination of these techniques reduces the PCB leakage to the low-fA range (<10 fA) such that any remaining leakage current is due to the on-chip ESD protection or core circuits.

This work was supported in part by equipment purchased through a DURIP award from the Office of Naval Research (award no. N00014-18-1-2350). *Corresponding author: Drew A. Hall (drewhall@ucsd.edu).*

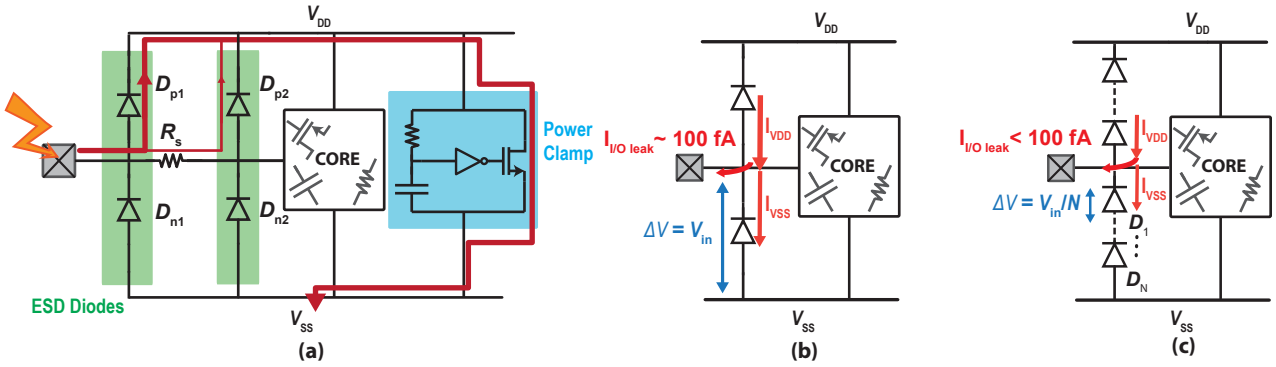

Fig. 2. (a) Standard whole-chip ESD protection during a positive charge ESD event. (b) Standard ESD leakage path. (c) Stacked diode leakage path.

B. Conventional ESD Protection Circuits

ESD is one of the main causes of reliability failure in modern ICs. It is estimated to be responsible for approximately 25% of IC failures [5]. This phenomenon is due to the transfer of electrostatic charge between materials upon contact or through a dielectric (*e.g.*, air) generating a large energy dissipation event that triggers gate oxide breakdown or melting of interconnects. Protection against such ESD events is accomplished through the on-chip circuits illustrated in Fig. 2(a). It consists of two stages of diodes and power-rail clamps [6]. During a positive charge ESD event, the voltage at the I/O pin suddenly increases causing D_{p1} to become forward-biased and redirects most of the current away from the core towards V_{DD}. The remaining current goes through R_S and D_{p2}, which act as a second layer of protection by allowing an extra voltage drop before the gate oxide. The rapid change in the supply voltage activates the NMOS clamp that enables a low impedance path to ground, thus protecting the core circuits [6]. During a negative charge ESD event, the circuit behaves very similarly, except that $D_{n1,2}$ are forward-biased and the power clamp is not used. The simplicity and effectiveness of this technique has made it omnipresent in modern ICs.

During normal operation, the input voltage, V_{in}, lies between the supply rails and thus the ESD diodes are reverse-biased. The ESD diode's current can be expressed by the Shockley equation

$$I = I_s\left(e^{\frac{\Delta V}{nV_T}} - 1\right) \tag{1}$$

where I_s is the reverse bias saturation current, V_T is the thermal voltage, and n the ideality factor. As illustrated in Fig. 2(b), ignoring leakage from the core-circuits, one can express the input leakage current as

$$I_{leak} = I_{VDD} - I_{VSS} = I_s\left(e^{\frac{V_{in}-V_{DD}}{nV_T}} - e^{\frac{-V_{in}}{nV_T}}\right) \tag{2}$$

where I_{VSS} and I_{VDD} are the diode currents to V_{SS} and V_{DD}, respectively. As can be seen from (2), if the voltages across the diodes is not identical or if there is any mismatch between the diodes, an undesired current will "leak" into/out of the input. Since I_S is proportional to the diode area and ESD diodes are large to be able to pass amperes of current during an ESD event, it causes the leakage current during normal operation to be ~100 fA and very sensitive to temperature, reaching nA levels at high temperatures. This is problematic for high impedance sensors and ultra-low current measurements as it can cause voltage drifts or drown out the signal entirely [4].

C. Low-Leakage ESD Protection Circuit

Stacking multiple ESD diodes has commonly been believed to reduce the leakage and parasitic capacitance from the ESD diodes and is used frequently in RF applications. The theory behind this is straightforward, as illustrated in Fig. 2(c). As more diodes are stacked, the voltage across each diode is reduced and so is the leakage. Considering N diodes in series, the leakage current given by (1) is

$$I_{leak} = I_s\left(e^{\frac{(V_{in}-V_{DD})/N}{nV_T}} - e^{\frac{-V_{in}/N}{nV_T}}\right). \tag{3}$$

While this seems to indicate that the leakage should be significantly reduced, the parasitic bipolar junction transistor (BJT) formed by the diode is the dominant source of leakage and thus this structure actually has worse leakage than the standard structure. Another significant drawback of this technique is that as N is increased, the risk of an ESD failure increases. During an ESD event, the voltage required to activate the diode stack and the turn-on resistance of the protection circuit also increases [8]. This results in an undesirable trade-off between the ESD protection provided and the input leakage current.

III. Ultra-low Leakage ESD Protection

The proposed ultra-low leakage (ULL) ESD technique is illustrated in Fig. 3(a). The concept of integrating a buffer to reduce the capacitance of the ESD diodes and the leakage of the pads has been reported in the literature and is used in industry [9-11]; however, this technique remains relatively unknown and is poorly characterized. Specifically, there is limited published data on the ESD resilience, the noise, and the leakage of the ULL ESD pads. This work addresses these shortcomings and directly compares other structures.

A. Concept

The key idea behind the circuit's operation is analogous to guarding; the input voltage is tracked by a unity-gain buffer, whose output drives the voltage across the center ESD diodes thereby ensuring an extremely low leakage current. Another advantage of this technique is that it provides better ESD protection than the stacked diodes as it can achieve fA-

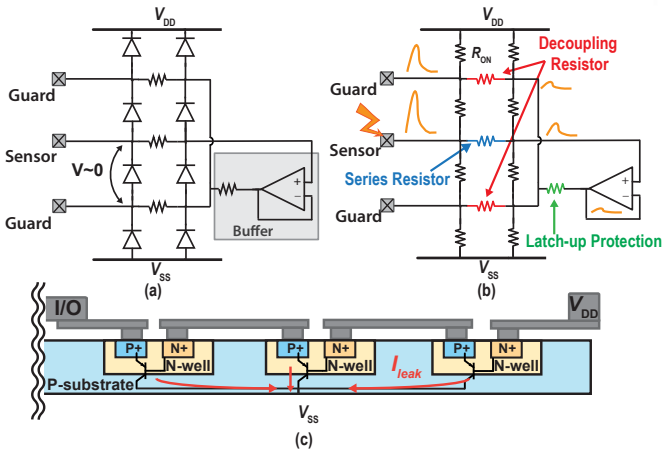

Fig. 3. ULL structure (a) schematic and (b) equivalent circuit during an ESD event. (c) Cross-section of a P-type diode stack illustrating parasitic BJT formed with the substrate.

level leakage with a string of only two diodes compared to the number of diodes required for the low-leakage structure to achieve similar leakage performance. Furthermore, since the voltage across these diodes is minimal, they can be sized larger to pass more current during an ESD event while maintaining low leakage. Lastly, it should also be noted that the output of the buffer can be directly used to drive the PCB guard trace, which is necessary for guarding.

B. Buffer Design Guidelines

Several factors warrant consideration when designing the buffer, namely: 1) The input/output range since the buffer needs to track the entire input range required by the application. Depending on how the input is used, this may be clamped (*i.e.* by an amplifier) as in most current inputs requiring very little range or it may need to be rail-to-rail for a voltage input. 2) The offset voltage since this will cause a voltage drop across the ESD diodes and add leakage. 3) The input bias current should be minimized because it directly adds to the leakage. This is readily addressed using thick-gate devices. 4) Ideally, the buffer area should be minimal. 5) The noise from the buffer should be limited to not degrade the system's performance. The buffer implemented in this work is a self-biased, single-stage differential amplifier with a dc gain of 42 dB, unity gain bandwidth of 5 MHz, input-referred noise of 15 μV_{rms}, power consumption of 15 µW, and an area of 0.002 mm^2. The input transistors were arranged in a common-centroid configuration to minimize the offset ($\mu <$ 2 mV and $\sigma = 1.5$ mV based on simulation). The buffer was designed and laid-out to fit the area of the standard TSMC ESD cells. This allows for the design of a custom ESD cell that integrates in the pad ring together with the standard foundry-provided structures. This constraint led to the choice of a very simple buffer architecture, which limits the input to 0.5 – 1.5 V.

Several precautions need to be taken to guarantee that the buffer itself can endure ESD events. First, the I/O pad cannot be connected directly to the input of the buffer otherwise there is an elevated risk of gate oxide breakdown. Second, the output of the buffer cannot be connected directly to the center of the diode string. During an ESD event, the diodes act as a voltage divider, which can cause the buffer output to latch-up. Fig. 3(b) shows how the protection resistors help to remedy these issues. First, like the standard ESD for a gate

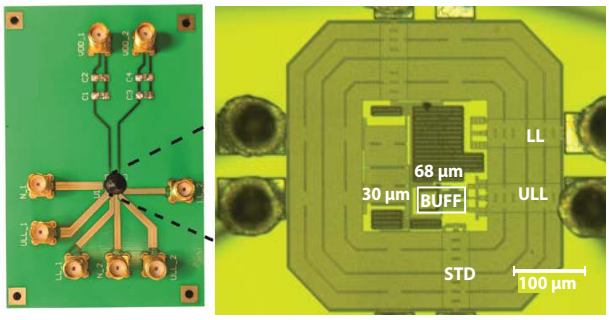

Fig. 4. PCB photograph and chip micrograph.

input, a second ESD stage is used with a series resistor. These decoupling resistors (shown in red) reduce the interference between the two stages of diode strings during an ESD event. Since the diode on-resistance, R_{ON}, is only of a few ohms, a resistance of 500 Ω provides enough isolation. Second, a protection resistor (also 500 Ω) is added at the buffer output (shown in green) to allow an additional voltage to drop preventing latch-up. All resistors were implemented as poly-resistors to minimize leakage and sized to be able to handle the transient current due to ESD events. It is important to note that during an ESD event, the buffer will not alter the ESD protection circuit's transient behavior, and it will behave as the standard case. This can be explained by the fact that it is placed after the second layer of protection and has limited bandwidth. Indeed, ESD discharge events are extremely fast (<5 ns), which is much faster than the buffer response time.

Concerning the noise contribution of the ULL circuit, it should be limited in the frequency range of interest (typically <1 kHz for most sensor applications) as the buffer's noise can couple back to the input through the bootstrapped diodes. However, since the diode's equivalent resistance is very large (> 1 TΩ), the buffer's output is effectively disconnected from the input and any buffer noise is heavily attenuated. This was verified through simulation with a transimpedance amplifier front-end and the noise of the ULL ESD system was on the same order as the standard and low-leakage (LL) protection circuits and two orders of magnitudes below the noise of state-of-the-art current front-ends [1], [4].

C. Diode Type and Size Selection

When using a stacked diode structure, one must use P-type diodes to avoid shorting the stack through the substrate. However, this causes the formation of parasitic BJTs formed with the substrate and results in extra-leakage [12], as illustrated in Fig. 3(c). These parasitic BJTs are not typically accounted for in the diode modeling, requiring explicit BJTs to be added in simulation to account for the extra leakage. This leakage will be dependent on the β of the parasitic BJT devices making it very temperature dependent. The BJT leakage increases with N as the V_{BE} of the individual BJTs will be reduced thus leading to weaker reverse biasing and higher leakage. Concerning the diodes' sizing, a good starting point is to size the diodes used in the stack similar to the standard cell ESD diodes, ~16 μm^2 in this technology, and use simulation to increase the size of the diodes to trade-off ESD resilience and leakage. In our case, all diodes were selected to be the same size as the standard cell diodes. For minimum leakage, the diodes should be sized as small as possible while making sure that they can still pass the required current during an ESD event.

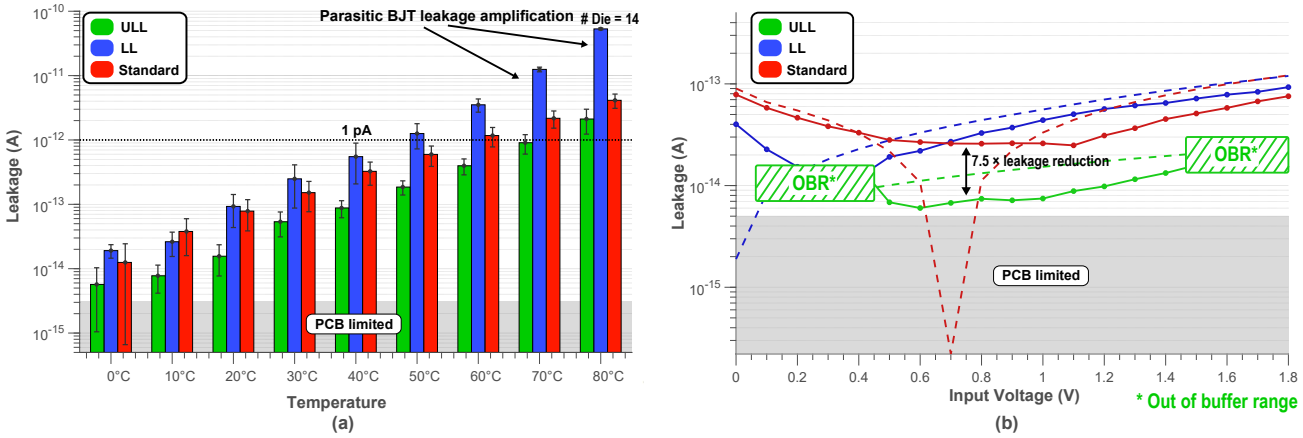

Fig. 5. (a) Measured maximum leakage between 0.5 – 1.5 V across temperature. (b) Measured (solid) and simulated (dashed) mean absolute leakage across the input voltage range at 20 °C.

IV. Measurement Results

To compare the performance of the different ESD protection circuits discussed in this paper, these circuits were fabricated in a 0.18 µm CMOS process on the same die. The standard ESD was taken directly from the foundry-provided library and the LL ($N = 4$) and ULL ($N = 2$) protection circuits were designed with similar sizes and type diodes (P-type) for a fair comparison.

A. Leakage Current Measurement

The I/O leakage was measured using a source meter (Keithley 6430) in a temperature-controlled chamber (TEQ 123H). A bare Rogers 4003C PCB (Fig. 4) was washed per the previously described protocol and the leakage was measured to be around 5 fA (20× lower than the unwashed PCB and ~20,000× lower than a standard FR4 PCB). A total of 14 dies were measured and the maximum leakage of each ESD structure across the buffer input voltage range (0.5 – 1.5 V) over temperature is shown in Fig. 5(a). The ULL circuit has a maximum leakage of ~2 pA over the commercial temperature range (0 – 85 ºC) and, at room temperature, the leakage is dominated by the PCB. Compared to the standard ESD and LL structures, the ULL ESD circuit has 7.5× lower leakage at room temperature and the lowest leakage across temperature. The LL structure performs poorly since standard P-type ESD diodes were stacked leading to amplification of the leakage current by the parasitic BJTs, which becomes apparent at higher temperatures. This effect, albeit at a smaller scale (due to the lower number of diodes in the stack), can also be observed to significantly increase the ULL ESD structure's leakage at higher temperatures. Fig. 5(b) compares the simulated leakage current (with explicit BJTs added to model the parasitic effect) against the average measured absolute leakage current. The leakage cancellation phenomenon discussed in Section II.B and, as seen in the simulation results, is not visible in the presented data because the voltage at which cancellation occurs depends on process variation. Since the plotted leakage is averaged across multiple dies ($n = 14$), this cancellation behavior is smoothed out. This was, however, observed in individual measurements.

B. ESD Stress Test

Human-to-chip interactions are a significant source of ESD events, which is why the human-body model (HBM) is one of the most common standards used for IC reliability verification. It requires the circuit to be able to handle 0.2 µC (2 kV) discharged from a 100 pF capacitor through a 1.5 kΩ resistor resulting in a transient current at the contact node of ~1.3 A [13]. Using the setup described in the standard and starting at 200 V, each pad was shocked 3× with an ESD tester (EMC Partners ESD 3000). If the measured leakage was within 3σ of the pre-shock value, the voltage was increased by 100 V. This procedure was repeated until failure for 6 different chips and the testing order was randomized to ensure that the results were not influenced by cross-channel stress. Table I reports the lowest recorded failure voltage for each ESD structures together with their leakage performance. As expected, the standard ESD performed the best, followed by the ULL, and finally the LL, which was extremely sensitive. The ESD stress test followed the testbench provided in the JEDEC/ESDA standard and we demonstrated that the ULL structure meets the HBM requirements.

TABLE I. COMPARISON OF ESD STRUCTURES.

	Standard	Low Leakage	Ultra-Low Leakage
ESD Diode Area	120 µm²	5000 µm²	360 µm²
Buffer Area	N/A	N/A	0.002 mm²
Power Overhead	N/A	N/A	15 µA
Mean Maximum Leakage @ 20 °C	80 fA	93 fA	10.5 fA
HBM Robustness	6 kV	0.5 kV	5 kV
Meets HBM Spec?	Yes	No	Yes

V. Conclusion

A technique enabling sub-pA leakage across the entire commercial temperature range while still having robust ESD protection was presented, analyzed, and characterized. It was shown to out-perform the standard low-leakage technique both in terms of leakage and ESD performances while only adding 15 µW and 0.002 mm² power and area overhead. This leakage could be further improved in a double N-well process by avoiding the parasitic BJTs that limit the performance at higher temperature. This is a valuable approach to maintain circuit robustness without introducing noise or leakage that are critical in high-performance instrumentation and sensor applications.

REFERENCES

[1] C.-L. Hsu and D. A. Hall, "A current-measurement front-end with 160dB dynamic range and 7ppm INL," in *IEEE ISSCC*, Feb. 2018

[2] Y. M. Chi *et al*., "Ultra-High Input Impedance, Low Noise Integrated Amplifier for Noncontact Biopotential Sensing," *IEEE J. Emerg. Sel. Top. Circuits Syst*, vol. 1, no. 4, pp. 526–535, Dec. 2011.

[3] T. Rooijers *et al*., "An Auto-Zero Stabilized Voltage Buffer with a trimmed input current of 0.2pA," *IEEE ESSCIRC*, Sep. 2019.

[4] D. Djekic *et al*., "A 0.1% THD, 1-MΩ to 1-GΩ Tunable, Temperature-Compensated Transimpedance Amplifier Using a Multi-Element Pseudo-Resistor," *IEEE JSSC*, vol. 53, no. 7, pp. 1913–1923, Jul. 2018.

[5] J. E. Vinson and J. J. Liou, "Electrostatic discharge in semiconductor devices: an overview," *Proc. IEEE*, vol. 86, no. 2, pp. 399–420, Feb. 1998.

[6] M.-D. Ker, "Whole-chip ESD protection design with efficient VDD-to-VSS ESD clamp circuits for submicron CMOS VLSI," *IEEE Trans. Electron Devices*, vol. 46, no. 1, pp. 173–183, Jan. 1999.

[7] C. Wang and M. Ker, "Design of Power-Rail ESD Clamp Circuit With Ultra-Low Standby Leakage Current in Nanoscale CMOS Technology," *IEEE JSSC*, vol. 44, no. 3, pp. 956–964, Mar. 2009.

[8] M. Ker *et al*., "ESD protection design for CMOS RF integrated circuits," *EOS/ESD Symposium*, 2001.

[9] M. Corsi, "Low leakage ESD network for protecting semiconductor devices and method of construction," U.S Patent 5563757A, Oct. 8, 1996.

[10] "ADA4530-1 Datasheet and Product Info | Analog Devices."

[11] "LTC6268-10 Datasheet and Product Info | Analog Devices."

[12] S. Chen *et al*., "Low-leakage diode string designs using triple-well technologies for RF-ESD applications," *IEEE Electron Device Lett.*, vol. 24, no. 9, pp. 595–597, Sep. 2003.

[13] *Joint JEDEC/ESDA Standard For Electrostatic Discharge Sensitivity Test - Human Body Model (HBM) - Component Level*., JEDEC Standard JS-001-2017, May 2017