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Ultra-Low Leakage ESD Protection Achieving 10.5 fA Leakage

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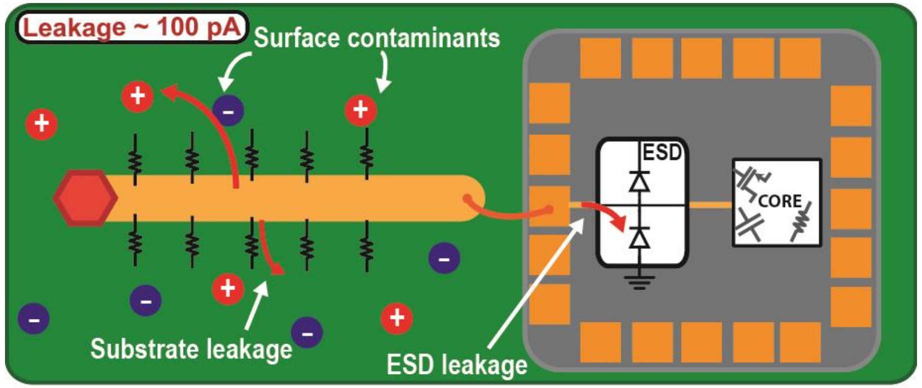
Need for Low-Leakage Interfaces

Many applications require input leakage below 50 fA:

- High-precision current front-ends
- High impedance sensor interfaces
- Ultra-low leakage voltage buffers

Achieving low leakage is challenging both at the PCB and chip level:

- FR4 PCB substrate’s resistivity is limited
- Surface contaminants are deposited on the PCB during fabrication and handling
- ESD protection diodes leakage is typically >100 fA

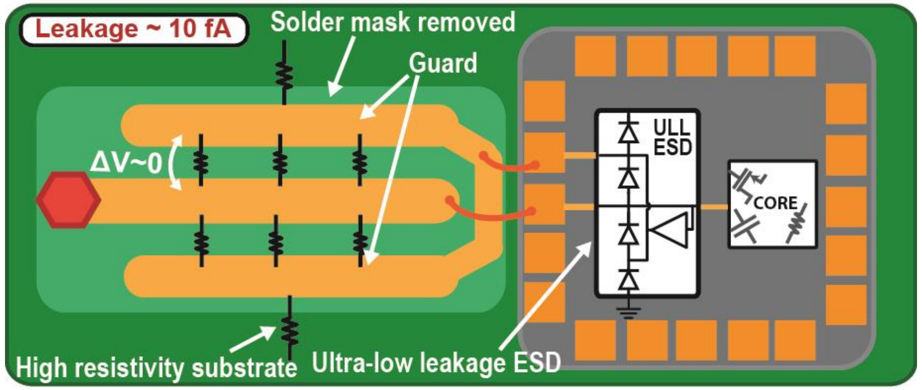


Techniques for Low-Leakage

Several techniques reduce the PCB leakage:

- Addition of guard traces surrounding the sensitive trace
- Removal of solder mask to avoid charge trapping
- Selection of a high resistivity substrate (*e.g.*, Rogers 4003C)
- Washing and baking to remove surface contaminants

PCB leakage reduced to **< 10 fA** → Need to reduce the ESD leakage



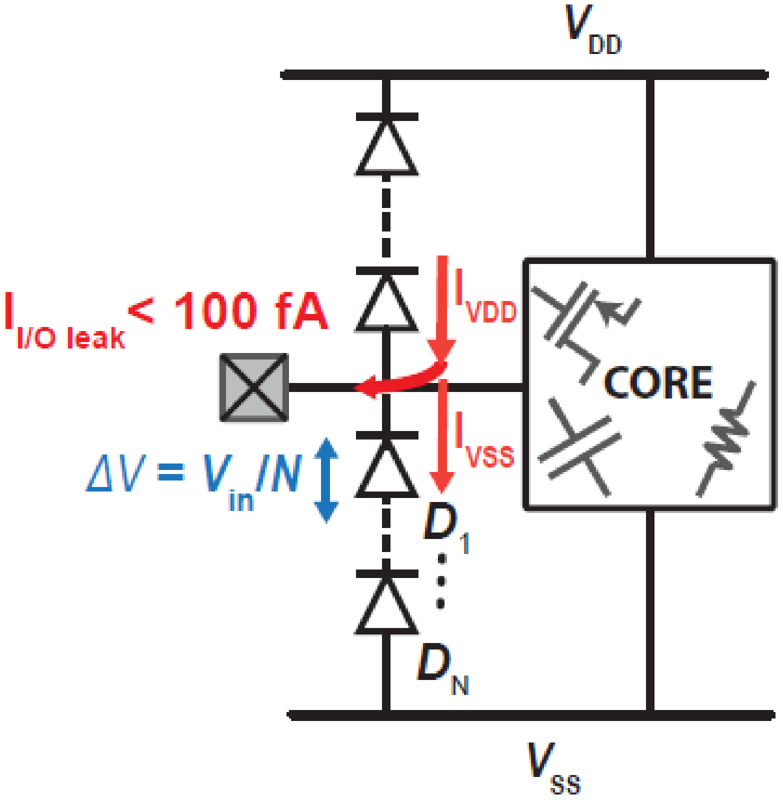
Typical solution for low leakage

Key idea: Reduce the voltage across the diodes to reduce leakage

Typical solution: Stack diodes to reduce ΔV

Problems:

- Need large diode stack for low leakage
- Reduces the ESD resilience of the circuit



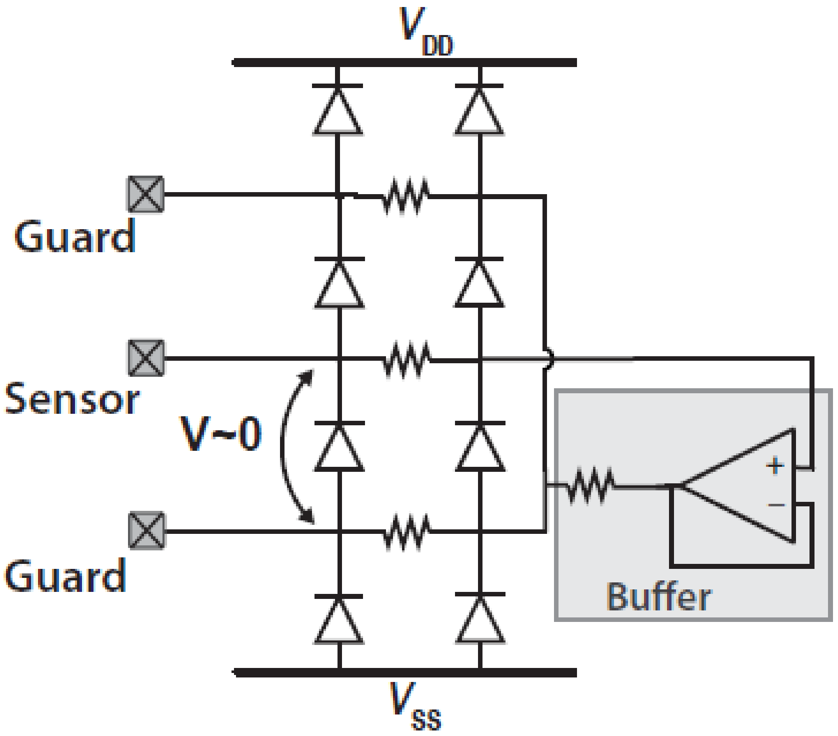
Proposed ESD Structure

Key idea: Reduce the voltage across the diodes to reduce leakage

Proposed Solution: Use a buffer to drive the voltage to ~0V

Buffer design guidelines:

- Thick oxide input devices
- Maximize input range
- Minimize offset through sizing and layout
- Minimize area & power

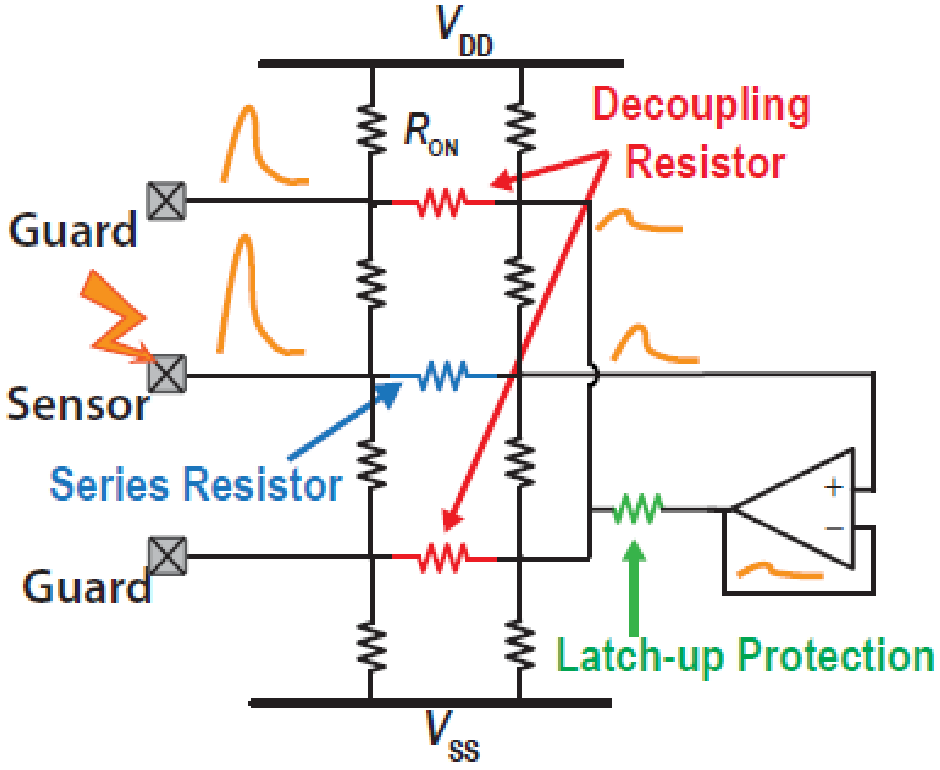


ESD resilience

ESD event : Extremely fast discharge (10s ns) of large current (1A)

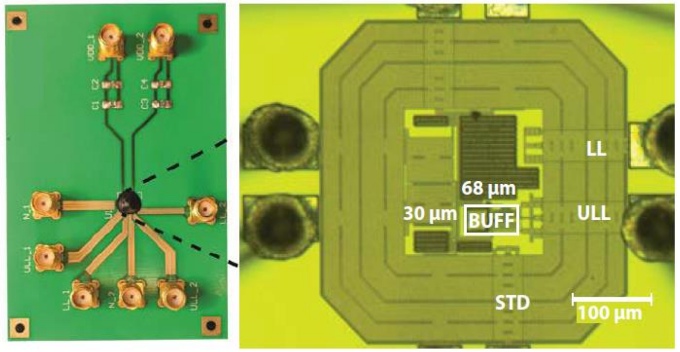
ESD resilience guidelines:

- Minimize diode stacking
- Decoupling resistors between stages
- Latch-up protection resistor at the amplifier output



Test Chip and Measurement Setup

Test chip fabricated in **TSMC 180 nm** process



Three ESD structures implemented:

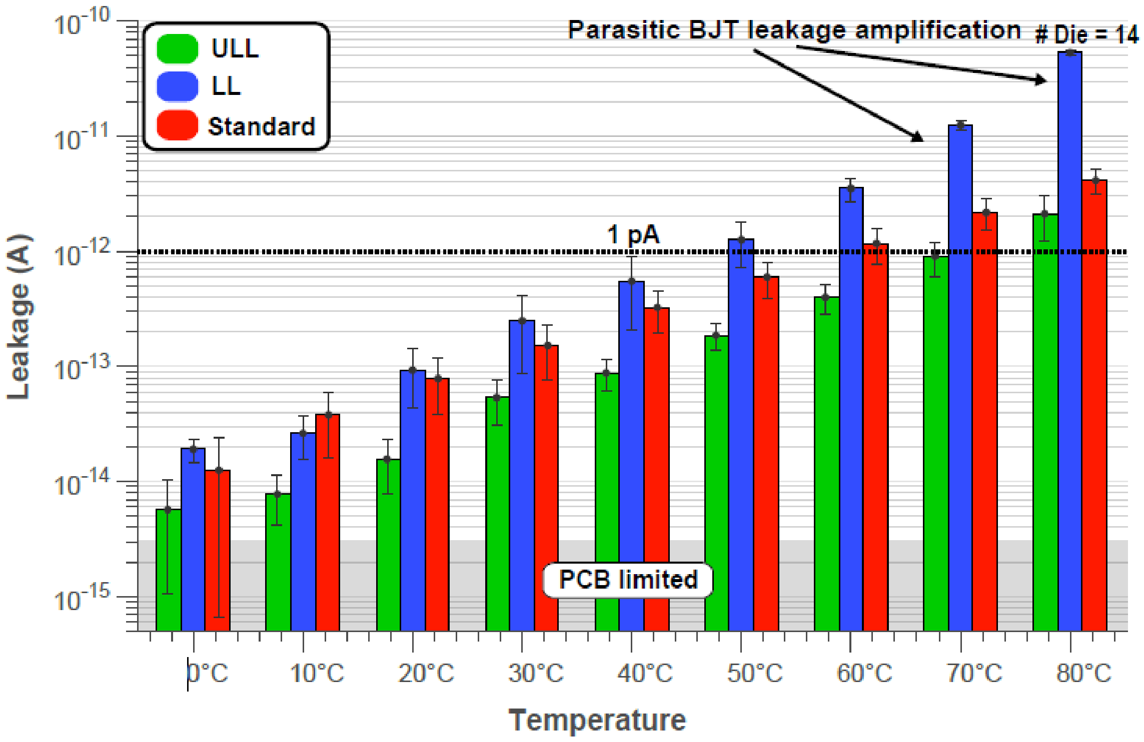
- 1 diode standard (STD) structure
- 4 diodes stack low-leakage (LL) structure
- 2 diode stack with bootstrapping ultra-low-leakage (ULL) structure

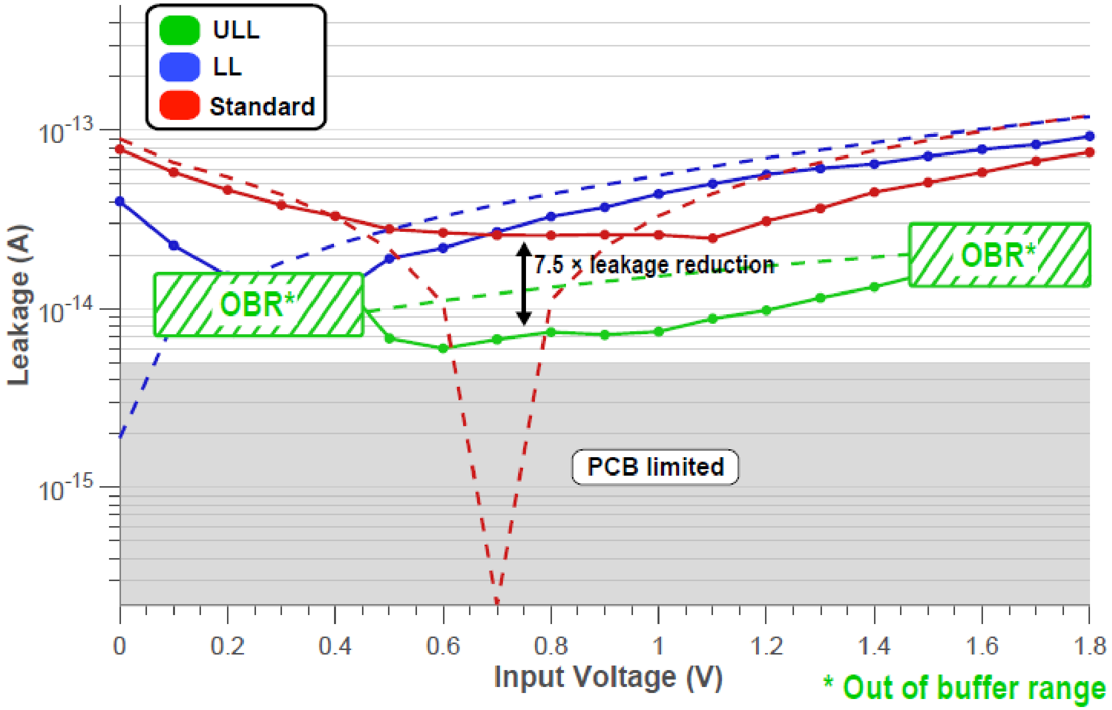
Leakage measured using a source meter (**Keithley 6430**) in a temperature-controlled chamber (**TEQ 123H**)

- Bare PCBs exhibited a **~5 fA** leakage
- Chips bonded directly on board to avoid package leakage

Leakage Measurements

Leakage measurements performed on **14** die across temperature and voltage





ULL structure improves the leakage performance by 7.5× and $I_{\max}$ = 10.5 fA!

Conclusion

Some applications require extremely low leakage at the input interface that can’t be achieved with standard PCB and ESD design.

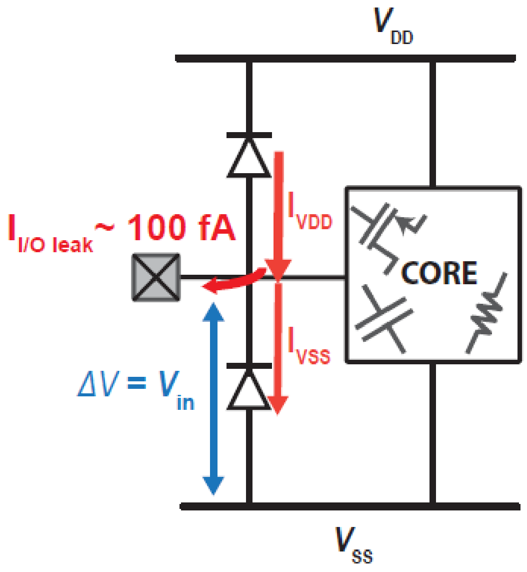
Paper’s contribution:

- Review of low leakage techniques for PCB and ESD
- Analysis and characterization of a diode bootstrapping technique for leakage reduction
- ESD resilience verified with Human-body model (HBM) ESD testing

Key results:

- **<10.5 fA** leakage in the input range of interest at room temperature
- High resilience to HBM ESD event (**5 kV**)
- Low power (**15 μW**) and area (**0.002 mm^2**) overhead

S1 - Standard ESD Structures

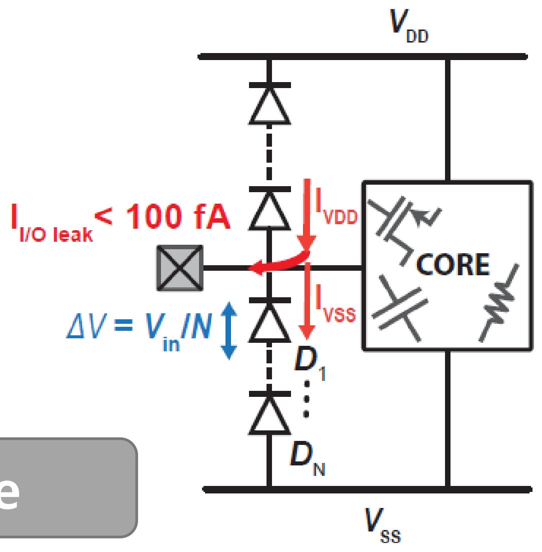


Typical ESD structures composed of diodes to the supply rails

- Shunt current in the event of an ESD event
- Large diodes to pass mA – A
- Multiple stages to improve protection (typically 2 for gate inputs)

The ESD diodes cause leakage

$$I_{\text{leak}} = I_{\text{VDD}} - I_{\text{VSS}} = I_{\text{s}}\left(e^{\frac{V_{\text{in}}-V_{\text{DD}}}{nV_{\text{t}}}} - e^{\frac{-V_{\text{in}}}{nV_{\text{t}}}}\right)$$



Intuitive solution is to stack multiple diodes

$$I_{\text{leak}} = I_{\text{VDD}} - I_{\text{VSS}} = I_{\text{s}}\left(e^{\frac{V_{\text{in}}-V_{\text{DD}}}{nV_{\text{t}}\boldsymbol{N}}} - e^{\frac{-V_{\text{in}}}{nV_{\text{t}}\boldsymbol{N}}}\right)$$

Stacking reduces leakage but also ESD resilience

S2 - BJT leakage

Issue:

- Simulated and measured leakage deviates significantly.
- Leakage much worse at high temperature

Cause:

- Leakage limited by the parasitic BJTs formed with the substrate

Solution

- Effect could be reduced by using double N-well diodes with well tied to supplies