The price for integrated bioelectronics: Quantifying the impact of e-beam post-processing

Zhaoyi Liu[1], Sang Heon Lee[1,2], Omid Ghadami[1], and Drew A. Hall[1]
[1]Department of Electrical and Computer Engineering, University of California San Diego, La Jolla, CA, USA
[2]Avery Digital, San Diego, CA, USA
drewhall@ucsd.edu

***Abstract*—The benefits of co-integrating sensors and electronics are well known, yet many biosensors require post-processing to realize sensor or actuator structures above CMOS integrated circuits. This is typically accomplished with Electron Beam Lithography (EBL) for patterning small geometry features. However, the optical alignment with respect to the on-chip alignment marks heavily affects the precision of such patterning. Moreover, high-energy electrons can damage the underlying transistor circuits, resulting in performance degradation. This paper investigates how to design the alignment marks for robust EBL pattern-transferring and the degradation effect and affected area of EBL patterning on CMOS transistors. Results show that the different device types (PMOS, NMOS, thick-oxide, thin-oxide) can be affected to different degrees by EBL, and while metal shielding offers no mitigation for such degradation, an efficient technique is to avoid a "blast radius" of 60 µm around the EBL site for circuit protection.**

Keywords—integrated biosensors, electron beam lithography, CMOS post-processing, electron impact ionization

I. Introduction

Biosensors enable one to observe or detect biological phenomena (*e.g.,* DNA hybridization, antibody-antigen binding, cell-based assays) with electronic readout, as shown in Fig. 1(a). These sensors have unique requirements for noise, readout speed, sensitivity, and form factors. Furthermore, these sensors are often very high impedance (>MΩ) or heavily arrayed (>1k pixels), necessitating monolithic integration with the readout circuitry [1]–[5]. Co-integration typically involves post-processing a CMOS die/wafer to add the transducer or open structures in underlying CMOS layers. While this integration results in shorter routing, lowering the parasitics and improving the sensitivity, it is challenging to pattern these sensors as they can be µm- to nm-scale. The patterning often requires lithography, where a resist layer is patterned to enable selective etching or lift-off. Electron beam lithography (EBL) is a common nano-fabrication technology in low-volume production and academic settings due to its versatility despite the low throughput. With EBL, an electron beam is guided by a magnetic field and optical lenses to pattern an electron-sensitive resist by electron bombardment [6], [7]. Since EBL offers high-resolution (nm-scale) and maskless pattern formation, it is increasingly utilized to co-integrate sensors and electronics, particularly in integrated biosensors and bioelectronics with MEMS, nanoelectrodes, nanogaps, microneedles, and nanowires [7]–[9].

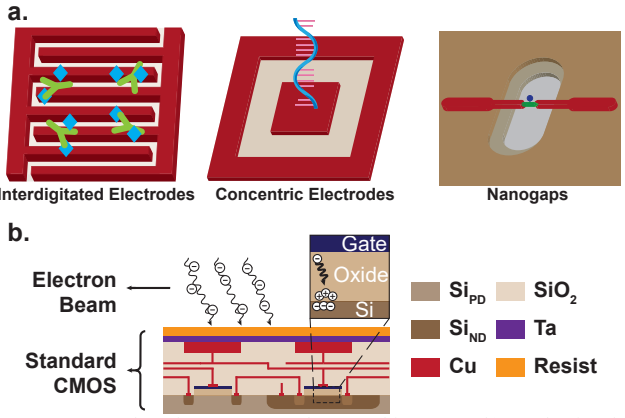

Fig. 1. a) Examples of post-processed CMOS biosensors; b) Mechanism by which EBL can degrade transistors performance through traps.

Despite EBL's growing popularity in nano-fabrication, device degradation due to e-beam irradiation is well known [10]–[17]. When electrons are accelerated at high energy (~100 keV), they penetrate through the passivation, metals, inter-layer dielectrics, and gate oxides, exciting electron-hole pairs by collisions. The secondary electrons from these collisions can scatter, spreading to an area larger than the e-beam aperture. The electrons and/or holes impregnate the gate oxide with enough energy to create traps and interface trap states, as shown in Fig. 1(b). These traps alter the electric field in the oxide and channel, degrading the device performance (*e.g.*, increased leakage, threshold voltage shift, carrier mobility changes, etc.). This effect is most pronounced near the EBL alignment marks since the EBL tool uses these for precise registration, and it can be exposed to the e-beam tens of thousands of times while patterning arrayed structures [3]. Without proper dosage selection or mitigation techniques, this can lead to transistor breakdown and circuit failures.

While there is currently little in the literature to offer designers guidance, this study aims to investigate the practical considerations of EBL for CMOS post-processing. A CMOS test chip was taped out in TSMC 65 nm GP due to its maturity and popularity for biomedical integrated circuits. Several alignment mark variants were constructed to understand what was needed for successful auto-alignment, and a 10×10 pixel array was designed to quantify EBL's transistor degradation effects, determine the effective "blast radius" from secondary scattering, and assess the utility of shielding to mitigate such degradation.

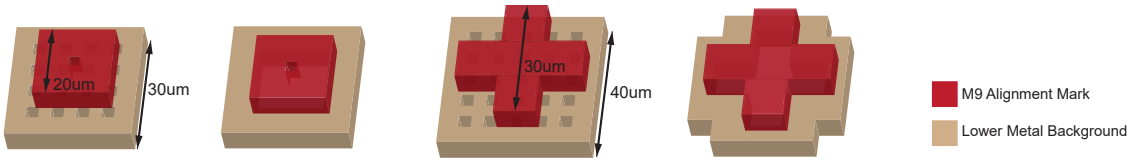

Fig. 2. Layout of the EBL alignment marks for auto-alignment experiments. The top metal is contrasted by a background made by a lower metal layer.

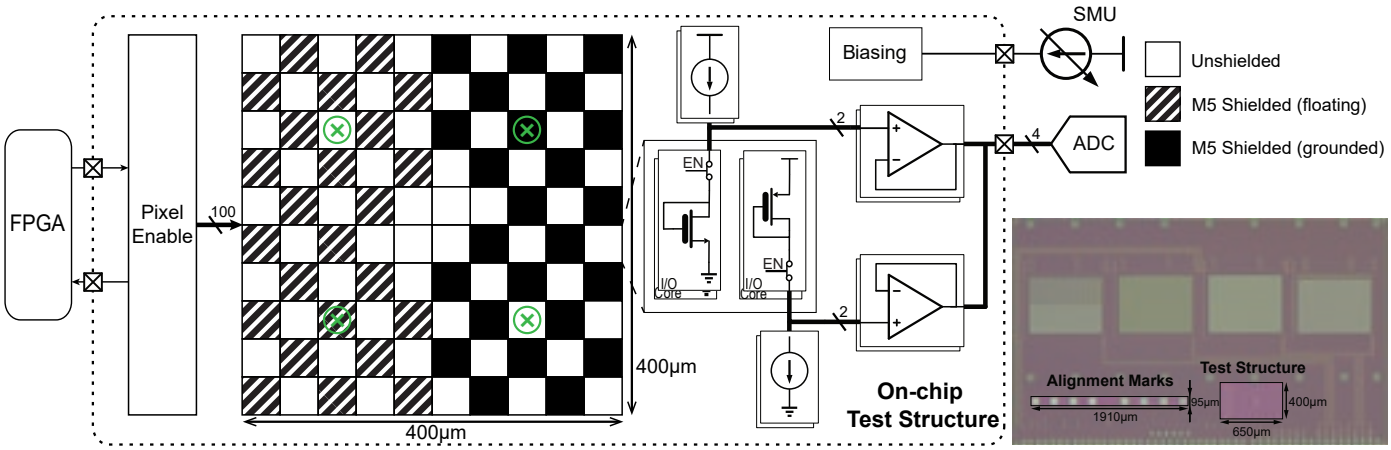

Fig. 3. Schematic of the test structure array for EBL degradation effect experiments. Floating shields (shaded) and grounded shields (solid black) on Metal 5 form a checkerboard layer on top of the array. The four e-beam sites are marked in green. Inset shows an annotated die photograph.

II. Alignment Marks

The EBL writing system employs an electromagnetic lens and a beam deflector to steer the electron beam during lithography. For high-precision, nanoscale feature patterning, the EBL tool must refer to an on-chip alignment mark as the "origin" for the writing process. In practice, multiple alignment marks are used to correct for tilt and rotation of the wafer. Hence, the first step of EBL involves detecting and aligning the system with these fiducials. In each EBL writing cycle, the system is programmed to guide the electron beam to start from the alignment mark, move to the patterning site for writing, then return to the alignment mark. A failure of the auto-alignment can affect the patterning precision, cause incorrect patterns to be written, or result in low throughput. Therefore, constructing a reliable alignment mark for robust pattern referencing and transferring is crucial.

The alignment mark pattern varies by tool, but common patterns include squares and crosses (10×10 µm^2), with some more advanced tools requiring complex diffraction patterns (100×100 µm^2). They are typically placed on the top metal layer with conventional guidance to avoid all metal layers nearby. While possible in some technology nodes, this becomes overly burdensome in newer technologies with tight metal and via density requirements. As such, we investigated whether the tool could still auto-align with other metal structures nearby.

Figure 2 shows four alignment mark structures where the primary feature is placed on Metal 9 (the top metal layer), while the background is individually constructed from Metal 1 to 8. A hole was cut out in the center of the square alignment marks to meet the metal slotting rule. Similarly, the background layer was either slotted or removed underneath the alignment mark to meet all design rules. Using a Vistec EBPG5200 e-beam pattern generator, we experimentally found that the tool recognized all alignment mark variants. No significant speed/performance degradation or misalignment was found for any alignment mark, even when the background layer was on Metal 8, defying the conventional wisdom that surrounding metals should be avoided.

III. Quantifying Transistor Degradation

A. Experimental setup

To quantify the degradation of transistors and the affected area from EBL, a 10×10 matrix of 40×40 µm^2 test pixels was designed. As depicted in Fig. 3, each pixel consists of four diode-connected transistors: PMOS thick gate-oxide (I/O), PMOS thin gate-oxide (core), NMOS I/O, and NMOS core devices with an enable switch. All transistors are minimum-sized (I/O devices: W/L = 400 nm/280 nm, core devices: W/L = 370 nm/60 nm). To evaluate the efficacy of shielding, pixels on a checkerboard pattern have a Metal 5 shield where the right half are floating and the left half are connected to V_{SS}.

The EBL blast radius experiment was conducted by spin coating EBL resist (950 PMMA A9, 1 µm thick) and then writing the four "quadrant" centers. The exact EBL sites are marked in green in Fig. 3. The Vistec EBPG5200 was set to a nominal 100 keV operation, and the dosage was adjusted across different chips to investigate dosage impact on transistor degradation. The low-dosage mode consists of two passes of 1120 µC/cm^2, while the high-dosage mode is two passes of 1750 µC/cm^2. These levels correspond to those often required for patterning thick resist without photolithography. One can effectively compare how the different shielding techniques mitigate transistor degradation since all pixels (*i.e.*, unshielded, floating, and grounded) are processed simultaneously.

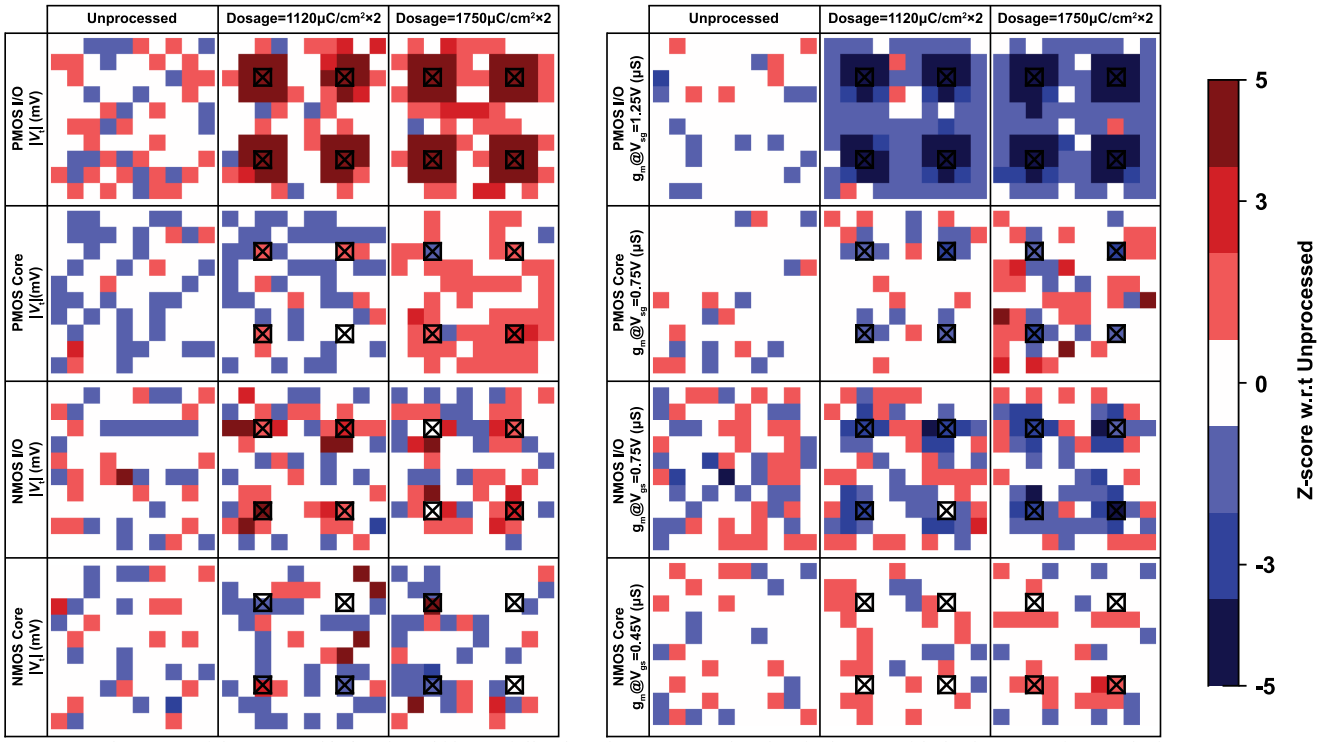

Fig. 4. Measured Z-score of the extracted $|V_t|$ and g_m shifts spatially plotted to correspond to the pixel array, with the four EBL sites marked.

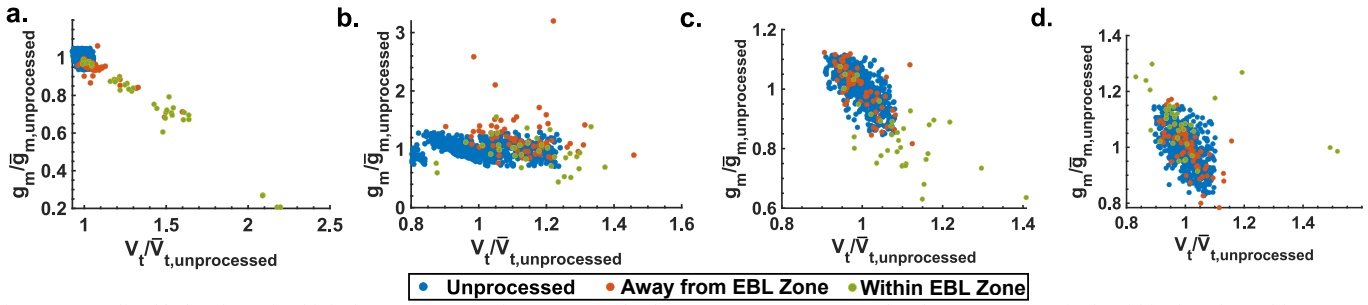

Fig. 5. Normalized $|V_t|$ and g_m after high-dosage treatment for a) PMOS I/O; b) PMOS core; c) NMOS I/O; d) NMOS core. Pixels within the e-beam blast zone (9 pixels centered around the e-beam site) are plotted with the pixels outside the zone and the unprocessed pixels.

Each pixel was sequentially activated using an FPGA to control the scan chain during the measurement. The transistors' drain current, I_d, was swept using a Keysight B2912A Source Measurement Unit (SMU) and the on-chip current mirror. The transistors' gate-to-source voltages, V_{gs}, were measured using an 18-bit analog-to-digital converter (PCI-6281, National Instruments, USA) while sweeping I_d. The transistors' threshold voltage, V_t, and transconductance, g_m, were extracted from the measured I-V curves using MATLAB scripts; V_t was extracted using the saturation-region linear extrapolation method [18], while the transconductance was calculated as $\partial I/\partial V$ at a fixed operating point (PMOS I/O: V_{sg}= 1.25 V, PMOS core: V_{sg}= 0.75 V, NMOS I/O: V_{gs}= 0.75 V, and NMOS core: V_{gs}= 0.45 V).

B. Experimental results

The measurement results are plotted in Fig. 4, where the V_t and g_m extracted values for all devices are visualized in a heatmap to depict the spatial impact of EBL damage. To preserve the proprietary process information and account for underlying process variation, the Z-score of V_t and g_m are calculated as

$$Z(x) = \frac{x - \mu_x}{\sigma_x} \quad (1)$$

where x is the measured value (V_t or g_m), μ_x is the mean value for all unprocessed chips (n = 8 chips, each with 100 pixels/chip), and σ_x is the standard deviation of the same quantity for the unprocessed chips. Thus, the Z-score provides a statistical way to assess how far the EBL-exposed pixel is from the unprocessed pixels. All chips tested were from the same wafer. Note that since the devices are all minimum-sized, there is a significant mismatch, even on the unprocessed chip. However, most of the unprocessed chip, shown in Fig. 4, is within ±2σ (by definition of using the Z-score), whereas the processed chips show much higher variation.

We designate the 3×3 pixels surrounding the EBL site as "within the EBL zone" for the subsequent discussion. The V_t and g_m of devices within/outside of the zone after high-dosage

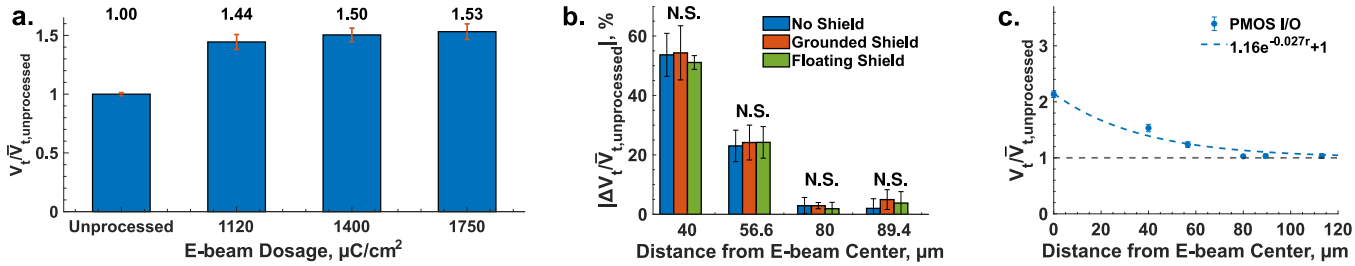

Fig. 6. a) Normalized V_t of PMOS I/O device at 40 μm from the e-beam center vs. different EBL dosages; b) $|\Delta V_t|$ of PMOS I/O device vs. distance from e-beam center after high-dosage treatment for different shields; c) Normalized V_t of PMOS I/O device vs. distance from e-beam center after high-dosage treatment.

treatment are plotted with respect to the unprocessed devices in Fig. 5. Statistical *t*-tests were performed between the pixels within the EBL zone and the unprocessed pixels, with the null hypothesis that V_t or g_m of pixels within the zone come from the same distribution as the unprocessed pixels. This determines if the measured device characteristics are dominated by EBL degradation ($p < 0.05$) or intrinsic mismatch.

1) Thick-Oxide (I/O) vs. Thin-Oxide (core) Devices

The I/O devices are more susceptible to e-beam damage than the core devices. The devices around the center of the EBL sites have the most extreme variation for I/O transistors and show a precise contour of the "blast radius." These pixels are statistically significantly different from the unprocessed devices ($p < 2.1\times10^{-28}$). The core devices are also degraded, but the effect is somewhat visually masked due to mismatch variation; however, they are also statistically significantly different ($p < 6\times10^{-12}$). This distinction between the I/O and core devices is partially attributable to the difference in sizing and the thicker gate oxide of the I/O devices, which generate more traps upon irradiation [13], [15].

2) PMOS vs. NMOS

These data show that PMOS devices are more affected than NMOS devices. The range of Z-scores for PMOS I/O devices (-23.5 to 31.6) is much higher than that for the NMOS I/O devices (-4.7 to 6.0). PMOS and NMOS core devices also show similar results, though mismatch partially masks the difference. This difference can be explained by the trap state failure mechanism, where oxide and interface traps steer V_t and g_m in different directions for PMOS and NMOS devices [15], [19].

3) Low vs. High E-beam Dosage

Figure 6(a) shows the degradation of PMOS I/O devices across EBL dosages: at 40 μm from the e-beam center, V_t is further increased by ~10% ($p < 6.2\times10^{-4}$) as dosage increases from 1120 μC/cm² to 1750 μC/cm². Additionally, as visualized in Fig. 4, the e-beam-affected area (regions with extreme Z-scores) expands when the dosage increases. These align with our hypothesis (and previous experience) that higher EBL dosage increases the chance of trap-state generation and creates more electron scattering upon bombardment. Therefore, increasing the EBL dosage causes more degradation to devices and increases the affected area. The minimum dosage should be used whenever possible.

4) Unshielded vs. Shielded

Figure 6(b) elucidates the effect of shielding. Although it was believed that a metal shield would help absorb scattered electrons and protect the devices underneath, these data show otherwise. There was no statistical difference between the floating shield and no shield ($p > 0.51$) or the grounded shield and no shield ($p > 0.53$). A shield on a thicker metal layer or a lower EBL acceleration voltage may be more effective; however, a more complex shielding structure and test setup are required to test these hypotheses. Conversely, the shielding technique may fail because the degradation is due to secondary scattering occurring underneath the shield.

5) "Blast Radius"

Figure 6(c) shows the proximity effect of the device degradation. The normalized V_t of PMOS I/O devices after high-dosage e-beam treatment is plotted since these devices exhibited the most pronounced degradation. The fitted curve shows an exponential decay with the distance from the EBL writing site. Devices more than 60 μm away from the writing site were relatively unaffected, whereas devices within 40 μm show a ~53% increase in V_t. While shielding may not be effective, increasing the distance is.

IV. Concluding Remarks

This paper explores two practical aspects of e-beam lithography post-processing in the context of integrated biosensor design. Firstly, we present a comprehensive guideline for designing a robust alignment mark for EBL system auto-alignment. This area-efficient geometric configuration ensures reliable and precise pattern transfer during lithography by incorporating precise edges and high contrast. Secondly, we constructed a test array to investigate the degradation effect of e-beam irradiation on transistors close to the EBL site. The measurement results reveal that PMOS I/O devices are particularly vulnerable to shifts in threshold voltage and transconductance caused by excessive e-beam irradiation. We showed that applying a single metal shielding layer provides insignificant mitigation. We also determined that critical circuitry placements should avoid an area of 120×120 μm² centered around the e-beam site, referred to as the "blast radius", due to the adverse impact observed in this region. While these effects may be specific to this photoresist, technology, and/or EBL tool, this result offers insight into circuit and post-processing optimization for robust and efficient biosensor-electronics co-integration. Furthermore, photo-lithography has advanced rapidly, and it is almost possible today to directly pattern nm-level features without using EBL, provided one has access to such advanced state-of-the-art tools.

Acknowledgment

The authors thank Sumedh Ramaprasad for helping design parts of this chip and Maribel Montero for EBL processing.

REFERENCES

[1] D. A. Hall et al., "A CMOS Molecular Electronics Chip for Single-Molecule Biosensing," in *2022 IEEE International Solid-State Circuits Conference (ISSCC)*, San Francisco, CA, USA: IEEE, Feb. 2022, pp. 1–3.

[2] C. W. Fuller *et al.*, "Molecular electronics sensors on a scalable semiconductor chip: A platform for single-molecule measurement of binding kinetics and enzyme activity," *Proc. Natl. Acad. Sci.*, vol. 119, no. 5, p. e2112812119, Feb. 2022.

[3] O. Ghadami *et al.*, "Helix: An Electrochemical CMOS DNA Synthesizer," in *2022 IEEE Symposium on VLSI Technology and Circuits (VLSI Technology and Circuits)*, Jun. 2022, pp. 66–67.

[4] A. C. Sun, E. Alvarez-Fontecilla, A. G. Venkatesh, E. Aronoff-Spencer, and D. A. Hall, "High-Density Redox Amplified Coulostatic Discharge-Based Biosensor Array," *IEEE J. Solid-State Circuits*, vol. 53, no. 7, pp. 2054–2064, Jul. 2018.

[5] "How to integrate readout electronics in next-generation tools for genomics | imec." https://www.imec-int.com/en/events/how-integrate-readout-electronics-next-generation-sequencing-tools.

[6] R. F. W. Pease, "Electron beam lithography," *Contemp. Phys.*, vol. 22, no. 3, pp. 265–290, May 1981.

[7] A. A. Tseng, K. Chen, C. D. Chen, and K. J. Ma, "Electron beam lithography in nanoscale fabrication: recent development," *IEEE Trans. Electron. Packag. Manuf.*, vol. 26, no. 2, pp. 141–149, Apr. 2003.

[8] G. Rius, J. Llobet, J. Arcamone, X. Borrisé, and F. Pérez-Murano, "Electron- and ion-beam lithography for the fabrication of nanomechanical devices integrated on CMOS circuits," *Microelectron. Eng.*, vol. 86, no. 4, pp. 1046–1049, Apr. 2009.

[9] R. Tian, S. Regonda, J. Gao, Y. Liu, and W. Hu, "Ultrasensitive protein detection using lithographically defined Si multi-nanowire field effect transistors," *Lab. Chip*, vol. 11, no. 11, pp. 1952–1961, 2011.

[10] Y. Mitsui, T. Sunaoshi, and J. C. Lee, "A study of electrical characteristic changes in MOSFET by electron beam irradiation," *Microelectron. Reliab.*, vol. 49, no. 9–11, pp. 1182–1187, Sep. 2009.

[11] H. S. Lin and C. H. Chao, "A study of the influence of electron beam on electrical characteristics of LOCOS device," in *2012 IEEE International Reliability Physics Symposium (IRPS)*, Apr. 2012, p. FA.3.1-FA.3.3.

[12] H. Noriko *et al.*, "Study on Effect of Electron Beam Irradiation in SEM-Based Nanoprobing on MOS Transistor," presented at the ISTFA 2016, ASM International, Nov. 2016, pp. 128–131.

[13] F. Campabadal *et al.*, "CMOS degradation effects due to electron beam lithography in smart NEMS fabrication," in *Smart Sensors, Actuators, and MEMS II*, SPIE, Jul. 2005, pp. 667–674.

[14] J. Jiang *et al.*, "Electron-Irradiation-Induced Degradation of Transfer Characteristics in Super-Junction VDMOSFET," *Electronics*, vol. 11, no. 13, Art. no. 13, Jan. 2022.

[15] J. R. Schwank *et al.*, "Radiation Effects in MOS Oxides," *IEEE Trans. Nucl. Sci.*, vol. 55, no. 4, pp. 1833–1853, Aug. 2008.

[16] P. T. Ng, F. Rivai, A. C. T. Quah, J. C. Alag, P. K. Tan, and C. Q. Chen, "Enhanced EBAC Detection on Gate Oxide Breakdown Isolation after High Voltage Electron Beam Irradiation," in *2022 IEEE International Symposium on the Physical and Failure Analysis of Integrated Circuits (IPFA)*, Jul. 2022, pp. 1–6.

[17] A. Paccagnella, A. Cester, and G. Cellere, "Ionizing radiation effects on MOSFET thin and ultra-thin gate oxides," in *IEDM Technical Digest. IEEE International Electron Devices Meeting,* 2004., Dec. 2004, pp. 473–476.

[18] A. Ortiz-Conde, F. J. García-Sánchez, J. Muci, A. Terán Barrios, J. J. Liou, and C.-S. Ho, "Revisiting MOSFET threshold voltage extraction methods," *Microelectron. Reliab.*, vol. 53, no. 1, pp. 90–104, Jan. 2013.

[19] K. F. Galloway and R. D. Schrimpf, "MOS device degradation due to total dose ionizing radiation in the natural space environment: A review," *Microelectron. J.*, vol. 21, no. 2, pp. 67–81, Jan. 1990.