The price for integrated bioelectronics: Quantifying the impact of e-beam post-processing

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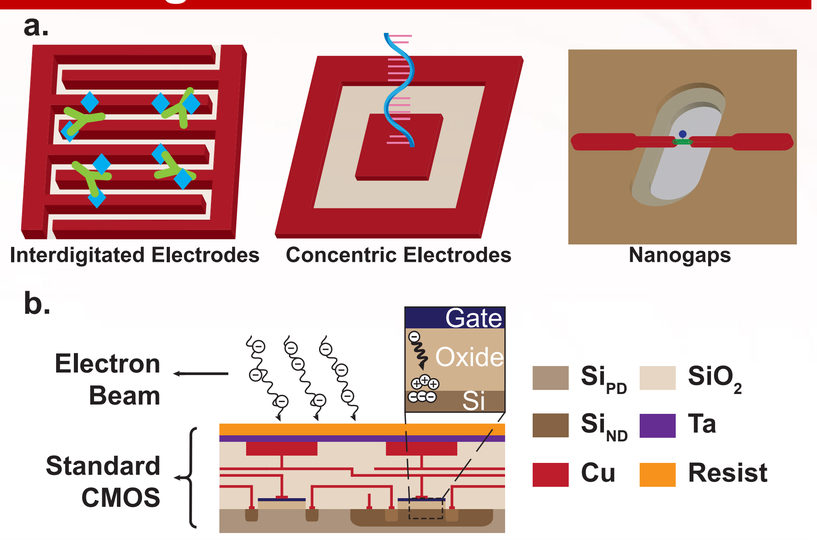
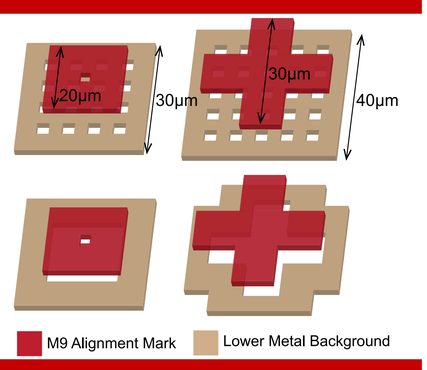
Advantages and Complexities of Sensor-Electronics Co-integration

- Co-integration of CMOS integrated circuits with sensors/transducers has many advantages, *i.e.*, shorter routing, lower parasitics, and improved system sensitivity
- Electron beam lithography (EBL) is a commonly used nano-fabrication technology in low-volume settings – maskless (low-cost) and high-resolution (nm-scale)
- However, high energy e-beam irradiation during EBL can cause transistor degradation, *i.e.*, increased gate leakage, threshold voltage shift, and change of carrier mobility
- While there is currently little in the literature to offer designers guidance, this study aims to quantify these device degradation and investigate the practical considerations of EBL for CMOS post-processing



On-Chip EBL Alignment Mark Construction

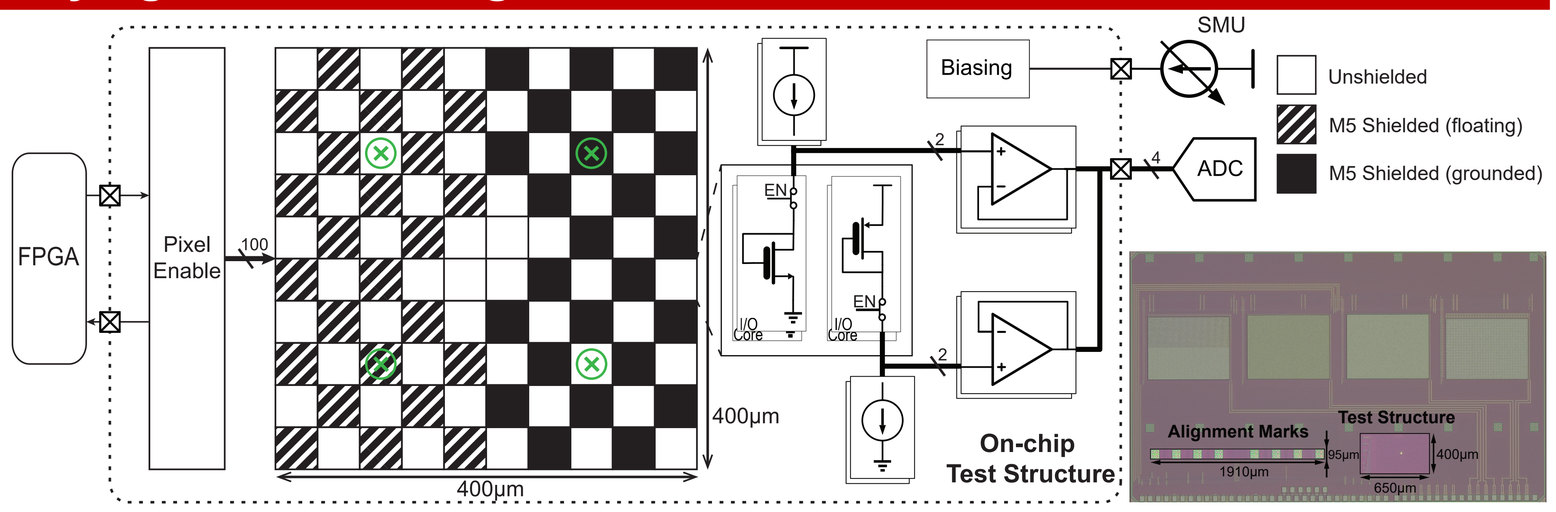
- On-chip alignment marks are needed for precise EBL post-processing; a failure of the auto-alignment leads to incorrect patterning and/or low throughput
- We investigated how to construct alignment marks with various background metals (M1-M8) and shapes (cross vs. square)
- **Key Result:** All variants were experimentally found to be recognized by the EBL tool without significant speed/performance degradation or misalignment



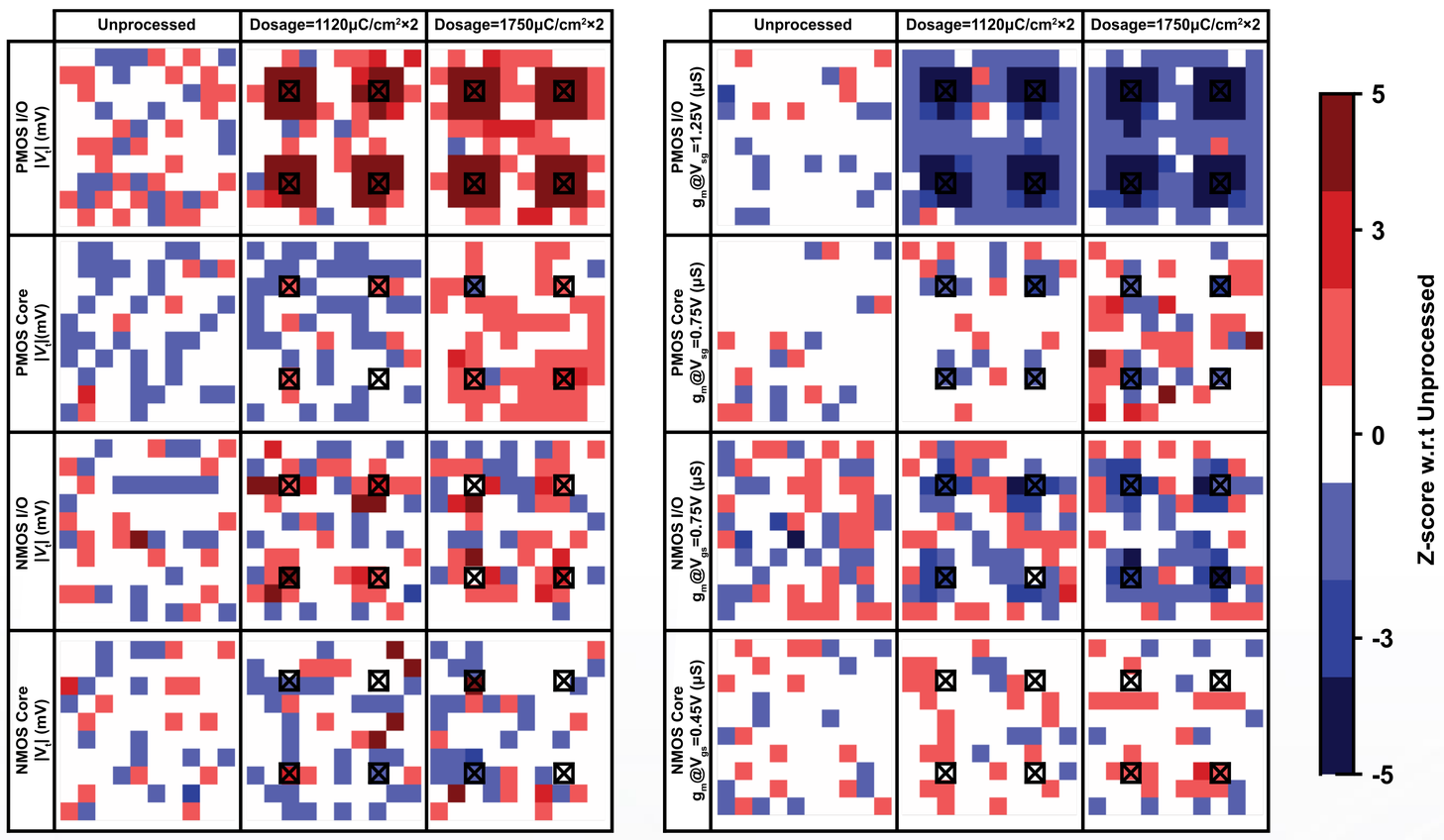
Quantifying Transistor Degradation

10×10 test array of 40×40 µm² pixels in TSMC 65GP:

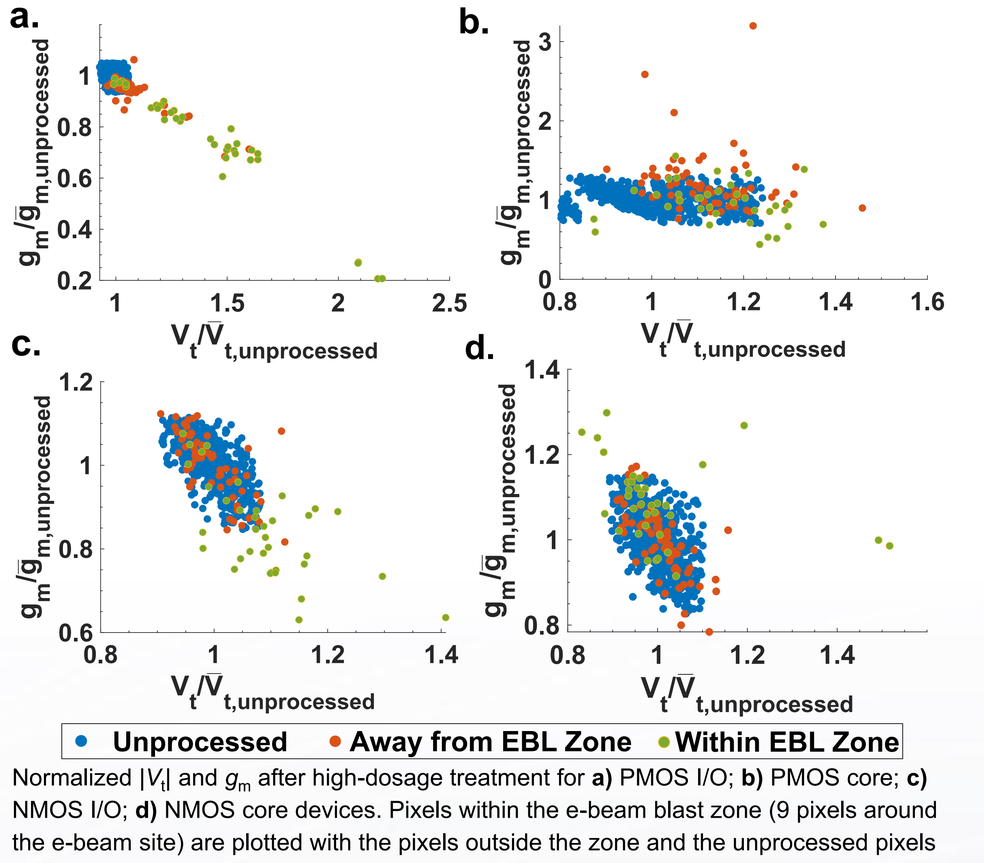
- PMOS thick gate-oxide (I/O), PMOS thin gate-oxide (core), NMOS thick gate-oxide (I/O), NMOS thin gate-oxide (core)
- I/O devices: *W/L* = 400 nm/280 nm, core devices: *W/L* = 370 nm/60 nm
- Checkerboard metal 5 shielding: left-hand side floating, right-hand side grounded



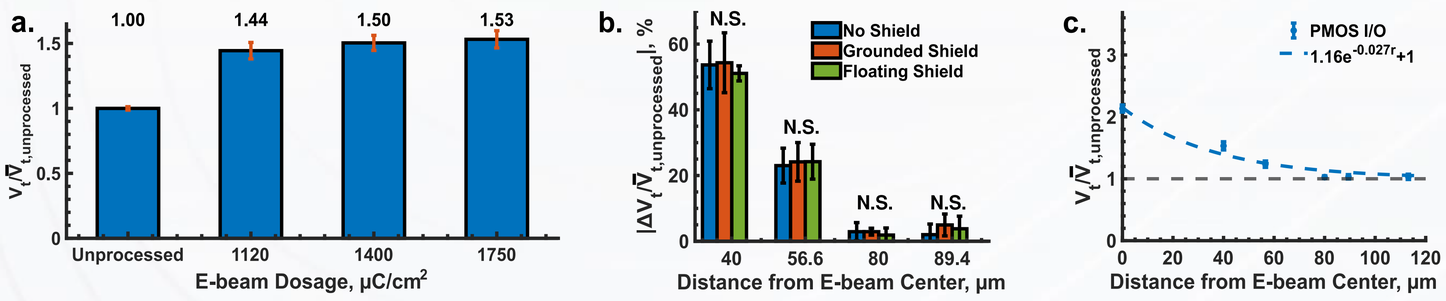
Measurement Results



Measured Z-score of the extracted $|V_t|$ and g_m shifts spatially plotted to correspond to the pixel array, with the four EBL sites marked.



Normalized $|V_t|$ and g_m after high-dosage treatment for **a)** PMOS I/O; **b)** PMOS core; **c)** NMOS I/O; **d)** NMOS core devices. Pixels within the e-beam blast zone (9 pixels around the e-beam site) are plotted with the pixels outside the zone and the unprocessed pixels



a) Normalized V_t of PMOS I/O device at 40 µm from the e-beam center vs. different EBL dosages; **b)** $|\Delta V_t|$ of PMOS I/O device vs. distance from e-beam center after high-dosage treatment for different shields; **c)** Normalized V_t of PMOS I/O device vs. distance from e-beam center after high-dosage treatment.

Key Results:

- Student *t*-test shows that I/O devices are more susceptible to e-beam damage than core devices
- Student *t*-test shows that PMOS are more affected by e-beam irradiation than NMOS devices
- The degraded is proportional to the EBL dosage
- No statistical differences were found between shielded and unshielded devices, regardless of floating vs. grounding (p<0.05)
- An exponential decay of device degradation with respect to distance from the EBL site; devices more than 60 µm away were unaffected by EBL

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