MONOLITHIC FABRICATION OF NANO GAP ELECTRODES FOR SINGLE-MOLECULE BIOSENSING

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ABSTRACT

This work reports a detailed fabrication process of the first CMOS-integrated nano-gap Ruthenium (Ru) electrode molecular biosensor. Ru electrodes are realized monolithically atop a standard 0.18 µm CMOS technology and patterned with a ~20 nm gap. The process integration is compatible with a wide range of electrode materials such as Pt, Tin, ITO, etc. The biosensor chip provides direct, real-time observation of the single-molecule interaction kinetics, unlike classical biosensors that measure ensemble averages of such events. This molecular electronics chip provides a platform for putting molecular biosensing "on-chip" to bring the power of semiconductor chips to diverse applications in biological research.

KEYWORDS

Molecular biosensor, Ru electrode, Single molecule biosensing, Monolithic CMOS integration process.

SINGLE MOLECULE BIOSENSOR

A common problem in biosensing is detecting a specific target biomolecule. Standard methods to identify target molecules are based on their physical properties [1]–[3]. However, these approaches cannot easily identify specific, complex biomolecules such as proteins, DNA segments, and diverse biochemicals. As shown in Fig. 1, the primary sensor element is a 25 nm long molecular wire connected to nanoelectrodes. which feeds into a current monitoring circuit, thus requiring the gap between the electrodes.

The molecular wire contains a central conjugation site for the selective coupling of various probe molecules (*e.g.*, DNA, proteins, enzymes, or antibodies). The current through the molecular wire under a dc applied voltage is monitored with millisecond temporal resolution. The detected signal is picoampere current pulses generated by molecular interaction. Implemented in a 0.18µm CMOS technology, 16k pixel circuits are arrayed with a 20 µm pitch and read out at a 1 kHz frame rate [4,5]. The resulting biosensor chip provides direct, real-time observation of the single-molecule interaction events.

FABRICATION

The precision-engineered molecular wires, such as dsDNA or the present helical peptides, are by design at the nanometer scale (<30 nm), thus requiring the gap between the electrodes to be smaller than what is possible in standard CMOS back end of the line (BEOL) metallization. Furthermore, the electrodes must be electrochemically stable in ionic solutions, precluding the use of standard

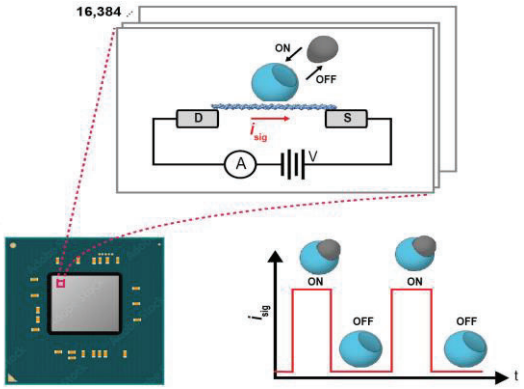

Fig. 1. Overview of a highly multiplexed, scalable CMOS-based molecular biosensor for single-molecule sensors.

metals like copper and aluminum. After a detailed material compatibility study, ruthenium (Ru) was chosen due to its foundry compatibility, robustness, and electrochemical performance. Two approaches were developed to pattern the nanoelectrodes, electron-beam lithography (EBL) (ideal for agile R&D) and conventional photolithography (ideal for mass production at CMOS foundries).

The ASIC chip was fabricated in a 180 nm CMOS process [5]. Wafers were post-processed in a CMOS-compatible facility to fabricate nanoelectrodes. After introducing the incoming CMOS wafers in a 200 mm foundry, a thick oxide is deposited, and wafers are planarized by CMP. Tungsten vias are realized on the planarized surface to establish contact between the post-processed Ru electrodes and underlying CMOS circuits. The sensing electrode stack consists of 20 nm Ru and 2 nm of Cr as a liner to ensure proper adhesion for the subsequent processing steps. To realize the nano-gap, both EBL and photolithography techniques are tested. For the EBL approach, the nanoelectrodes are realized by spin coating 30 nm resist and patterning using a wafer-scale E-Beam tool.

It is important to have a photolithography process for producing nanoelectrodes that is fully foundry compatible and capable of producing nanoelectrodes at scale. A gap-narrowing technique along with 193 nm deep-ultraviolet (DUV) patterning is employed, that leverages the tool capability to achieve the required feature size. First, a 50 nm SiO_2 hard mask is deposited on the electrode stack and a light-field exposure is used for the hard mask etch. This process also helps to realize the arms of the electrode assembly. To generate the gap between the electrodes, a darkfield exposure was done perpendicular to the hard mask print. DUV lithography was used to print 120 nm

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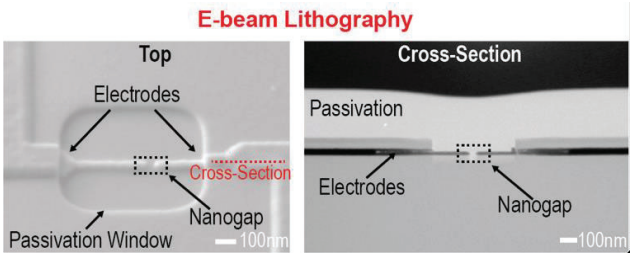
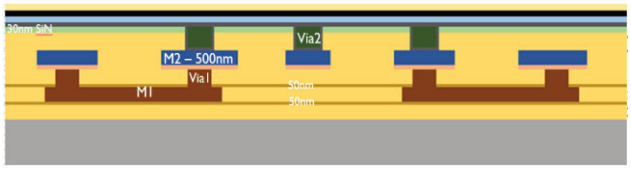
features. A proprietary etch chemistry results in a tapered etch profile and achieves a final distance of 50 nm between the bottoms of the SiO_2 mandrels. To further reduce the electrode gap size, spacer patterning is employed. Highly conformal SiO_2 is deposited via PEALD atop the SiO_2 mandrels, as shown in Fig. 2(b). After exposure, the electrode layers are etched using wafer-scale Ion Beam Etching. This results in electrodes with less than 20 nm gaps.

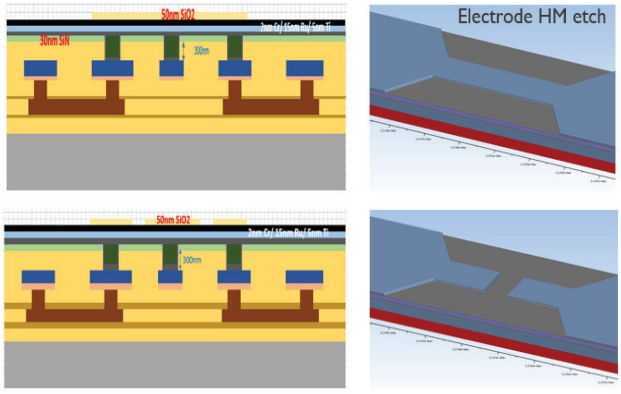
After the electrode processing, the wafers are coated with oxide layers to passivate the electrode sidewall and seal it from the fluidic sample. Next, the Bond pad (BP) module is processed. The planarization and passivation dielectric stack are etched to open the BP aluminum layer coming from the incoming CMOS wafer. The cavity to open the electrodes has been realized as the last module. As a design of experiment, different shapes, sizes, and depths of cavities were fabricated to optimize the wetting efficiency of the electrodes. Fig. 2(c) shows scanning electron microscope (SEM) images of the resulting nanoelectrodes. The top SEM image shows the via connectivity of the electrode to CMOS and confirms the passivation. The top-down critical dimension (CD) SEM shows the gap between the electrodes post-IBE etch.

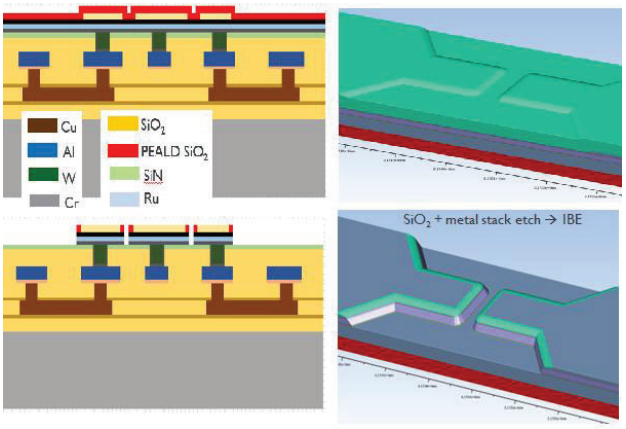


(a)

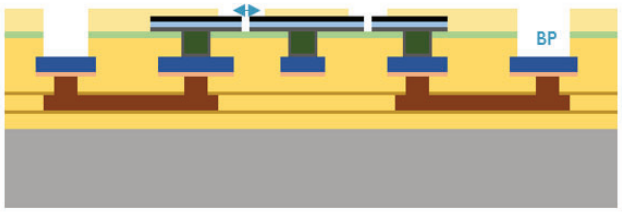


Planarized CMOS wafer with via and Electrode deposition



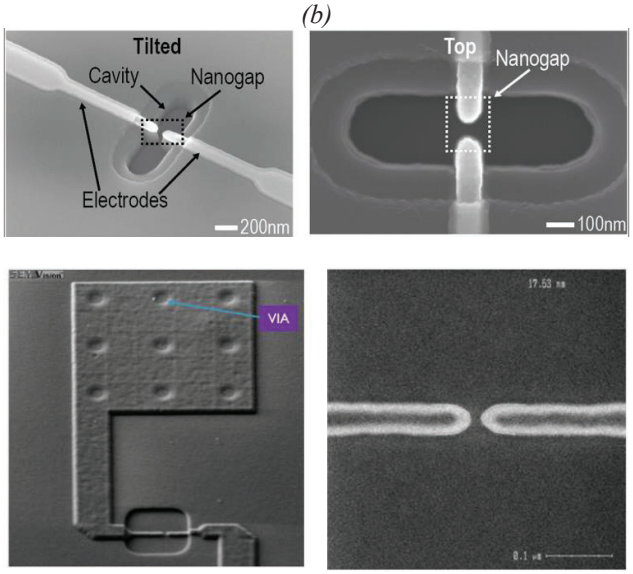


Electrode fabrication: gap narrowing.



Schematic of the Integrated final device

(b)



(c)

Fig. 2. (a) SEM images of nanoelectrodes fabricated via E-Beam lithography. (b) Fabrication steps of CMOS integrated nanogap electrodes. (c) SEM images of the fabricated nanoelectrodes.

CHARACTERIZATION

To characterize the integrity of the fabricated electrodes, the bridge molecules must be loaded into the circuit for use as a sensor. Delivery by passive diffusion alone can require over 24 hours, even at a high concentration. Instead, the much faster process of active dielectrophoretic trapping is employed by applying an ac voltage to the electrodes for 10-second intervals, as shown in Fig. 3 [5]. The "boot up" phase consists of up to 10 rounds of such active bridging, applying a 1.6 V_{pp} sinusoid at 100 kHz. During the bridging phase, the buffer is a low ionic strength solution to prevent Debye screening. After each dielectrophoretic trapping

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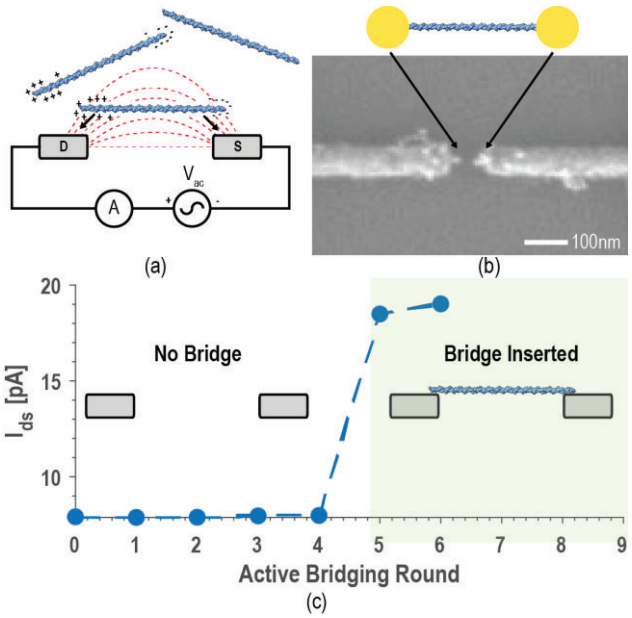

Fig. 3. (a) Dielectrophoretic trapping concept, (b) SEM image of dsDNA with gold beads, and (c) measured current after successive active bridging rounds, resulting in bridging.

round, the array is read out to determine if a bridge was incorporated, as observed by an increase in the pixel current. A pixel is marked as bridged if two successive measurements show an elevated current, and trapping is stopped to prevent additional bridging. An SEM image of a single "dumbbell" bridge (made observable by the addition of two 10 nm diameter gold beads capping a 25 nm dsDNA molecular wire) spanning the electrode gap is shown in Fig. 3(b). In theory, multiple bridges could bind to a sensor. This is controlled by limiting the number of DEP rounds and observing the sensors after each bridging round.

Orthogonal (non-electrical) verification of a single bridge molecule in the circuit is challenging due to their nanometer dimensions and low contrast. Platinum nanoparticles (d = 30 nm) can be trapped in the gap and easily imaged with SEM, as shown in Fig. 4(a); however, similar direct imaging of peptide or dsDNA bridges is impossible. Instead, one must either label the bridge with metal nanoparticles for SEM imaging or measure the nm changes in z-height with atomic force microscopy (AFM). Fig. 4(b) shows an AFM image of a nanoelectrode with a single bridge molecule. This process is slow and limited in the scanning area and is therefore only used for proof-of-concept verification rather than for routine systematic assessments.

CONCLUSION

This work reported the fabrication process steps of Monolithically integrated nano-gap electrodes. Finally, we demonstrated bead trapping experiments to qualify the electrode integrity and CMOS connectivity.

ACKNOWLEDGEMENTS

The authors would like to acknowledge the contributions of past and present employees of IMEC, whose collective efforts made this work possible. We thank Prof. Yoshio Mita from The University of Tokyo for guiding us in setting up the e-beam litho conditions.

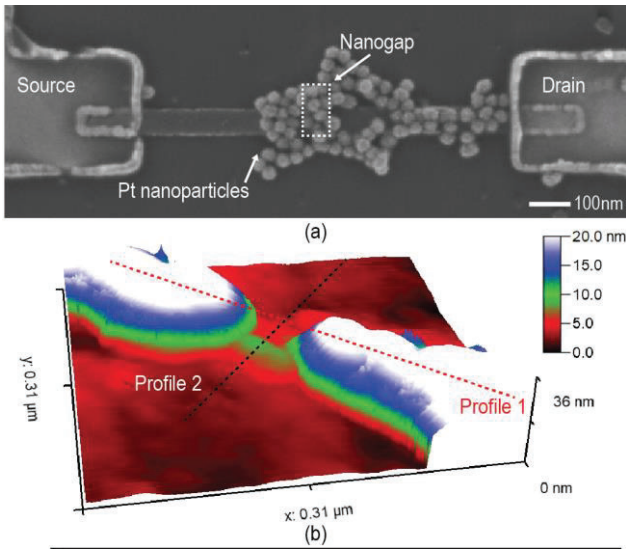

Fig. 4. (a) SEM images of platinum nanoparticles trapped between electrodes, (b) 3D AFM image of a bridge between electrodes,

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