Integrated Circuits for Wireless Communications: Research Activities at the University of California, San Diego

Peter Asbeck, Dinesh Bharadia, Ian Galton, Drew Hall, Hanh-Phuc Le, Patrick Mercier, and Gabriel Rebeiz

The continuing demand for improved wireless connectivity and enhanced data rates has spurred worldwide research in microwave and millimeter (mm)-wave circuits and systems within academia, government, and industrial centers. At the University of California, San Diego (UCSD), the Center for Wireless Communications (CWC) was established more than two decades ago and has contributed to analog, microwave, and millimeter circuits and systems research; communication and information theory; coding; and application studies for 4G, 5G, and 6G wireless systems. This article highlights recent UCSD research efforts, emphasizing the microwave and mm-wave circuits and systems and accompanying analog circuit techniques, carried out in conjunction with the CWC.

Multiple companies from around the world have sponsored UCSD research, and additional research has been funded through numerous U.S. government awards. The closeness between the wireless industry

Peter Asbeck (asbeck@ece.ucsd.edu), Dinesh Bharadia (dineshb@eng.ucsd.edu), Ian Galton (galton@eng.ucsd.edu), Drew Hall (dahall@eng.ucsd.edu), Hanh-Phuc Le (hanhphuc@eng.ucsd.edu), Patrick Mercier (pmercier@eng.ucsd.edu), and Gabriel Rebeiz (rebeiz@ece.ucsd.edu) are with the Department of Electrical and Computer Engineering, University of California, San Diego, La Jolla, CA 92093 USA.

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firms and the university has been particularly valuable in focusing the research on themes important for applications. Graduates of the program have also had a major influence on wireless industry activities, particularly in California.

This article first covers research results in mm-wave circuits and assemblies for antenna array transmitters and receivers for 5G and beyond, followed by a discussion of low-power microwave circuits for Internet of Things (IoT) applications, mixed-signal circuits for translating the relevant signals between microwave and digital domains, and a novel system methodology for interfacing with low-power wireless nodes via Wi-Fi.

mm-Wave Antenna Array Transmitters and Receivers

A cornerstone of wireless communication systems at high frequencies is the use of antenna arrays to direct the transmitted power toward the desired receiver (or multiple receivers) in appropriate narrow beams. As the number of elements in the array increases, the beamwidth decreases, enabling efficient focusing of the output power on the desired receivers. For large arrays, it is a significant challenge to provision appropriately phased and amplitude-controlled signals to the different array elements, which are typically spaced at distances of half the free space wavelength of the carrier frequency. Prof. Gabriel Rebeiz's group has been pioneering the development of affordable satellite communications (SATCOM) and 5G phased arrays based on silicon technologies since 2005 [1], [2], [3], [4], [5], [6], [7], [8, and references therein]. At present, these systems can integrate the entire phased array on a single low-cost printed circuit board that includes the antennas, silicon beamformer chips, and the necessary control electronics. The board can be assembled using automated high-volume manufacturing techniques, making it very low cost in large numbers, and is also calibrated using built-in tests and also fast far-field pattern measurements. UCSD and Rebeiz's group pioneered this approach for phased arrays and developed the first silicon phased array chips (called beamformer chips) based on the 2 × 2 quad approach and the first single-printed circuit board (PCB) phased arrays. This has lowered the cost of phased arrays by a factor of 50–100×, making them affordable for commercial use in SATCOM and mm-wave 5G. A representative example is shown in Figure 1, a 1,024-element receiver array

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covering the K-band (17.7–20.2 GHz) for SATCOM [7]. A single PCB of 25 cm × 22 cm is used, making it the largest single-PCB K-band array to date. The narrow 3.5° beamwidth with ±70° scan angles enables tracking satellites in low Earth orbit, an emerging area for broadband connectivity.

The same ideas and techniques have been used by companies such as SpaceX/Starlink for their SATCOM terminals (known as "Dishy"), Collins Aerospace, Viasat, Boeing, and others for their airborne phased array terminals on commercial and defense aircraft and Qualcomm, Nokia, Samsung, Ericsson, and several other companies for their low-cost 5G phased arrays at 28 GHz and 39 GHz. It is no exaggeration that every affordable phased array built today follows the silicon beamformers and single-PCB design approach developed at UCSD.

Prof. Rebeiz continues developing wideband phased arrays for X-/Ku-/Ka-band SATCOM, 18- to 50-GHz wideband 5G systems, and 140-GHz 6G phased arrays. His group has also developed large wafer-scale phased arrays for mm-wave applications and proven them at 60 GHz, 110 GHz, and 140 GHz. For example, for potential applications in 6G, an eight-channel transmit array and an accompanying eight-channel receive array were demonstrated using Si CMOS-silicon on insulator (SOI) technology, shown in Figure 2 [6], [8]. Antennas were directly mounted on top of the Si ICs, using metal

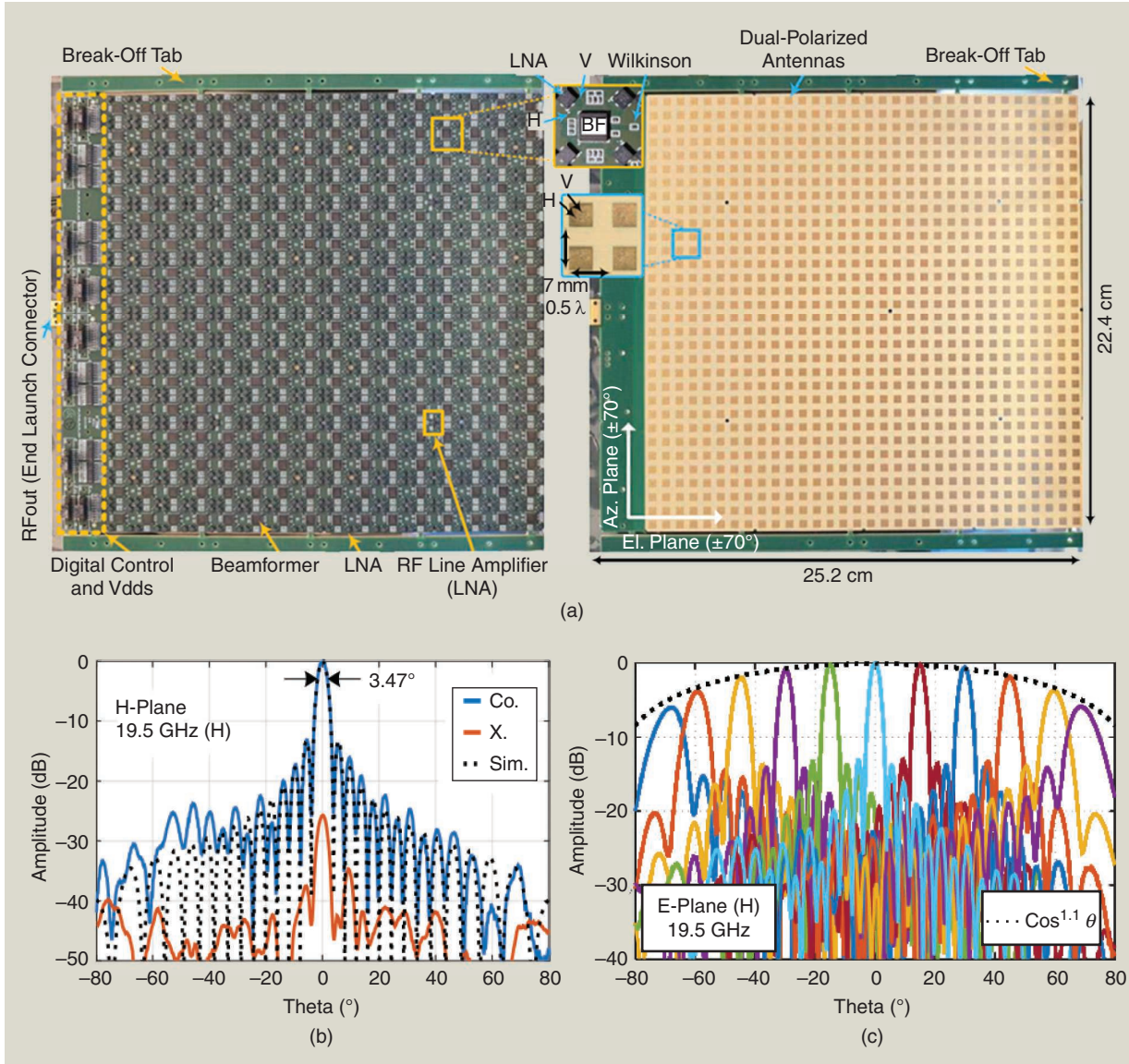

Figure 1. *The 1,024 dual-polarized phased array for K-band SATCOM. (a) A PCB photograph illustrating electronic side and patch antenna side. (b) The output pattern for broadside emission showing 3.5° beamwidth, cross-polarization, and simulation. (c) The antenna patterns covering scan angles of ±80°.*

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patterns on a quartz plate; the tight integration was made possible by the small 1-mm distance between antennas. Local oscillator (LO) routing around the chip was done at a subharmonic, and upconversion to 140 GHz was carried out at each channel, as shown in Figure 3. Prof. Rebeiz and his former students founded Extreme Waves, a company in San Diego developing and delivering phased arrays for SATCOM, 5G, and specialized functions.

In addition to phased arrays, the Rebeiz group has demonstrated a variety of key building block circuits for high-frequency systems, including power amplifiers (PAs) (as detailed in the section below), LNAs, phase shifters, filters, and voltage-controlled oscillators. Another ground-breaking circuit for instrumentation and optical communication applications is a distributed amplifier with over 100 GHz bandwidth, 33 dB gain, and peak output power of 23 dBm, shown in Figure 4 [9].

Microwave and mm-Wave PAs

The overall range and efficiency of wireless transmitters are typically determined by the PA; accordingly, PAs have been the topic of intensive research. For mm-wave communications (notably 5G), the use of antenna arrays and the resultant spatial power combining has meant that peak output power in the neighborhood of 20 dBm is adequate to provision a given antenna, and this is in the realm of what be achieved with Si technology. Bulk CMOS, CMOS-SOI, and SiGe HBT are all candidates for use in both handsets and base stations, along with GaN PAs for very high power transmitters. Efficiency is a central concern, which is exacerbated by the fact that amplifiers must operate in backoff due to the high peak-to-average power ratio for the signals, typically 8–9 dB. Linearity requirements provide an additional challenge: while at microwave frequencies, digital predistortion is typically used to mitigate PA nonlinearity; for the mm-wave antenna arrays with large numbers of individual PAs and wide bandwidth requirements (200 to 1,000 MHz), the PA intrinsic linearity must be sufficient to amplify signals with error vector magnitude down to 3–5%.

A primary focus of 5G and 6G PA research at UCSD has been CMOS-SOI, which provides a variety of advantages. Excellent isolation between devices facilitates series-connecting FETs (“stacking”) to enhance

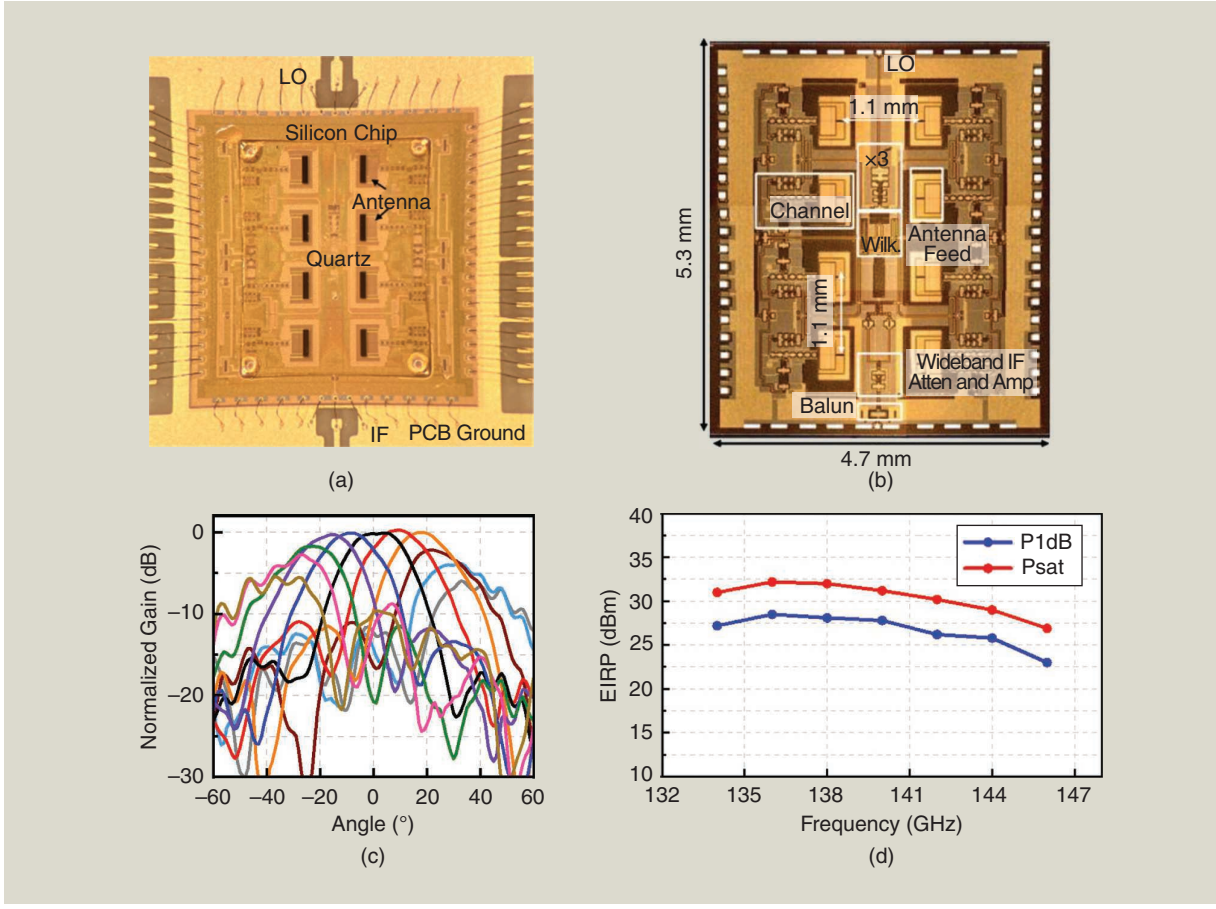

Figure 2. *The 140-GHz CMOS eight-channel transceiver ICs with antennas on quartz “superstrate”: chip photos of (a) transmitter and (b) receiver and (c) and (d) measured transmitter performances. EIRP: equivalent isotropically radiated power.*

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their voltage-handling capability. The buried oxide decreases the parasitic capacitance to the substrate. In the GlobalFoundries 45-nm CMOS-SOI technology, high-resistivity (>1,000 ohm-cm) Si substrates are used, virtually eliminating capacitance of interconnect lines to the substrate. High figures of merit ft and fmax in the vicinity of 300–400 GHz are also obtainable.

In conjunction with the 6G-oriented transceiver at 140 GHz described previously, Prof. Rebeiz's group demonstrated a ground-breaking Si 45-nm CMOS-SOI PA for use at 130–150GHz, showing the potential of Si-only technology for practical use in wireless transmitters above 100 GHz [10]. As shown in Figure 5, the four-stage PA achieves a saturated output power of 17.5 dBm and an efficiency of 13% at 140 GHz.

One target of UCSD's research for mm-wave 5G (24–40 GHz) has been demonstrating high power and efficiency. With the use of pMOS rather than nMOS, in Asbeck's group, power-added efficiency (PAE) up to 50% and output power up to 22 dBm have been demonstrated in a simple two-stack differential amplifier [11], as shown in Figure 6. The use of pMOS enables

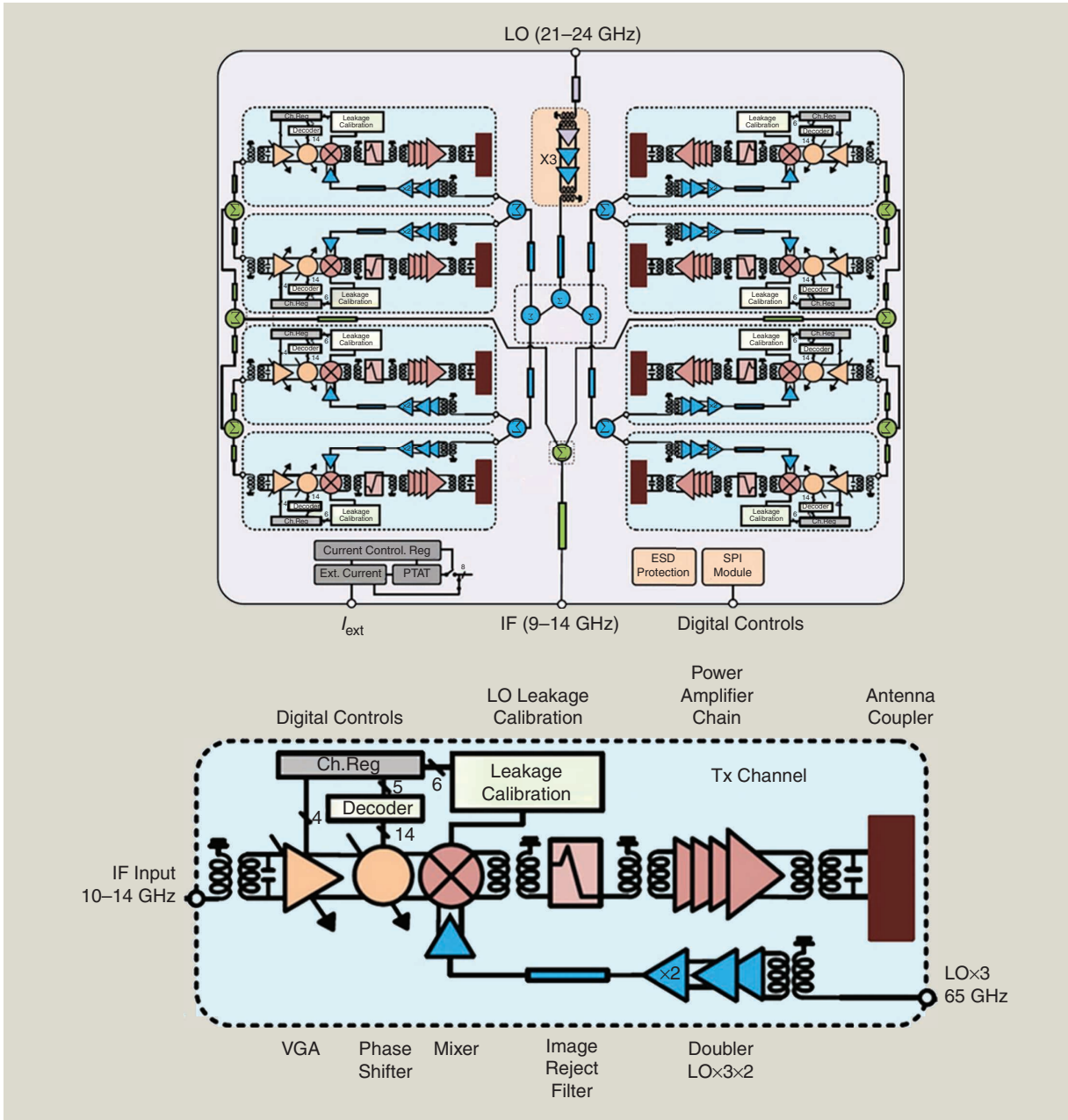

Figure 3. *The anatomy of a 140-GHz phased array transmitter IC. To avoid the necessity of routing 140-GHz signals all around the 5.4 × 5.1 mm^2 chip, a lower-frequency LO is fed in and multiplied ×6 prior to mixing with the IF. Beamforming is done at IF. An image reject filter is used in each channel. VGA: variable gain amplifier.*

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increasing the power supply voltage without sacrificing reliability, because of superior resistance to hot carrier injection and increased ability to handle high voltage when the device is off (in class B or deep class AB operation). The PA uses only a positive supply (connected to the source) to maintain compatibility with conventional nMOS circuits.

Another target of research has been to provide high efficiency in backoff. Doherty amplifiers have been implemented in nMOS-SOI and pMOS-SOI, using low-loss output impedance matching and power combining designed using the Ozen technique [12], [13], [14]. Figure 7 illustrates the circuit diagram for a pMOS Doherty, which achieves 20% PAE at 8 dB backoff from the saturated output power of 23.5 dBm at 27 GHz. It is notoriously difficult to maintain good linearity in a Doherty PA; digital predistortion is almost always used in the microwave frequency range. Here good linearity is achieved with multiple active bias networks that detect the transmitted power on the chip with FET-based rectifiers and adjust the gain by controlling gate biases accordingly. In high-frequency Doherty amplifiers, this is particularly valuable to facilitate a transition for the peaking amplifier from deep class C to class AB as the input power increases, without sacrificing gain. The active bias networks are also used to mitigate soft saturation effects in amplifier AM–AM characteristics.

Improved efficiency at backoff can also be achieved using envelope tracking (ET). This technique, based on the use of a dynamically varied power supply voltage, has been the subject of extensive past development at UCSD for base station and handset applications at 1–2 GHz [15], [16] and is now in use in many smartphones. ET research is continuing with a primary focus on base station applications for 4G and 5G in sub-6-GHz bands. One novel theme being explored by Prof. Hanh-Phuc Le's research group is based on a multiple switched capacitor network [17], [18] to supply a menu of fixed supply voltages to a GaN base station 5G-NR PA, allowing it to select the most efficient voltage on a symbol-by-symbol basis [19]. Another recent result is a tour-de-force ET amplifier system achieved by collaborative industry–CWC research (led by Mitsubishi Electric and Nokia/Bell Labs). A 3.6- to 4.0-GHz ET

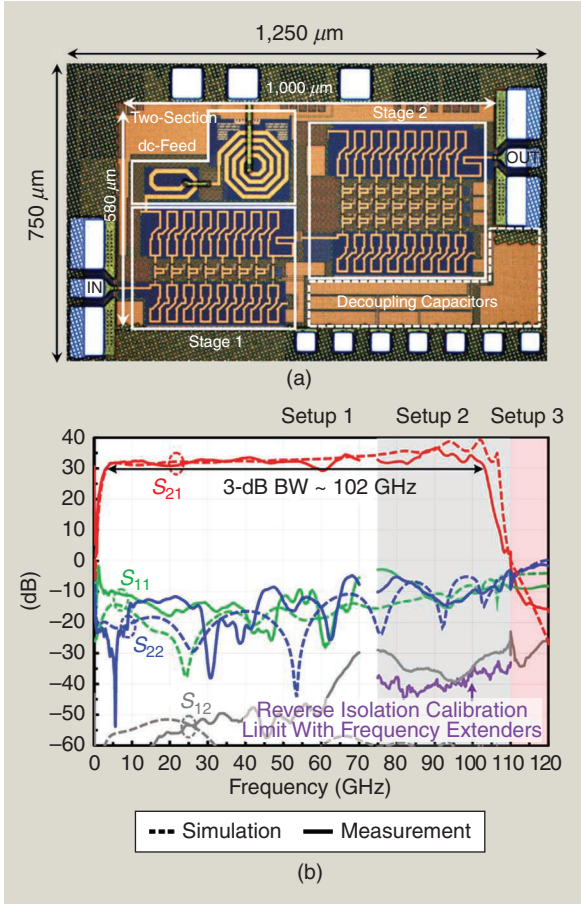

Figure 4. *The broadband high-power distributed amplifier in 45-nm CMOS-SOI: chip layout and measured characteristics.*

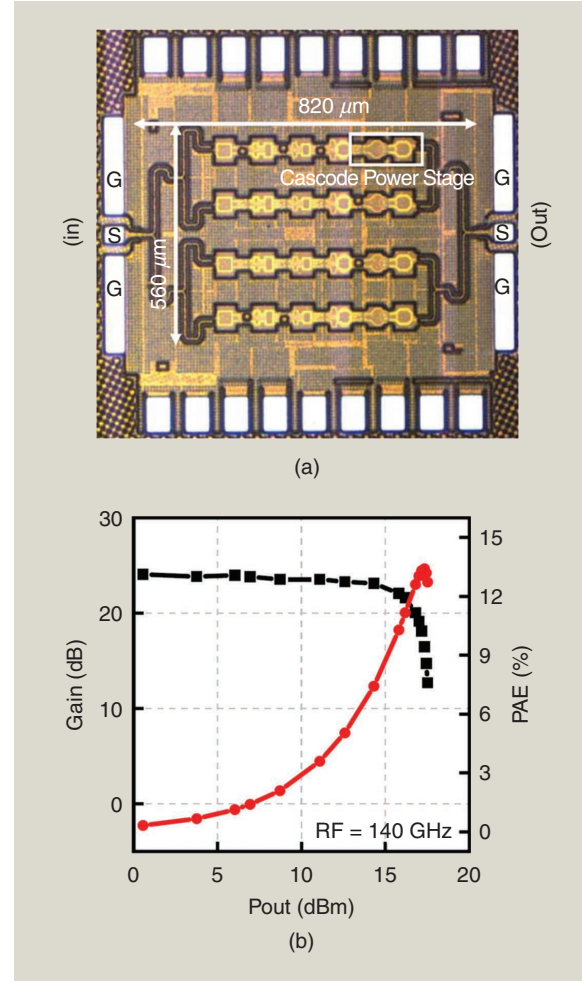

Figure 5. *The 140-GHz CMOS PA: chip photograph and performance characteristics. PAE: power-added efficiency.*

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amplifier was demonstrated using a GaN soft-switching buck converter feeding a GaN 0.15-μm HEMT PA, in conjunction with a digital front-end environment for signal generation and predistortion [20]. ACLR was below −45 dBc, and total efficiency reached 47% at 3.6 GHz, as shown in Figure 8.

IoT: Wake-Up Receivers

Most IoT devices require RF ICs to communicate information among each other and/or with local infrastructure. Many of these devices use wireless standards such as Bluetooth Low Energy, Wi-Fi, Zigbee, LoRa, NB-IoT, etc.; however, these standards were designed to support high throughput, from tens of kbps to tens of Mb/s. As such, the power consumption of these devices is commensurately high, or they lower power by turning off the radios for extended periods, lengthening the latency of connecting the device to the network. However, many emerging IoT applications do not require high average throughput: consider, for example, applications in perimeter detection or infrastructure monitoring, where communication is not needed until relatively infrequent events occur. Unfortunately, most radio standards require frequent packet communication for network synchronization purposes, even if there are no data to transmit. This stay-on-to-communicate approach can reduce battery life significantly [21], [22].

Wake-up receivers (WuRXs) provide an elegant solution by continuously monitoring the RF spectrum for prespecified event signatures (i.e., wake-up messages) that tell the WuRX to

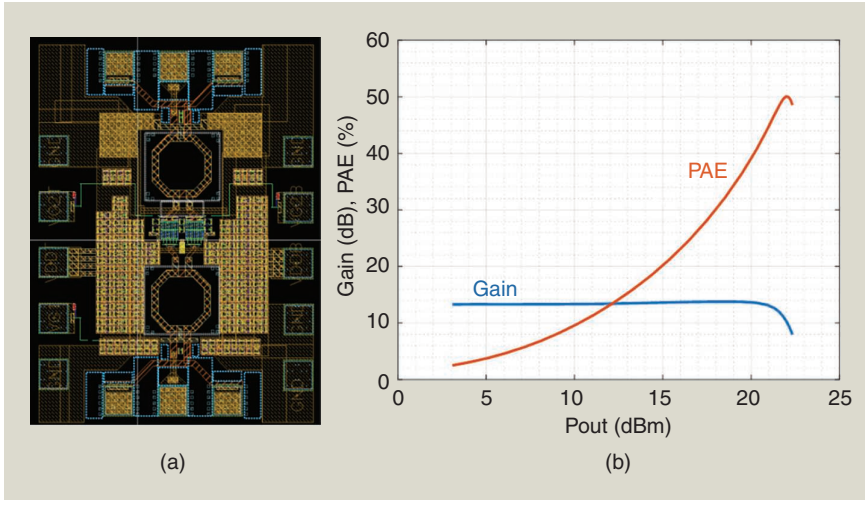

Figure 6. *(a) The layout of differential pMOS-SOI Ka-band amplifier using positive supply voltage. (b) The measured gain and PAE at 25 GHz versus output power.*

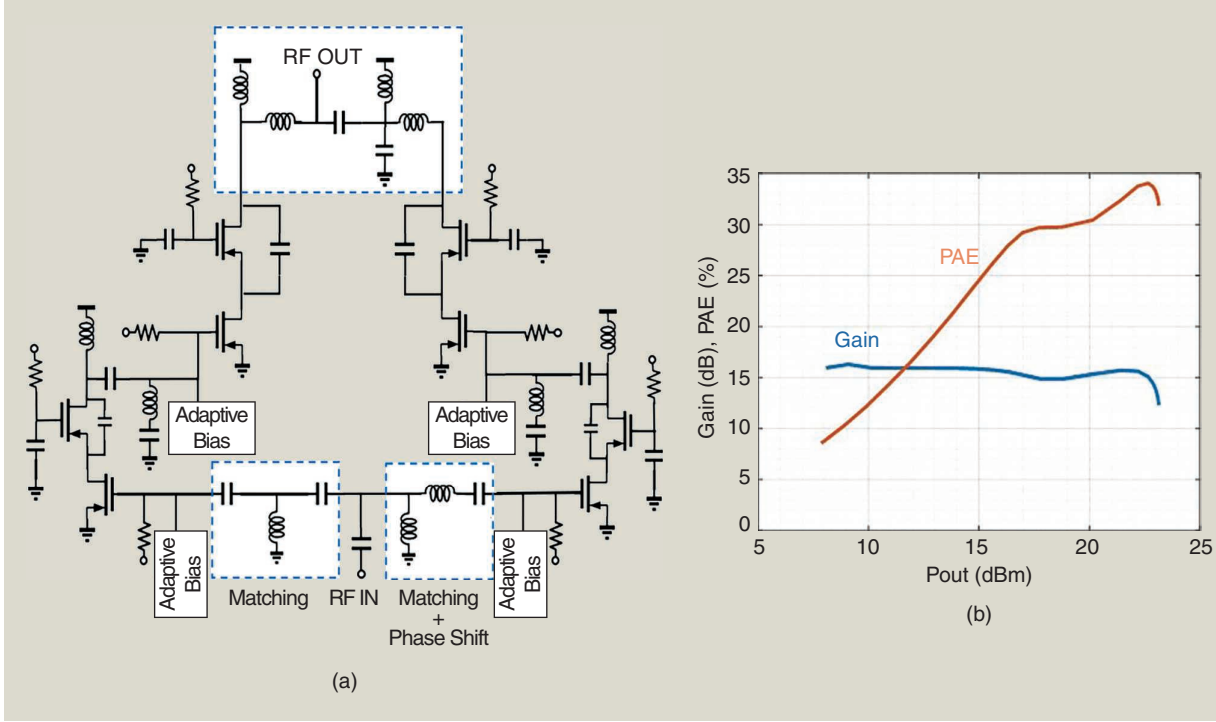

Figure 7. *(a) The circuit diagram of a Doherty amplifier implemented with pMOS-SOI. (b) The measured gain and PAE at 27 GHz versus output power.*

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enable the device to take further action, such as turning on the main radio. If a wakeup event is detected, the normal main radio can provide high-throughput communication without requiring frequent synchronization packet communication. The WuRX provides energy savings if its average power consumption is lower than the power of the main radio at the target latency for device response to a query over the network. For many standards-based radios, the target latency is imposed by the standard or by an application-dependent communication latency constraint. If the active WuRX power consumption is low, the energy savings can be substantial.

With support from the Defense Advanced Research Projects Agency, researchers in the groups of Prof. Drew Hall, Patrick Mercier, and Gabriel Rebeiz developed several WuRXs with nanowatt-level power consumption, less than the leakage power of a coin cell battery. The first radio demonstrated a 113.5-MHz OOK-modulated WuRX that achieved −69 dBm sensitivity with only 4.5 nW, as shown in Figure 9(a) [22], [23], [24].

This work aggressively reduced the power by 1) reducing the baseband signal bandwidth to 300 Hz, suitable for many event-driven applications, to aggressively filter noise; 2) employing a high-Q transformer/filter that passively amplifies the voltage of the incoming RF waveform by 25 dB and filters adjacent channel noise and interferers; 3) simultaneously demodulating and amplifying the wake-up signal via a high-impedance dynamic threshold MOS envelope detector (ED) with subthreshold active-inductor biasing; 4) digitizing the ED output via a regenerative comparator with kickback elimination; 5) generating the baseband clock via a 0.9 pJ/cycle, 1.1 nW relaxation oscillator [25]; 6) decoding the received OOK signal modulated with a custom 16-bit code word using a high-V_t subthreshold digital baseband correlator; and 7) operating all circuits at 0.4 V to minimize static and dynamic power. When published in 2017, this work reduced the power consumption by over 1,000× from the state of the art. Follow-on work demonstrated that this concept works at higher frequencies (e.g., 400 MHz and 9 GHz); as shown in Figure 9(b), it can have sensitivities better than –100 dBm, and it can be made robust against process, voltage, and temperature (PVT) variation [26], [27], [28].

IoT: Low-Power MedRadio

The IoT era is experiencing rapid growth with the deployment of a wide variety of sensor nodes, most notably for healthcare monitoring and industrial automation. An important distinction from classic radios is that such IoT nodes only need to wirelessly communicate over short distances, typically ~1–2 meters, to reach a nearby data aggregator (e.g., smartwatch or smartphone). Owing to their autonomous and unobtrusive

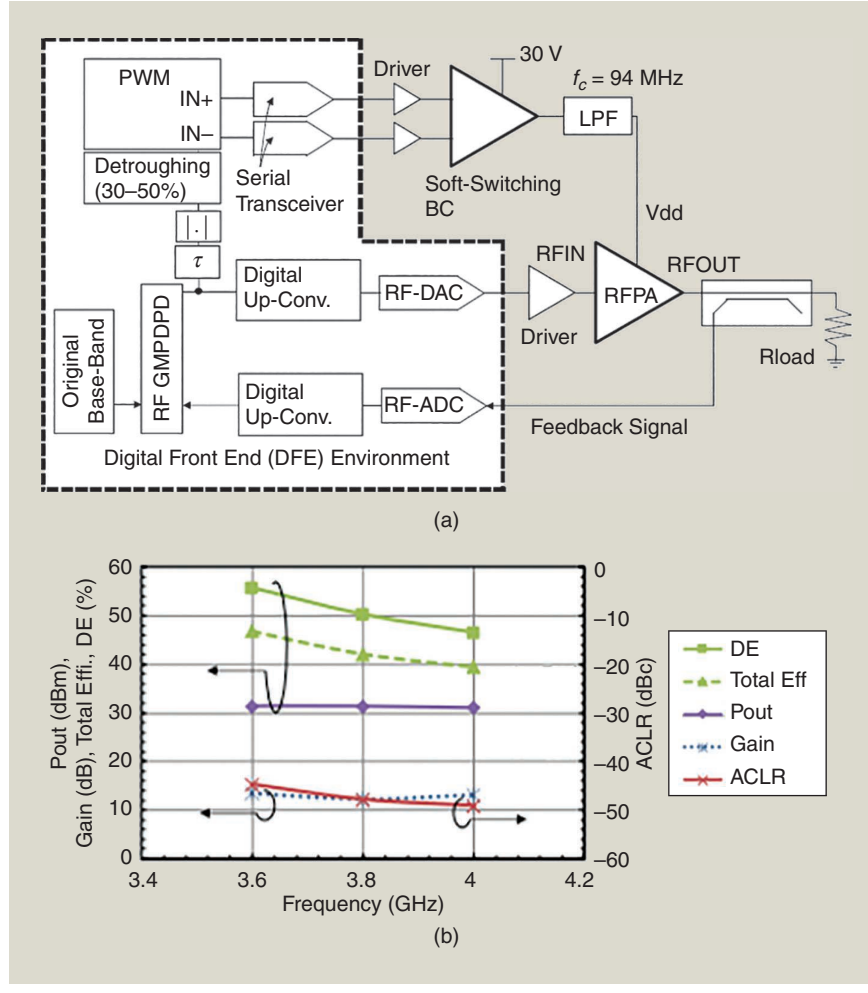

Figure 8. *(a) The ET system comprising a GaN soft-switching buck converter, GaN RF PA, and digital front-end environment. (b) The experimental results (Mitsubishi Electric, Nokia/Bell Labs, and UCSD). PWM: pulse width modulation; DE: drain efficiency; LPF: low-pass filter; BC: buck converter; GMPDPD: generalized memory polynomial digital predistortion.*

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nature, enabling high deployment lifetimes through ultralow-power (ULP) operation is critical and often achieved through aggressive duty cycling.

Simplistic transmitter topologies are preferred for this application. In contrast to conventional radios, the PA in a short-range radio is not the highest power-consuming block due to the low output power. Instead, the frequency synthesizer or phase-locked loop (PLL) consumes a significant fraction of the overall transmitter power. The MedRadio/ISM band (~400 MHz) is widely used for the aforementioned applications due to its relatively low carrier frequency and suitability for short distances. To generate this RF carrier in a ULP manner, ring oscillator-based injection-locked clock multipliers with small frequency multiplication factors (~8–12×) are regarded as state of the art [29], [30], [31], [32].

Toward this end, a new technique for PVT-robust, calibration- and regulation-free synthesis of the RF carrier was developed in Prof. Drew Hall's group based on generating poly-phasors at 50 MHz with no power overhead [33]. This is accomplished using a passive polyphase filter directly integrated within a crystal oscillator followed by an 8× edge combiner to synthesize the RF carrier with –109 dBc/Hz phase noise at a 100-kHz offset, as illustrated in Figure 10. A dual-supply, inverse class E PA is implemented for high efficiency at low output power (–17.5 dBm). Open-loop operation permits aggressive duty cycling (<40 ns startup time). This work demonstrated a BPSK, PVT-robust transmitter fabricated in 22 nm fully-depleted SOI technology when operated from a 0.4-/0.2-V supply consuming 67 µW with 27% global efficiency. This radio demonstrates excellent robustness to process variation, consistent performance across –30 to 90 °C, and complete insensitivity to voltage variation. This work achieves the best energy efficiency (67 pJ/bit) and lowest power (67 µW) among reported sub-1 mW narrowband transmitters, significantly advancing the state of the art for low-power, short-range radios.

Mixed Signal Circuits: Phase-Locked Loops

The relentless evolution of wireless transceiver standards toward higher bandwidths, higher-order modulation, and higher receive sensitivities imposes increasingly stringent requirements on local oscillator frequency synthesis in terms of rms jitter, spot phase noise, and spurious content. For example, in the 5G NR wireless standard, error vector magnitude requirements for higher than 64 quadrature amplitude modulation require a LO frequency synthesizer with a total rms integrated jitter less than 90 fs, which is very challenging.

The best-performing present-day PLLs are analog PLLs, i.e., PLLs based on conventional analog circuitry, so analog PLLs are the predominant means of frequency synthesis in high-performance commercial wireless transceivers. Unfortunately, analog PLLs require large-area loop filters, are not inherently reconfigurable, and are not amenable to digital calibration. Yet, reconfigurability is essential as modern wireless standards require handling widely variable data rates, and digital calibration is increasingly necessary to address issues associated with the low supply voltages, high device nonlinearity, poor signal isolation, and device leakage of highly scaled CMOS technology nodes as well as for the cancellation of mutual interference among the multiple on-chip PLLs required for carrier aggregation. In contrast, digital PLLs have very small loop filters, are easily reconfigurable, and are amenable to digital calibration, but they have yet to achieve the phase error performance of their analog counterparts [34, and references therein]. To date, the best-performing published digital PLLs are based on analog sampling or digital bang-bang (BB) architectures. However, both types of PLLs have practical issues. Sampling PLLs suffer from

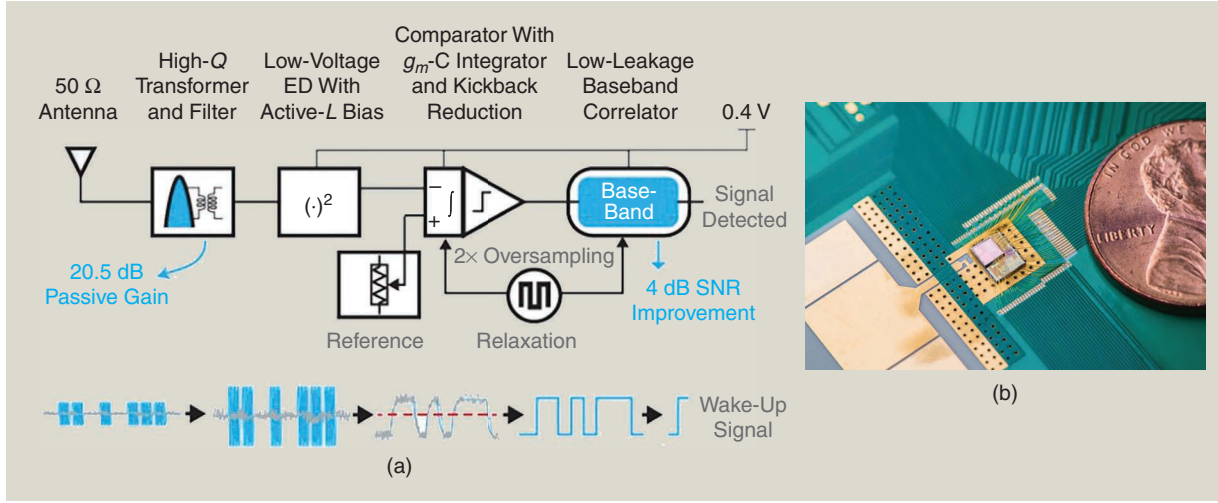

Figure 9. *(a) A block diagram of a WuRX. (b) A photograph of a 9-GHz WuRX assembly.*

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poor reference spur performance and high PVT sensitivity because their loop dynamics are highly dependent on the slope of the sampled waveform around its midscale crossings. BB digital PLLs suffer from locking issues under large frequency steps, loop dynamics that depend on the PLL's noise sources, and require impractically high reference frequencies to sufficiently suppress the quantization error introduced by the BB phase detector. Furthermore, the digitally controlled oscillators (DCOs) required in digital PLLs lead to a serious, but rarely acknowledged, intermittent phase noise degradation phenomenon called spectral breathing.

The ongoing digital PLL research performed by Prof. Ian Galton's group aims to develop new techniques that systematically eliminate the limitations of present-day digital PLLs with the objective of elevating their performance to that of the best present-day analog PLLs while retaining the digital PLL benefits. Research results so far include the development of a robust frequency-to-digital converter-based digital PLL architecture, several phase noise and spurious tone reduction techniques based on time amplification and digital calibration, and a solution to the spectral breathing problem [34], [35], [36], [37], [38], [39]. The group's first-generation 6- to 7-GHz versions of these PLLs, illustrated in Figure 11, achieve 145-fs rms random jitter performance without the abovementioned drawbacks [38], and the next-generation version currently under design is targeting 75-fs rms jitter performance with best-of-class spurious tone performance.

Mixed Signal Circuits: Digital to Analog Converters

The most significant sources of static and dynamic nonlinear error in practical high-speed, high-resolution, continuous-time RF digital to analog converters (DACs) are clock skew, component mismatches, and intersymbol interference (ISI). Most published digital calibration techniques aimed at addressing these issues only reduce the static portion of such error, which leaves dynamic error as a major limitation. Techniques such as return-to-zero signaling can be used to mitigate ISI, but they generally have undesirable side effects, such as halving the signal power and significantly increasing

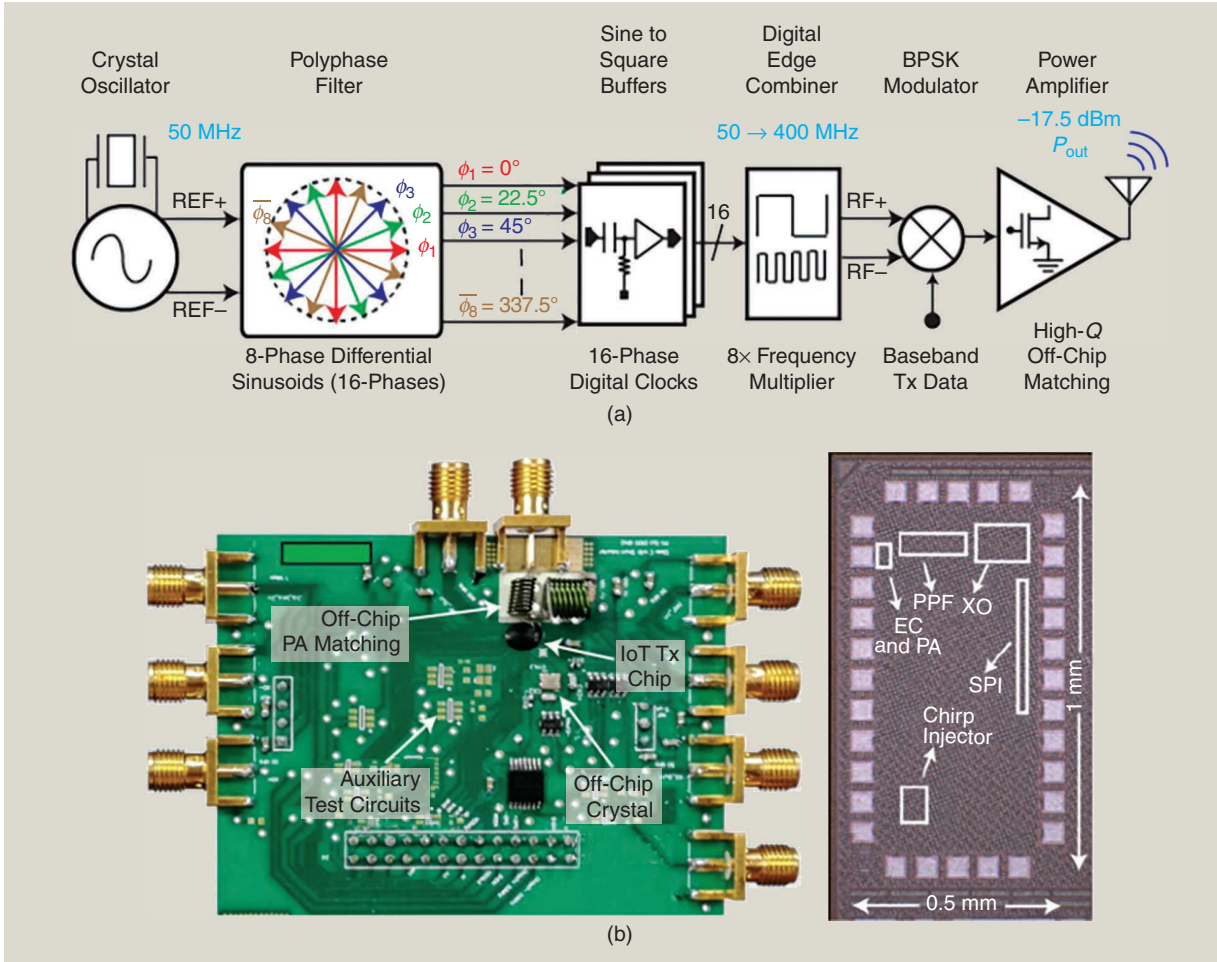

Figure 10. *(a) A block diagram of a ULP transmitter. (b) A photograph of a 400-MHz transmitter PCB and die.*

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sensitivity to clock jitter, which greatly increase power consumption and/or decrease signal-to-noise-and-distortion ratio (SNDR). Consequently, clock skew, component mismatches, and ISI typically limit the Nyquist band SNDR of present-day CMOS RF DACs to less than 65 dB. Nonetheless, RF DACs with Nyquist band SNDRs of well over 65 dB are increasingly necessary for high-performance wireless applications such as 5G cellular base station transmitters. The ongoing DAC research performed by Ian Galton's group at UCSD aims to address this disconnect via digital calibration techniques that adaptively measure and cancel both static and dynamic DAC errors from clock skew, component mismatches, and ISI in real time.

The difficulty that has prevented most published DAC calibration techniques from suppressing dynamic error arises from a property inherent to continuous-time DACs. Such DACs generate a continuous-time output pulse for each input codeword, and the output pulse has a bandwidth that far exceeds the DAC's sample rate because its duration is time limited to one clock period. Therefore, any technique that cancels dynamic error either must do so over a bandwidth much wider than the DAC's signal bandwidth, which is unlikely to be practical given the multi-GHz sample rates required of RF DACs, or must perform frequency selective cancellation over a single Nyquist band. Prof. Galton's group recently developed the first technique to accomplish this that does not require elaborate manual tuning [40]. This mismatch-noise cancellation (MNC) technique cancels static and dynamic errors from clock skew and component mismatches over an RF DAC's first Nyquist band. The initial version of the MNC technique has been used to demonstrate a 600 MS/s DAC IC that achieves a Nyquist band SNDR of 77 dB, as illustrated in Figure 12 [41]. This circuit still has two limitations: it oversamples the DAC output, which limits the sample rate of the DAC IC to 600 MHz, and it does not cancel ISI. The group has since developed a subsampling version of the MNC technique that eliminates the oversampling requirement [42] and a separate technique to address ISI.

Beam-Steering Ambient Wi-Fi and Bluetooth Signals for ULP IoT Devices

Wireless security cameras, wearable devices, pet health tracking systems, wireless earbuds, augmented reality glasses, and more are all starting to take hold in today's marketplace. However, there is a major problem faced by many of these IoT applications: power consumption. Most of these devices are designed to be small and portable, and yet some of these devices consume so much power that they must be plugged into the wall (e.g., wireless security cameras), or the devices must be so small they do not have room for a large battery, and as a result, their battery life is poor (e.g., wireless earbuds). A key culprit for this is the relatively high power consumption of the radio circuits that enable

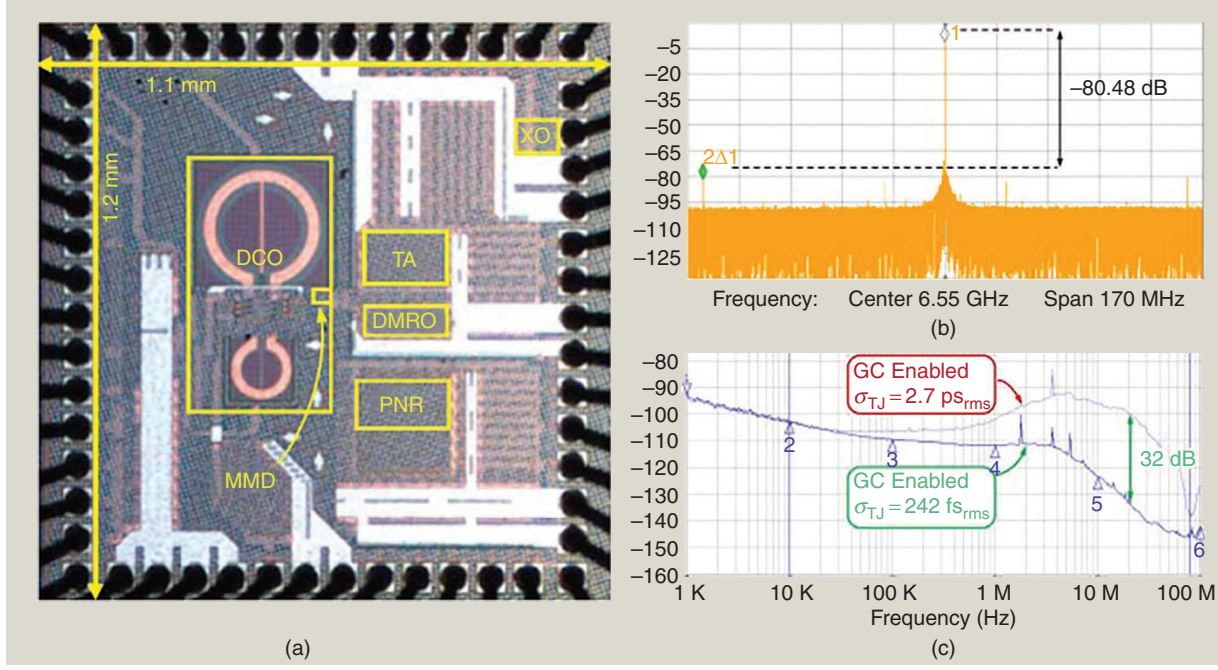

Figure 11. *The digital fractional-N PLL including gain calibration and time amplifier: (a) chip photograph, (b) output spectrum at 6.5 GHz showing low reference spur, and (c) phase noise with and without gain calibration enabled. DCO: digitally controlled oscillator; PNR: place and route; DMRO: dual-mode ring oscillator; TA: time amplifier; XO: crystal oscillator; MMD: multi-modulus divider; GC: gain calibration.*

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wireless communication. Wi-Fi, and even Bluetooth Low Energy—despite "low energy" being in the name of the standard—often dominate the overall power of such devices, and thus, such devices either require wall power or have a short battery life.

In the groups of Prof. Patrick Mercier and Dinesh Bharadia, work envisions a future where devices like wireless security cameras do not have to be plugged into the wall and can be placed anywhere, or where the battery life of other IoT devices can be 100 times longer. The key to enabling this vision involves not generating the Wi-Fi or Bluetooth signals on the IoT device itself but rather leveraging the fact that smartphones and routers, which either have a large battery or are already plugged into the wall, do a very capable job of generating these signals already. By hitchhiking on top of these existing transmissions, the IoT device can avoid the power consumption of expensive circuits operating at GHz frequencies.

A technique to achieve this is backscatter communication, whereby an incident Wi-Fi or Bluetooth signal arrives at an antenna, and depending on what impedance is loading the antenna on the IoT device, a certain portion of the signal will be reradiated back to the environment. By dynamically controlling what kind of impedance is connected to the antenna, additional data can be modulated on top of the incident signal. While this forms the basis for RFID systems, and some previous work on Wi-Fi backscatter has been demonstrated using discrete parts [43], [44], our recent previous work showed that Wi-Fi communication can be achieved at ~1,000 times lower power than conventional approaches using this technique, a major improvement toward enabling the next-generation IoT vision [45], [46], [47].

The key challenge in backscatter communication, however, is range: since there is no active transmitter on the IoT device, the reradiated signal is weak

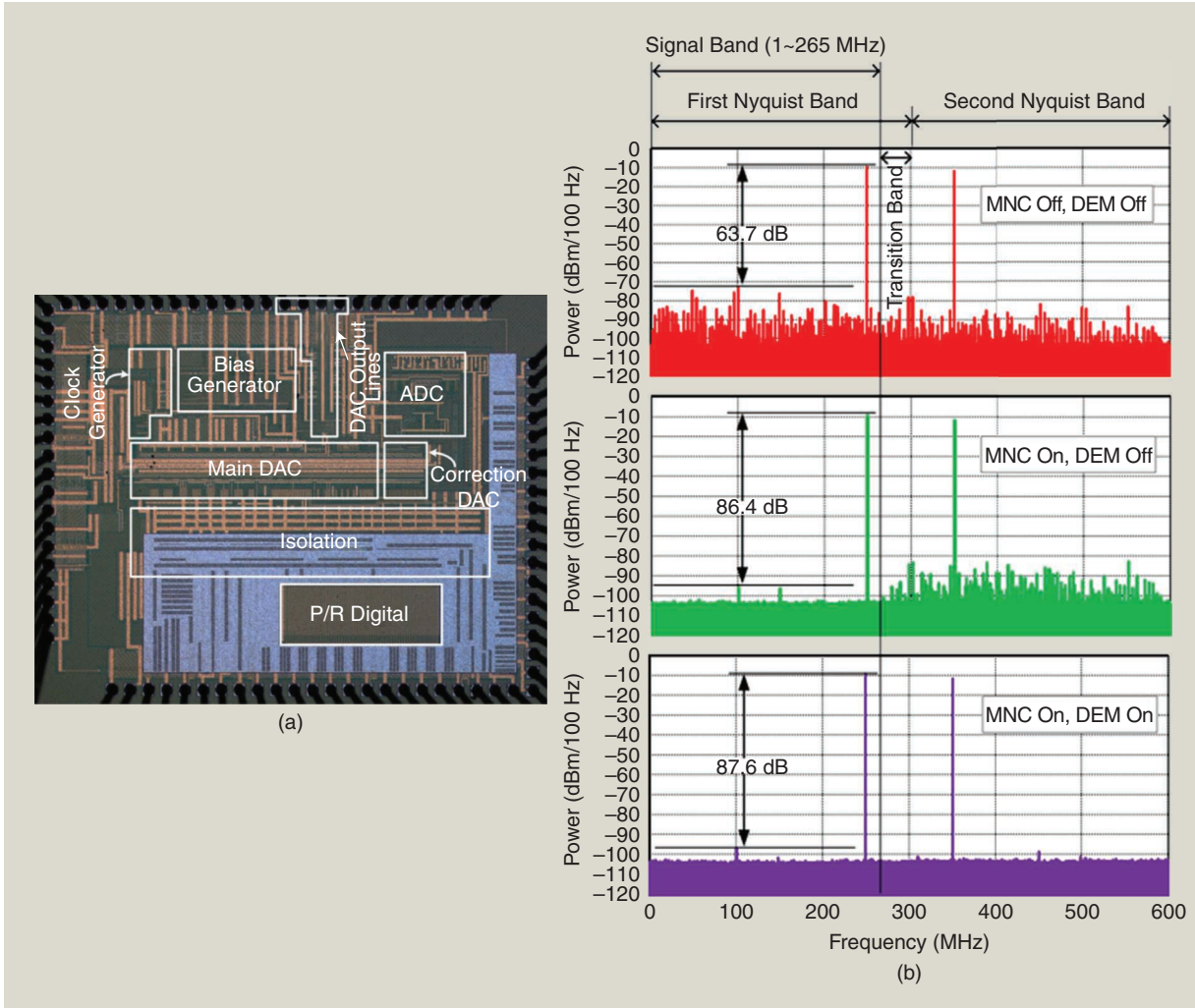

Figure 12. *The 600 MS/s DAC with adaptive cancellation of static and dynamic mismatch errors: (a) chip photograph and (b) one-tone output spectra with and without digital dynamic element matching (DEM) and MNC enabled.*

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and will only go so far before being lost to noise (e.g., 10 meters in previous work), as shown by the link budget in Figure 13. In fact, due to limitations set by the FCC, standards, or receiver noise constraints, the only way to improve range in backscatter systems is to either improve insertion loss at the tag or add multiple input/multiple output (MIMO) gain. Our most recent work featured improvements on both fronts [48]. For example, we developed a transmission-line-free single-antenna backscatter modulator that enables fully reflective single-side-band QPSK signaling without requiring a power combiner, thereby enabling a low overall insertion loss. Adding MIMO techniques on top of this normally requires precise control of the phase of a multi-GHz signal, which can consume significant amounts of power. In our latest work (Figure 14), we demonstrated this can be achieved with only microwatts of power by operating at baseband, thereby keeping the ~1,000 times power reduction in place, while increasing the range from 10 to 50+ meters [48] (Figure 15). We also demonstrated techniques to enable backscattering of Bluetooth signals, for an ~100 times power reduction. These results represent a major step forward to making backscatter communication, and as a result small, tetherless IoT devices, a reality.

Outlook

Academic research continues to have a major role in advancing microwave and mm-wave technology for wireless communications. Many academic demonstrations have been rapidly followed by industry. At UCSD, we appreciate that we have had access to a variety of advanced process nodes, which is important to push the state of the art. Although the coverage here is limited to highlights and short descriptions, interested readers are encouraged to view the attached references or contact the authors for further information.

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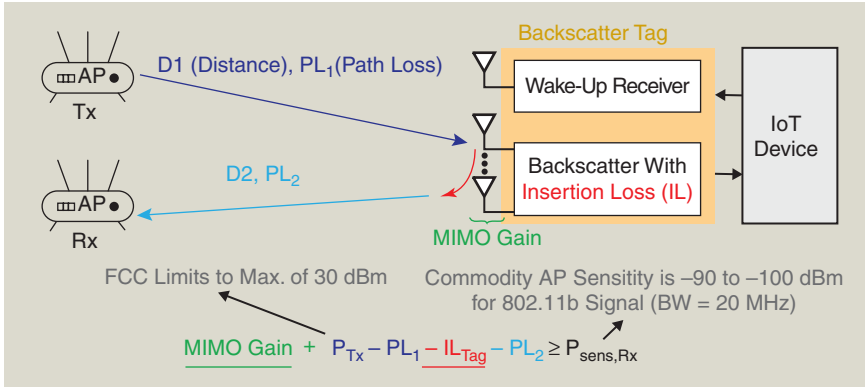

Figure 13. *The link budget constraints in backscatter systems. The only opportunity to improve the range involves improving the insertion loss and adding multiple input/multiple output (MIMO) gain. BW: bandwidth; TX: transmitter; RX: receiver; AP: access point.*

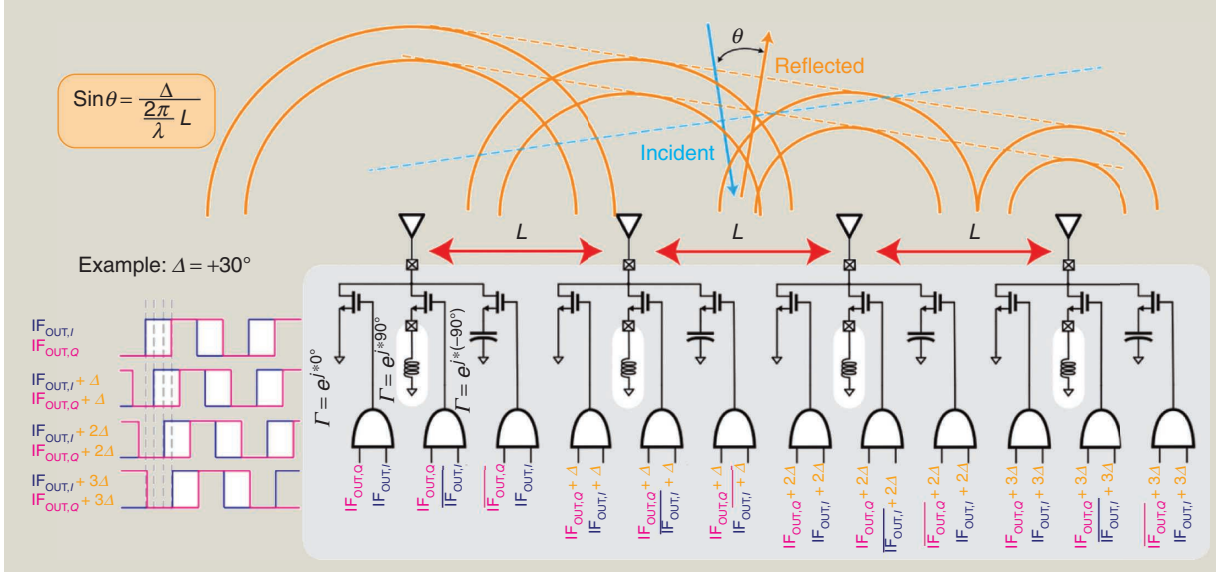

Figure 14. *A schematic of a beam-steering fully reflective backscatter modulator.*

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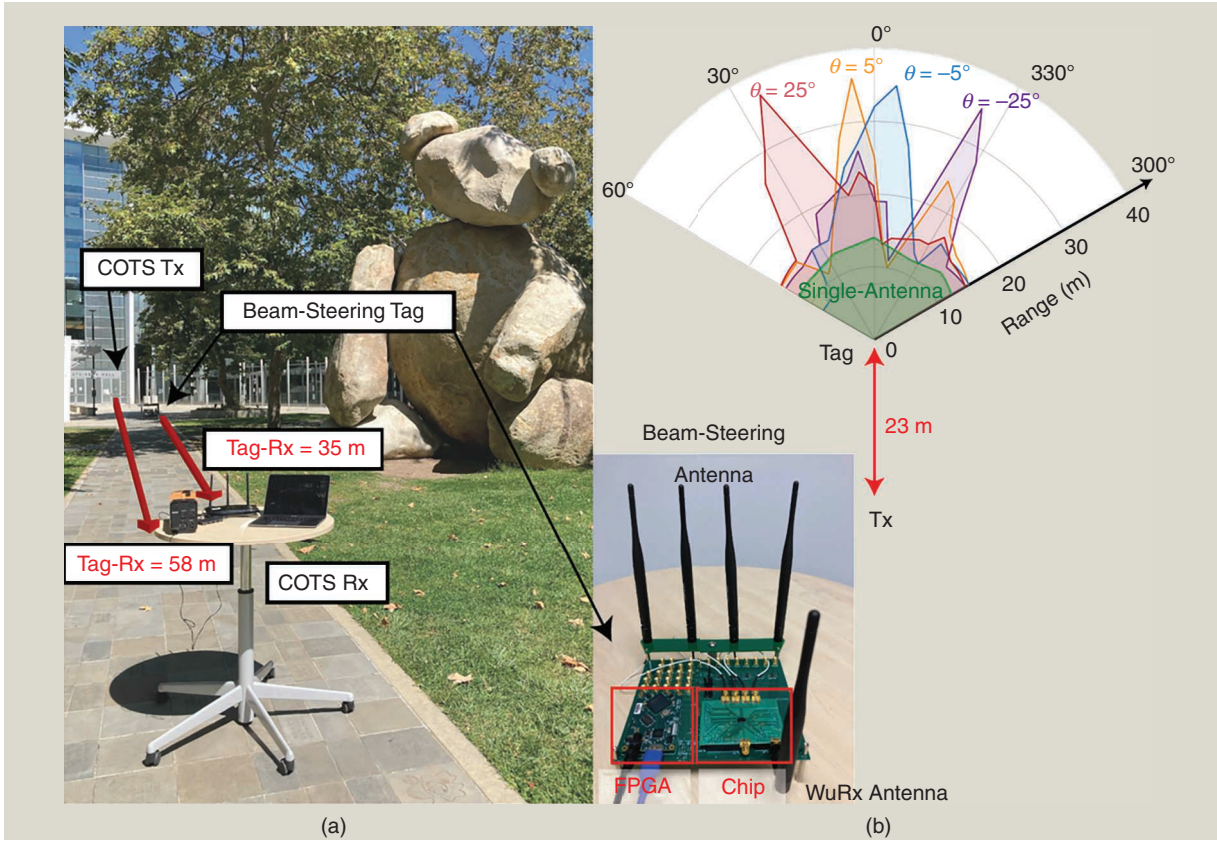

Figure 15. *A photograph of the test setup, demonstrating a 58-m Wi-Fi access point separation (tag in between) with (a) reliable communication and (b) beam-steering capabilities. COTS: commercial off-the-shelf; FPGA: field-programmable gate array.*

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