Current Sensing Front-Ends: A Review and Design Guidance

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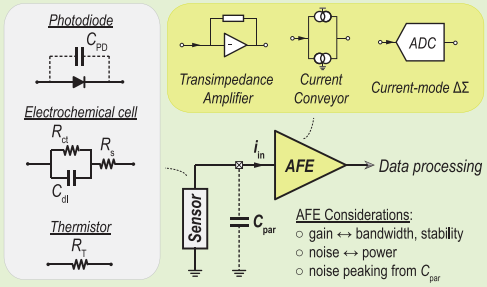
***Abstract*—Sensors link the physical and electronic worlds, finding uses in environmental, automotive, industrial, communication, and medical applications, among many more. Here, current-output sensors and current-sensing front-ends are reviewed, aiming to provide readers comprehensive design guidance from both sensor and circuit perspectives. Starting from the transduction method, capacitive, resistive, diode/FET-based, and MEMS sensors are individually reviewed with a focus on applications, circuit models, and nonidealities that must be considered for the front-end design. This is followed by a discussion of current-sensing front-ends, including transimpedance amplifiers (TIAs), current conveyors (CC), current-to-frequency (*I*-to-*F*) converters, and current-mode delta-sigma (I-ΔΣ) modulators. Each front-end is analyzed in terms of gain, bandwidth, stability, noise, and general design considerations are presented. State-of-the-art works for each front-end are then reviewed, and tradeoffs between different architectures are discussed.**



***Index Terms*—Sensor, current sensing, front-ends, transimpedance amplifier, current conveyor, delta-sigma.**

I. Introduction

SENSORS are ubiquitous in nearly all aspects of our daily life ranging from environmental and industrial to medical applications. They serve as the gateway for humans and machines to gain awareness and understand the environment from a macroscopic down to a microscopic level. In addition to the sensor that captures the signal of interest, one also needs a front-end to record and process it. A well-engineered acquisition system can be challenging to realize as it requires designers to have a deep understanding of both the sensor and circuit – two very different skill sets. This paper aims to bridge this gap by reviewing different types of sensors and circuit design considerations for front-ends and providing readers with practical knowledge on how to design a front-end for their sensor.

The fundamental principle of a sensor is the ability to transduce an external stimulus into an electrical signal. Among which, current-output sensors refer to the subset of sensors whose output signal is a current. In this paper, current-output sensors are referred to as "current sensors" for simplicity. However, readers should note that current sensors might refer to the sensors that measure a current outside the scope of this paper. Based on the underlying transduction method, current sensors are categorized into four main types, *i.e.* capacitive [1]–[11], resistive [12]–[23], diode/FET-based [24]–[31], and microelectromechanical system (MEMS) sensors [32]–[38], as shown in Fig. 1. For both capacitive and resistive sensors, they are typically biased at a constant voltage such that a current signal is generated from a change in sensor impedance due to stimuli (*e.g.*, temperature [13], humidity [4], or biomolecular interaction [10]). On the other hand, diode- and FET-based sensors work by lowering a semiconductor barrier in response to stimuli. Classic examples of this type of sensors are photodiodes [27], [39] and ion-sensitive field-effect transistors (ISFETs) [26]. Finally, MEMS sensors, while often capacitive, require much different design considerations than conventional capacitive sensors and therefore deserve their own discussion.

To interface with the sensor, an analog front-end (AFE) typically consists of an amplifier, some filtering, and an analog-to-digital converter (ADC). In a current-sensing AFE, the sensor output is converted to a voltage by a transimpedance amplifier (TIA), time by a current-to-frequency converter (*I*-to-*F*), or interfaced with current-mode circuits to avoid the need for an explicit transimpedance element. Typical current-mode circuits include current conveyors (CC) and current-mode delta-sigma (I-ΔΣ) modulators. Each of these front-ends has a constellation of performance tradeoffs, includ-

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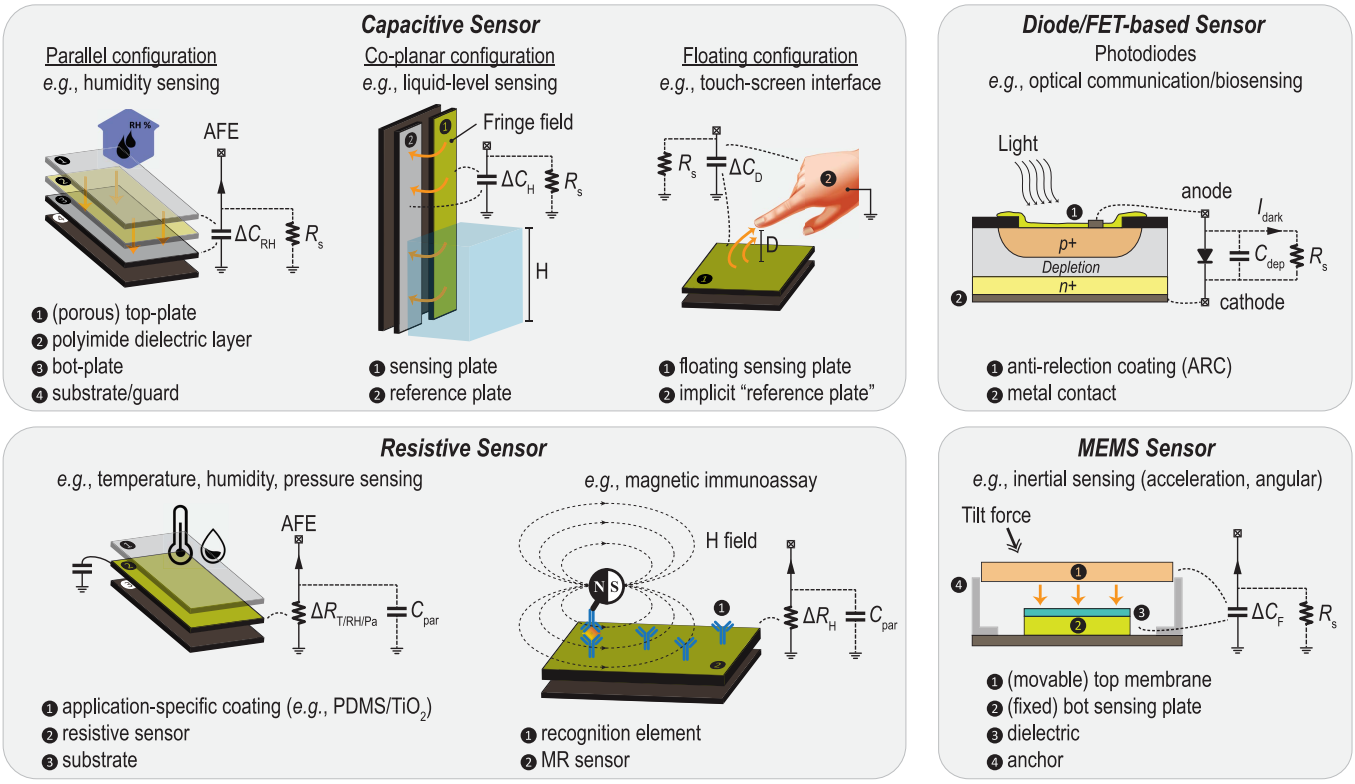

Fig. 1. Examples of current sensors and their applications.

ing bandwidth, noise, power, and input impedance, among others. Choosing and designing the appropriate readout circuit is critical to achieving high performance from any sensor. Even though there are many other semiconductor technologies such as bipolar junction transistors (BJT) or bipolar CMOS (BiCMOS), they are far less commonly used and prone to issues such as large input bias current. Therefore, this paper focuses discussion on front-end designs to integrated and discrete CMOS implementations.

The rest of this paper is organized as follows: Section II reviews current sensors starting with their transduction principle, applications, and nonidealities. While we illustrate this with biosensors, the discussion of sensor nonidealities is generally applicable. Section III, IV, V, and VI describe the four main types of current AFEs: TIA, CC, I-$\Delta\Sigma$ modulators, and I-to-F converters, respectively. Each architecture is reviewed and analyzed in terms of its gain, bandwidth, stability, and noise performance. In Section VII, low-leakage printed circuit board (PCB) design considerations and cleaning protocols are described. State-of-the-art current sensing AFEs are summarized in Section VIII, and the advantages and disadvantages of each front-end architecture are discussed in a comparative manner. Finally, Section IX concludes this paper.

II. Sensors Overview

A. Capacitive Sensors

Capacitive sensors are used in a wide range of applications, including liquid level sensing [1], [2], environmental sensing (gas [3], humidity [4], etc.), touch interfaces [5], [6], material analysis [7], and life science applications [8]–[10]. Capacitive sensors are formed by two conductive electrodes separated by a dielectric where the material properties are modulated by the stimuli, as shown in Fig. 1. For example, polyimide is an insulating material with a dielectric constant dependent on humidity, thus can modulate the capacitance at different humidity levels. The high electric field between the parallel plates allows capacitive sensors to have very high sensitivity. Several other capacitive sensor geometries, such as co-planar and floating structures, exploit the principle of fringe capacitance – a consequence of the fringing electric field at the edge of a conductor. In a co-planar configuration, the two electrodes are arranged side-by-side (or interdigitated) in the same plane. In this way, the electric field lines are more dominant near the edges between the electrodes such that this type of sensor has high sensitivity along the z-axis, enabling applications ranging from liquid level sensing [1] to molecular sensing (*e.g.*, bacteria growth monitoring [8], neurotransmitter detection [9], cell culture monitoring, and drug testing [10]). The electrode placement remains the same in a floating configuration; however, the second electrode is instead implicitly defined by a grounded medium that can be, for example, the culture solution for living cell monitoring [11], as shown in Fig. 2(a), or a fingertip for touch display applications [5], [6]. Unlike the parallel-plate capacitance, the fringe capacitance is non-linearly related to the sensor area, often necessitating finite element modeling (FEM) and geometric optimization.

In electrochemistry, an electrode submerged in an electrolyte has an electrode-electrolyte interface modeled as a double layer capacitance, C_{dl}, which is a series combination of the Stern layer and diffuse layer capacitors [40]. The capacitance per unit area is very high ($\sim$1 pF/μm^2), with sensor areas that are often several square millimeters resulting

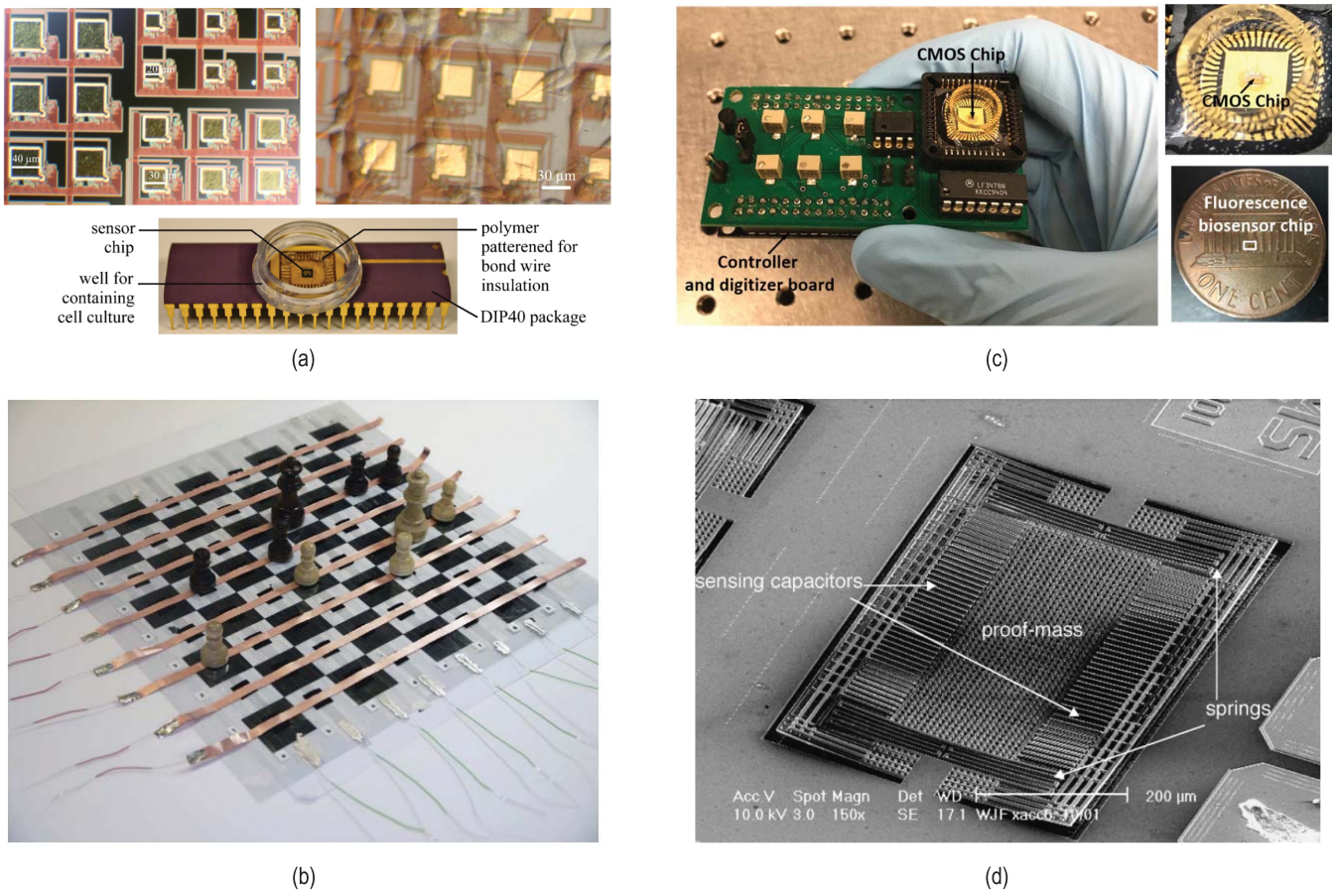

Fig. 2. Examples of current sensing systems based on sensor types: (a) a capacitive sensing platform used to monitor the *in-vivo* proliferation of breast cancer cells [11], (b) a prototype chess board with an ultra-sensitive resistive pressure sensor based on a microstructured conducting polymer thin film [15], (c) the first single-chip fluorescence-based biosensor with integrated nanoplasmonic filters [39], and (d) scanning electron microscope (SEM) image of an ultra-sensitive capacitive MEMS accelerometer [32].

in large capacitances. This capacitance is in parallel with a charge transfer resistance, R_{ct}, that is all in series with the solution resistance, R_s, as shown in the abstract figure. The signal from C_{dl} can be non-faradaic, faradaic, or a combination of both, as in the case of fast-scan cyclic voltammetry (FSCV), a technique with high temporal resolution used to study neurotransmitters [41]. In a non-faradaic process, the current is a direct result of charging or discharging the capacitor, *i.e.* $i = C\ dV/dt$, whereas in a faradaic process, ions transfer electrons during a reduction-oxidization (redox) process at the electrode-electrolyte interface resulting a current proportional to the analyte concentration.

The sensitivity and dynamic range (DR) are important parameters to define when designing a capacitive sensor AFE. Since the change in capacitance (ΔC) may be orders of magnitude smaller than the nominal capacitance (C_0), this often requires a capacitive AFE to have a DR of more than 40 dB and, in some cases, upwards of 100 dB. In addition, any form of a capacitance-to-current front-end must be concerned with the stray capacitance at the input node because it can significantly affect the bandwidth, stability, and noise performance of the system. This stray capacitance can come from packaging, connections between the sensor and front-end on the PCB, and/or the sensor itself.

B. Resistive Sensors

Resistive sensors have been reported for environmental monitoring applications including temperature [12]–[14], pressure [15], [16], [23], and gas sensing [17], [18], as well as biosensors for proteomics [19] and lab-on-chip platforms [20]–[22]. Among them, resistor-based temperature sensors, or thermistors, are made with metal oxides with large temperature coefficients. Resistive pressure and gas sensors are based on piezo-resistive and chemo-resistive effects, respectively. For pressure sensors, a polydimethylsiloxane (PDMS) elastomer doped with conductive composites such as graphene and carbon-nanotubes has been recently reported to increase the sensitivity [16], [23]. Fig. 2(b) shows an example of a resistive pressure sensor array that achieves 1 Pa sensitivity using a modified polymer thin film. The key challenge for pressure sensors has been achieving high sensitivity across a large pressure range. Similarly, in sensing gas, highly conductive metal electrodes (*e.g.*, Pt) are generally modified by acceptor coating materials (*e.g.*, TiO_2 for sensing H_2) for high selectivity. Compared to their capacitive counterpart, resistive gas sensors are less sensitive to parasitic capacitance but suffer from temperature and humidity drift [42].

Examples of magnetic sensors used for current sensing are Hall-effect and magnetoresistive (MR) sensors [43]. Sensing

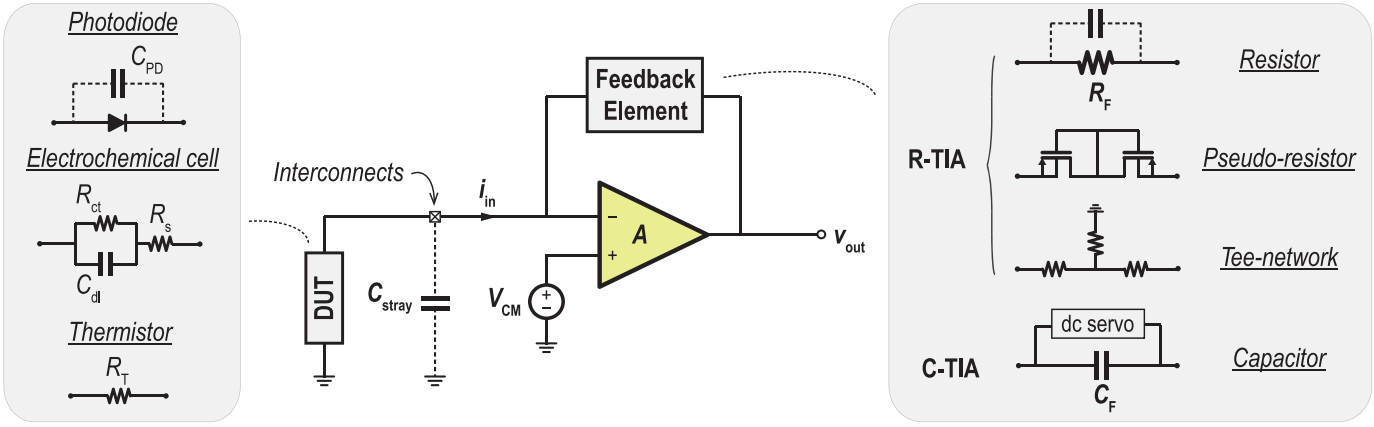

Fig. 3. Transimpedance amplifier with different feedback configurations and input sensor models.

using a magnetic field has enabled Hall-effect sensors to be widely employed in non-contact current monitoring, position sensors, and automotive applications. For MR sensors, the sensor resistance is a function of the applied magnetic field due to quantum mechanical effects. They have been used as the read head in rotating hard disk drives and recently biosensors to detect biomolecules labeled with magnetic nanoparticles (MNPs) [44], [45]. Since biological samples are intrinsically non-magnetic, this enables MR biosensors to achieve very high sensitivity. However, the need for an external magnetic field (*e.g.*, magnet, electromagnet, etc.) generally makes such platforms bulky.

Although resistive sensors can be easily arranged in a differential configuration (*i.e.* Wheatstone bridge), they often have a sizeable sensor-to-sensor mismatch and still require front-ends with large DR (>40 dB) to compensate. Worse yet, in applications such as MR biosensing, the presence of an external field leads to a large baseline-to-signal ratio ($R_0/\Delta R$) and requires an even larger DR (>80 dB). In cases where a signal pattern is predicable, signal processing techniques such as matched filtering can increase detection efficiency [46]. On the other hand, noise peaking concerns for resistive sensor front-ends are less significant due to lower input capacitance.

C. Diode/FET-Based Sensors

Diode- and FET-based sensors are semiconductor devices that modulate their conductance in response to stimuli, often non-linearly. Among which, photodiodes (PD) generate currents due to the presence of light and are often used for communication [47]–[49], automotive [50], [51], and biosensing (*e.g.*, SPR [28], ELISA [29], [31]). Optical sensing is typically complicated and bulky as it requires a multitude of external optical elements such as lasers, lenses, filters, and/or photo-multiplier tube (PMT) detectors. However, Hong *et al.* demonstrated an optical biosensing system (Fig. 2(c)) with integrated waveguide-based filters in a standard CMOS technology [39], opening a promising landscape for compact optical sensing systems. Among FET-based sensors, ISFETs are a type of electrochemical biosensor that modulate the channel conductance based on charged species present at the gate electrode. ISFETs have been reported for detection of DNA hybridization [24] and immunoassays [25], but they are mostly used as pH sensors [26].

Unfortunately, both PD and ISFET experience large sensor mismatch and temperature dependency, making a pseudo-differential architecture less effective at canceling the common-mode variation. Worse yet, the sensitivity and DR of a PD are typically limited by the dark current. In image sensors, signal-processing techniques such as spike-based encoding are used to recover the DR [52]. The parasitic capacitance of a PD heavily depends on the process and how the *pn* junction is implemented [53]. Although it can be small (0.2 to 0.5 pF [54]), the PD capacitance can seriously complicate the front-end design for high-speed applications.

D. MEMS Sensors

MEMS sensors are often treated as a subset of capacitive sensors. However, the design considerations for MEMS are very different from the ones for general capacitive sensors described earlier since MEMS sensors target an entirely different set of applications such as accelerometers [32]–[35] and gyroscopes [37], [38]. In MEMS sensors, as illustrated in Fig. 1, one side of the capacitor plate is movable under an exerted force to change the sensor's inertial state. The plate's movement alters the electric potential between plates; therefore, it can be measured as a change in capacitance.

Negative feedback (*e.g.*, TIA, I-$\Delta\Sigma$) improves linearity and lowers sensitivity to process, voltage, and temperature (PVT) variation; however, it is particularly challenging to introduce another feedback in a MEMS system due to the existing feedback in a typical accelerometer or gyroscope that is used to control the proof mass position of the sensing element [34]. The system dynamics require careful attention to not cause instability. MEMS sensors are mostly fabricated through specialized micromachining processes (*e.g.*, surface micromachining in Fig. 2(d)) and connected to front-ends through wire bonding or flip-chip techniques, which can cause large parasitic capacitance on the order of a few pF. As will be discussed later, large input capacitance for a current front-end can cause more noise and even stability issues.

III. Transimpedance Amplifier

A. Overview

TIAs have been widely investigated and employed for optical receivers [55]–[59], biosensing [60]–[63], and many other applications due to their simplicity and a reasonable trade-off between design parameters such as noise, bandwidth, and power [39]. A TIA converts the current into a voltage signal with a transimpedance element, either a resistor or capacitor, known as a resistive-TIA (R-TIA) capacitive-TIA (C-TIA), as shown in Fig. 3. The reason behind such I-to-V conversion is that signal processing (*e.g.*, filtering, digitization, etc.) is traditionally done in the voltage domain.

In a conventional R-TIA, a resistor, R_{F}, is connected in feedback between the inverting and output nodes of an amplifier while the non-inverting terminal is driven to a potential, V_{CM}, that also biases the sensor, as shown in Fig. 3. There is usually also a feedback capacitor (explicit or parasitic) connected in parallel with R_{F} that determines the TIA's stability and band limits the signal. The amplifier's non-inverting input is also connected to the sensor, known as the device under test (DUT). This node is often referred to as a "*virtual ground*" since the negative feedback ensures minimal voltage perturbation. The current signal from the DUT, i_{in}, flows through R_{F} whose value, when the open-loop gain of the amplifier is much greater than unity, determines the total transimpedance gain. The output voltage, v_{out}, is simply related to the input current as: $v_{\mathrm{out}} = V_{\mathrm{CM}} \pm i_{\mathrm{in}} R_{\mathrm{F}}$, with the sign depending on whether the DUT is sinking (+) or sourcing (−) current. Having a virtual ground at the input node means one has full control over the sensor voltage, which can be helpful in, for example, electrochemical impedance spectroscopy (EIS), where the DUT is excited with a sinusoidal voltage and the impedance calculated by reading the resulting in- and quadrature-phase currents. Many advantages of the R-TIA stem from the fact that it is a closed-loop system. Negative feedback around the amplifier ensures a constant transimpedance gain and makes it insensitive to variation in the amplifier's open-loop gain. It can also be easily shown that the negative feedback reduces the input impedance, which is desirable for a current front-end, while simultaneously lowering the output impedance, which is desirable for a voltage output.

B. Gain, Bandwidth, and Stability

While a TIA structure is relatively straightforward, contradicting design requirements such as high gain, large bandwidth, and low noise make designing a TIA a non-trivial task. Since increasing the gain usually has the opposite effect on the bandwidth and stability, the three parameters must be considered together during the design process. As shown in Fig. 3, the total input capacitance, C_{IN}, is the parallel combination of the sensor capacitance (photodiode, C_{dl}, etc.) and the total stray/parasitic capacitance, C_{stray}, from the amplifier input and routing interconnects. The amplifier has a single-pole response $A(s) = A_0/(1 + s\tau_{\mathrm{A}})$ where A_0 is the dc gain and τ_{A} is the RC time constant for the internal pole at frequency, f_{A}, *i.e.* $\tau_{\mathrm{A}} = 1/(2\pi f_{\mathrm{A}})$. The closed-loop transimpedance

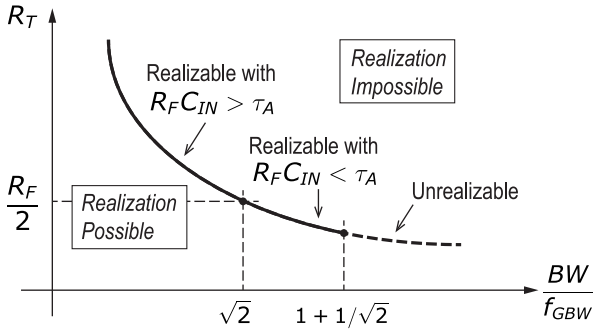

Fig. 4. Tradeoff between BW and R_{T} for an R-TIA [64].

frequency response, $Z_{\mathrm{T}}(s)$, can be derived as [64]

$$Z_{\mathrm{T}}(s) = -R_{\mathrm{T}} \frac{1}{1 + \frac{s}{\omega_0 Q} + \frac{s^2}{\omega_0^2}} \tag{1}$$

$$R_{\mathrm{T}} = R_{\mathrm{F}} \frac{A_0}{A_0 + 1} \tag{2}$$

$$\omega_0 = \sqrt{\frac{A_0 + 1}{R_{\mathrm{F}} C_{\mathrm{IN}} \tau_{\mathrm{A}}}} \tag{3}$$

$$Q = \frac{\sqrt{(A_0 + 1) R_{\mathrm{F}} C_{\mathrm{IN}} \tau_{\mathrm{A}}}}{R_{\mathrm{F}} C_{\mathrm{IN}} + \tau_{\mathrm{A}}} \tag{4}$$

where R_{T} is the dc gain accounting for the finite loop gain, ω_0 is the natural frequency, and Q is the quality factor describing the damping behavior of the filter response. For a typical peaking-free Butterworth low-pass characteristic, $Q \leq 1/\sqrt{2}$ and therefore the maximum bound on transimpedance gain is

$$R_{\mathrm{T}} \leq \frac{f_{\mathrm{GBW}}}{2\pi C_{\mathrm{IN}} BW^2} \tag{5}$$

where BW is the TIA's −3dB bandwidth and $f_{\mathrm{GBW}} = A_0 f_{\mathrm{A}}$ is the amplifier's gain-bandwidth product (GBW). This bound is known as the *transimpedance limit* [65] and was generalized for other TIA topologies by Säckinger [64]. The transimpedance limit describes the maximum transimpedance gain a TIA can achieve for a given bandwidth. The tradeoff between transimpedance and bandwidth of an R-TIA for a given amplifier GBW can be represented graphically in Fig. 4, which can be helpful for TIA designers to make an educated estimate of the amplifier requirements for a particular design. For applications (*e.g.*, biomedical) that need considerable gain (>100 MΩ) for high sensitivity, large R_{F} can be implemented as a discrete chip resistor, on-chip as a pseudo-resistor [66], or in a tee network configuration [67].

The TIA stability is another important design consideration due to C_{IN}, especially for sensor applications where C_{IN} can be quite large or the TIA is near the transimpedance limit. For example, the C_{dl} introduced by electrochemical sensors can easily be a few nF [41]. As a result, $C_{\mathrm{IN}} R_{\mathrm{F}}$ may introduce a pole within the loop bandwidth and cause instability. The feedback capacitor, C_{F}, introduces a zero in the feedback path to compensate for the phase shift from the input time constant. C_{F} may be either an explicit or parasitic capacitance. The ∼1 pF capacitance from the PCB and package is often sufficient for high gain discrete designs. Extra care must be

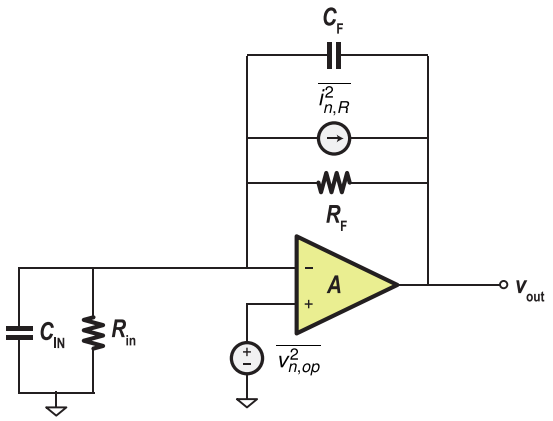

Fig. 5. Noise sources in an R-TIA with the input sensor replaced by an equivalent circuit model.

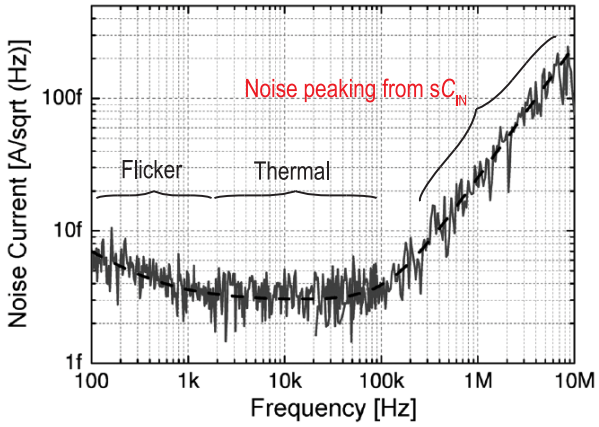

Fig. 6. Representative input-referred current noise PSD in a TIA [60].

taken with the tee network due to the parasitic capacitance at the intermediate node. To find a good starting point for sizing C_F, it is mathematically convenient to calculate C_F for a phase margin of 45° where

$$C_F = \frac{1}{4\pi R_F f_{GBW}} \left(1 + \sqrt{1 + 8\pi R_F C_{IN} f_{GBW}}\right). \quad (6)$$

However, designers should overcompensate the TIA to ~65° phase margin considering the tolerance in C_F as well as the fact that PVT variation may shift the amplifier bandwidth.

C. Noise

The noise model of a typical R-TIA is shown in Fig. 5. Having a resistor in the feedback path unavoidably adds to the total input-referred noise of the system. The input-referred current noise power spectral density (PSD) is

$$\overline{i_n^2} = \frac{4k_B T}{R_F} + \overline{v_{n,op}^2}\left[\frac{1}{R_F^2} + (2\pi f)^2 (C_F + C_{IN})^2\right] \quad (7)$$

where $\overline{v_{n,op}^2}$ is the input-referred voltage noise of the amplifier, k_B is Boltzmann's constant, and T is the temperature. The two main contributors to the noise are the resistor and the amplifier's noise. Decreasing the amplifier's noise typically comes at the expense of higher power consumption whereas R_F can be maximized considering the amplifier output swing. However, as shown in (5), larger R_F reduces the closed-loop bandwidth making it undesirable for high-speed applications. There has been research on noise-canceling (NC) techniques to reduce the TIA noise by 15% while maintaining a large bandwidth [57]. In the proposed NC-TIA, the noise voltage at the input and output of the TIA are added destructively through an auxiliary path while the signal is unaffected. However, such cancellation is very sensitive to PVT variation and ineffective at canceling the thermal noise from R_F, therefore R_F still needs to be maximized and the tradeoff remains.

Another implication of (7) is in its second term where the amplifier noise is scaled by the total input capacitance and asymptotically increases at 20 dB/dec, typically dominating the noise performance at high frequency, as shown in Fig. 6. Unfortunately, this noise-peaking behavior is shared among all current front-end topologies, making low-power, low-noise, and high-bandwidth TIA design a very challenging topic. Therefore, most TIAs are designed to be application-specific. For example, TIAs for biosensing applications are usually heavily bandlimited to achieve low noise and power since most biological signals are slow (<100 Hz) while having large gain (>10 MΩ). On the other hand, broadband (>GHz) TIAs for optical applications are typically very power-hungry and have considerably lower gain (<100 kΩ).

D. Capacitive TIA

Besides its effect on the bandwidth, large R_F (up to GΩ) also poses a practical limitation due to the area required in CMOS implementations and tolerance in discrete applications. C-TIAs are one way of eliminating such limitation by replacing R_F with a noiseless capacitor. In CMOS technologies, capacitors are usually preferred since operational transconductance amplifiers (OTAs) have high output impedance. As shown in Fig. 7(a), a C-TIA is essentially an integrator whose output voltage is a function of the integrated input current. However, like all integrators, a C-TIA is prone to saturation when given a dc input signal or leakage. Therefore, a simple reset switch across C_F is used to reset its charge periodically and provide a dc feedback path. In the presence of a signal with a large dc component, as in many bio-applications (*i.e.* dark current from photodiodes or ionic current in nanopores), the reset time can set an unreasonably short measurement period. Continuous-reset schemes using a pseudo-resistor [68], [69] or current reducer [60] (Fig. 7(b)) have been proposed to maintain large bandwidth at the expense of linearity and additional power overhead. A second stage differentiating amplifier is needed to recover a linear relationship between the input current and output voltage. The resulting topology is referred to as the *integrator-differentiator* architecture. The differentiator's noise is inconsequential as it is heavily attenuated by the first stage when input-referred. As a result, a C-TIA offers unique advantages of high sensitivity and very low noise across a wide bandwidth.

The total transimpedance gain for a typical integrator-differentiator architecture is $R_d C_d / C_i$ where C_i is the integrator

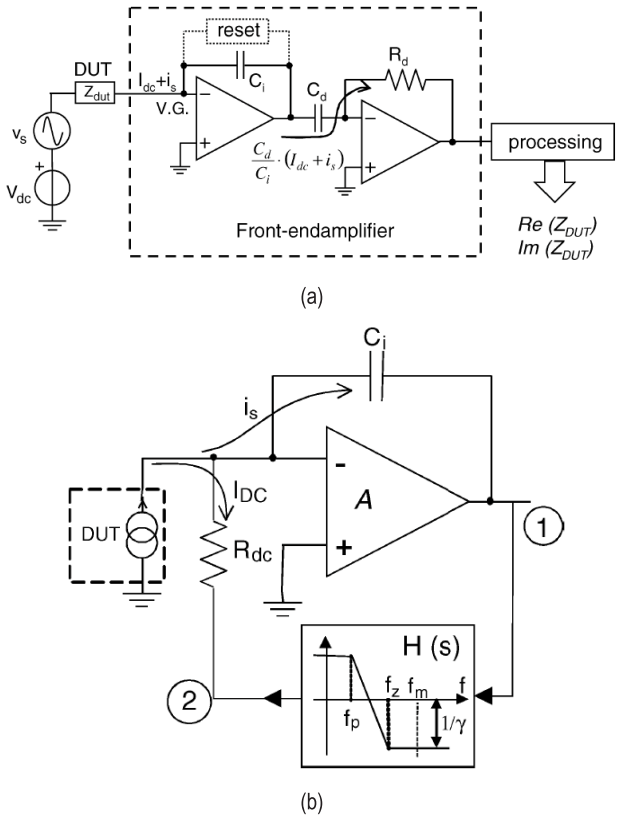

Fig. 7. (a) Example of an impedance spectroscopy setup using the integrator-differentiator architecture with a reset network to prevent saturation of the integrator induced by the dc input current, (b) schematic of a C-TIA with active feedback as a continuous reset [60].

feedback capacitance and R_d and C_d are the RC components in the differentiator, as shown in Fig. 7(a). The closed-loop bandwidth is

$$f_{-3dB} = f_{GBW}\frac{C_i}{C_i + C_{IN}} \tag{8}$$

where C_{IN} is the total input capacitance and f_{GBW} is the gain bandwidth product of the opamp. It is beyond this paper's scope to derive the exact expression for frequency response and input-referred current noise for a C-TIA as it depends on how the dc servo loop is implemented. In general, designers need to consider the thermal noise introduced by the active path in a continuous-time feedback implementation. In a discrete-time reset scheme, the system is limited by the k_BT/C and folded-back high-frequency noise due to sampling. However, it has been shown that correlated double sampling (CDS) is very effective at eliminating correlated noise such as k_BT/C and flicker noise in a discrete-time system [70]. However, designers also need to be aware that CDS increases the overall white noise due to noise-folding.

E. Common-Gate TIA

As mentioned above, traditional shunt-feedback TIAs have reduced bandwidth and instability when presented with a large input capacitance. The common-gate TIA (CG-TIA) has been proposed as an alternative TIA topology where the open-loop nature eliminates stability concerns. As a result, CG-TIAs are widely used in high-speed optical receivers with large photodiode parasitics [71]–[73]. In a typical CG-TIA shown in Fig. 8(a), the input current is sensed by a CG stage which provides an input impedance of roughly $1/g_m$, where g_m is the transconductance of the input transistor M_1. The drain terminal of M_1 is connected to a resistor, R_T, which defines the total transimpedance gain. In this way, the input impedance (input pole) and the transimpedance (output pole) are conveniently decoupled and can therefore be optimized separately, a notable advantage over its shunt-feedback counterparts. To further reduce the input impedance of a CG-TIA, techniques such as regulated-cascode [71], [72] and negative impedance by cross-coupling CGs [73] have been proposed.

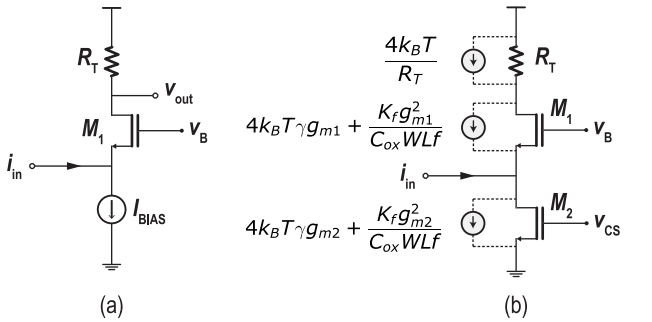

Fig. 8. (a) Basic common-gate TIA implementation; (b) Noise sources in CG-TIA including current source noise.

The main challenges in designing CG-TIAs are noise and limited headroom. Noise sources in a typical CG-TIA are shown in Fig. 8(b). Since the input transistor M_1 forms a cascode stage when the input is open (to calculate current noise), it contributes negligibly to the total input-referred current noise at low frequency. However, the noise current produced by the load R_T and current source M_2 are directly referred to input as

$$\overline{i_n^2} = \frac{4k_BT}{R_T} + 4k_BT\gamma g_{m2} + \frac{K_f g_{m2}^2}{C_{ox}WLf} \tag{9}$$

where g_{m2} is the transconductance of M_2, γ and K_f are both process dependent coefficients ($\gamma = 2/3$ for long channel devices and >2 for deep sub-micron processes), C_{ox} is the unit oxide capacitance, and W and L are the width and length of the transistor, respectively. A CG-TIA typically has higher noise due to the first term in (9) since the size of R_T is limited by the headroom. In low voltage designs, R_T is usually maximized for transimpedance gain and lower noise; hence the IR drop across R_T severely limits the headroom available for the rest of the circuit.

Table I provides a non-exhaustive summary of state-of-the-art TIAs in different form factors. This table aims to provide readers with general guidance on picking or designing the TIA for their sensor of choice. Benchtop TIAs provide excellent performance and flexibility due to additional features such as active cooling or capacitance neutralization, which come at the cost of power and size. Integrated solutions

TABLE I
STATE-OF-THE-ART TRANSIMPEDANCE AMPLIFIERS

	Reference	Topology	Gain (Ω)	Input Range [a]	BW (Hz)	IRN (fA/ √ Hz)	C_{IN} [b] (pF)	I_{BIAS} (fA)	Power (mW) @ Supply (V)	Application
Bench-top	Femto™ DDPCA-300	R-TIA	10 k – 10 T	1 mA	1 – 400	0.2 – 45,000	5	30	1050 @ 15	General
	Axopatch™ 200B	R-TIA	0.5 – 500 G	200 nA	70 k	11 – 30	-	1000	-	Patch-clamp
	SRS™ 470	R-TIA	1 k – 1 T	5 mA	10 - 1 M	5 – 150,000	-	-	6000 @ 24	General
	Keithley™ 480	R-TIA	1 k – 100 G	10 mA	1 – 10 k	1.2 – 900	-	-	-	General
Discrete	LTC6563	R-TIA	22.2 k	90 µA	500 M	4,500	1.5	-	200 @ 3.3	Lidar
	ADN2820	SiGe R-TIA	5 k	1.4 mA	9 G	10,000	-	-	200 @ 3.3	Ethernet
	OPA857	R-TIA	5 k, 20 k	240 µA	105 M, 125 M	125,000	2	-	77 @ 3.3	Optical
Integrated	Ferrari [60]	C-TIA	60 M	10 nA	4 M	4	-	-	45 @ 3	General
	Mulberry [63]	C-TIA	0.86 – 7 G	1 nA	4.4 k	6.25	-	-	12.5 @ 3.3	Nanopore
	Kang [62]	C-TIA	10 M – 10 G	100 µA	5 M	1,700 – 30,000	-	-	5.2 @ 1.8	Ultrasound
	Rosenstein [61]	R-TIA	100 M	1.5 nA	1 M	41	1	-	5 @ 1.5	Nanopore
	Djekic [66]	R-TIA	1 M – 1 G	20 nA	8 k – 2 M	5.5 – 140	-	-	9.2 @ 1.8	General
	Ray [72]	CG-TIA	50 k	30 µA	6.3 G	27,000	1	-	108 @ 1.2	Optical

[a]Maximum input I_{peak} [b]input stray capacitance, not the input capacitance used for noise characterization
BW: bandwidth, IRN: input-referred noise, I_{BIAS}: input bias current

typically employ the C-TIA topology and open a new frontier for large-scale parallel sensing, especially in arrayed applications, such as biosensors and touch displays. Discrete solutions provide a middle ground between compactness and versatility and are used in low channel count applications and for prototyping.

IV. CURRENT CONVEYOR

A. Overview

A current conveyor (CC) is the most integral building block of any current-mode circuit due to its versatility and ability to handle a large input range with high efficiency. It is worthwhile to introduce the concept of a current-mode circuit first to help further the discussion. Current-mode circuits are characterized as circuits whose signals of interest are handled in the current domain without the need for a transimpedance element, such as in a TIA. For example, the current signal from the sensor can be directly processed by current-mode circuits (*e.g.*, CC or current-input ADC), eliminating the need for an extra step to convert the signal into the voltage domain followed by a voltage-mode ADC. The advantages of current-mode circuits should become evident at this point, as they: 1) do not require a high-performance closed-loop amplifier for large voltage gain; 2) are easily scaled into advanced CMOS process nodes since the limited supply voltage does not constrain their DR, and they do not need high precision passive components; and 3) show high performance in terms of speed, bandwidth, and accuracy.

The concept of a CC was first introduced by Sedra and Smith [74], and it has since been shown using the *Theory of Adjoint Networks* [75], [76], that all active devices can be made of a suitable connection of one or two CCs (specifically the second generation CC, or CCII), making the CC a versatile component in analog systems. As shown in Fig. 9, a CCII is a three-port system that can be represented by a transfer matrix that captures the current or voltage expression at each port. The CCII has a transfer matrix of

$$\begin{bmatrix} i_Y \\ v_X \\ i_Z \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 \\ 1 & 0 & 0 \\ 0 & \pm 1 & 0 \end{bmatrix} \begin{bmatrix} v_Y \\ i_X \\ v_Z \end{bmatrix} \tag{10}$$

where i_k and v_k are the current and voltage at port *X, Y,* and *Z*, respectively. Therefore, the voltage at the input node *X*, v_X, follows the voltage applied to node *Y*, which has an infinite input impedance as it sees no current (the difference between CCI and CCII is whether $i_Y = i_X$ or $i_Y = 0$, respectively). The output node, *Z*, which has ideally infinite output impedance, carries the same (or opposite) current as i_X. The following intrinsic properties of a CC make it a promising front-end choice for sensor applications: 1) low input impedance for negligible signal attenuation and thus is less sensitive to stray capacitance at the sensor interface; 2) high output impedance as needed to drive subsequent

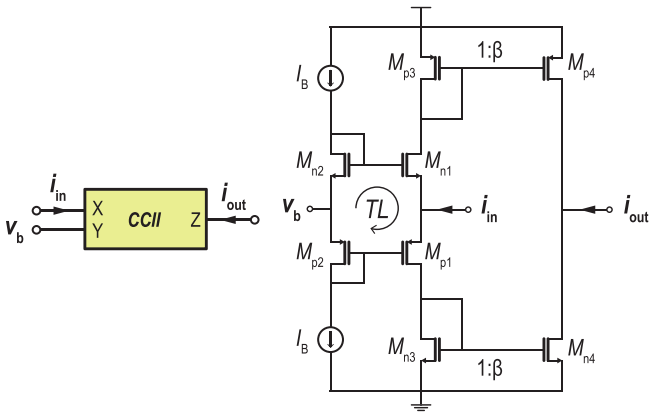

Fig. 9. Block representation and simplified CMOS implementation of second-generation current conveyor (CCII).

current-mode circuits; and 3) voltage following between nodes X and Y ensures a well-defined bias of the sensor voltage, which is required in most sensor applications [77]–[81].

The CMOS implementation of the CCII shown in Fig. 9 was derived from the CCI based on a translinear loop (TL) formed by the four input transistors [82]. The translinear principle exploits the exponential I-V characteristic of bipolar transistors [83], [84] and was later generalized for CMOS transistors operating in subthreshold (which also have an exponential I-V relationship) and eventually operating above-threshold [85]. The TL ensures accurate voltage following from node Y to X while defining a PVT-insensitive quiescent current flowing through transistor M_{n1} and M_{p1}, which solves the major limitation in early generation CCs [86], [87]. Another issue with conventional CCs is that they could not achieve simultaneous low quiescent power consumption and large input range since they have a maximum input and output current limited by the dc bias current. With the TL architecture, the CC has class-AB (push-pull) operation by conveying a current larger than its quiescent current, significantly increasing the current efficiency over its class-A counterpart. However, the additional transistors required to construct the TL loop unavoidably increase the minimum headroom margin by two overdrive voltages. To address this issue, class-AB CCs based on quasi-floating gate techniques were developed without the supply voltage penalty but at the cost of an additional amplifier and passive components used for ac coupling [88], [89].

B. Gain, Bandwidth, and Stability

The dc transfer function of the CCII in Fig. 9 can be derived by the size ratio, β, between the output current mirrors, M_{n4}/M_{n3} and M_{p4}/M_{p3}. To evaluate the ac response of a current-output circuit, the output port of the CC is shorted to ground in small-signal analysis, hence

$$\frac{i_{out}}{i_{in}}(s) = \frac{\beta}{1 + s R_{IN} C_{IN}} \tag{11}$$

where C_{IN} is the total input capacitance and R_{IN} is the finite input impedance of the CC, namely

$$R_{IN} \approx \frac{1}{g_{m,n} + g_{m,p}}. \tag{12}$$

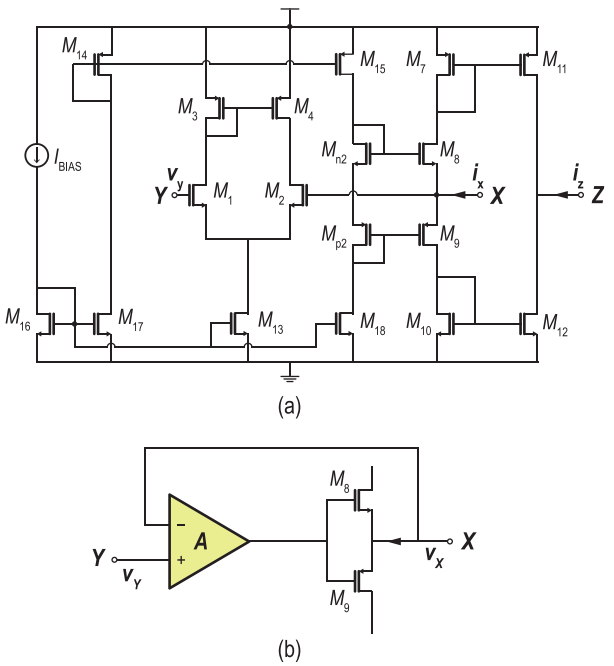

Fig. 10. (a) Schematic of an early class-AB CCII with opamp feedback to reduce the input impedance; (b) Conceptual model for the input stage proposed in [90] and later employed in [91].

One issue with a TL-based CC is that its input impedance is solely determined by the transconductance of the input transistors, which is highly dependent on the process and the quiescent current, I_Q, of the input branch. In low-power applications, when the CC is biased with a small I_Q, the transistors have small g_m therefore resulting in a relatively large input impedance (*e.g.*, ~2.5 MΩ at $I_Q = 10$ nA with $g_m/I_D = 20$, which places the input pole at ~60 Hz for $C_{IN} = 1$ nF), significantly limiting the frequency and noise performance.

To reduce the input impedance of a TL-based CC while maintaining the class-AB operation, I_Q can be increased for larger g_m. However, this increases the thermal noise and power consumption of the CC. Another approach is to use an amplifier feedback topology (Fig. 10), which was proposed in [90] and recently used in a current front-end for amperometry [91]. The resulting closed-loop system resembles a regulated common-gate structure, and the open-loop gain of the amplifier reduces the CC input impedance. However, the addition of a feedback amplifier may introduce stability concerns since there are two poles in the new CC structure – one pole remains at the CC's input, and the other is the dominant pole of the added amplifier. It can be shown that stability can be maintained if the unity-gain frequency of the amplifier is less than the input pole of the original CC [92].

C. Noise

Typical noise sources in a CC are shown in Fig. 11. For simplicity, assume the transconductance of the PMOS and NMOS transistors are the same, *i.e.* $g_{m,n} = g_{m,p} = g_m$, and the output current mirrors have a gain of β. The input-referred current noise PSD of a TL-based CC can be calculated as

$$\overline{i_n^2} = \left(4 + \frac{2}{\beta}\right)\left(4k_B T \gamma g_m + \frac{K_f g_m^2}{C_{ox} W L f}\right)\left(1 + s\frac{C_{IN}}{2g_m}\right)^2. \tag{13}$$

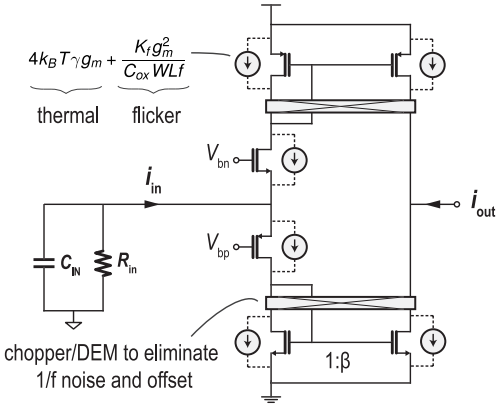

Fig. 11. Noise sources in a CCII with the input sensor replaced by an equivalent circuit model.

The first and second noise terms in (13) refer to the thermal noise (or shot noise, $2qI$, depending on the region of operation) and flicker noise of each transistor, respectively. The in-band flicker noise (and offset) of the current mirrors can be significantly suppressed by using chopping or dynamic element matching (DEM) at the expense of additional power from the clock and pseudo-random sequence generation [93]. The third term in (13) is why the input impedance of CC needs to be minimized such that the noise zero gets pushed away from the signal bandwidth. In the case of the feedback variant of the CC shown in Fig. 10, even though the input impedance is reduced, the amplifier introduces another noise source such that the input noise PSD becomes

$$\overline{i_n^2} = \overline{i_{n,\mathrm{CC}}^2}\left(1 + s\frac{C_{\mathrm{IN}}}{A_0 2g_{\mathrm{m}}}\right)^2 + \overline{v_{n,\mathrm{op}}^2}\left(\frac{1 + sR_{\mathrm{s}}C_{\mathrm{IN}}}{R_{\mathrm{s}}}\right)^2 \quad (14)$$

where A_0 is the dc gain of the added opamp, and R_{s} is the sensor shunt resistance, which is typically very large (>100 MΩ). Like the TIA, the voltage noise of the amplifier in a CC also scales with C_{IN} and needs to be minimized at the cost of more power consumption.

V. Current-Mode Delta-Sigma Modulator

A. Overview

Current-mode delta-sigma (I-ΔΣ) modulators have been gaining interest as sensor interfaces for direct current-to-digital conversion. Although most state-of-the-art continuous-time (CT) ΔΣ modulators are used for digitizing voltage signals, they can be adapted into a I-ΔΣ modulator by removing the input resistors such that the loop filter directly integrates the sensor current. Therefore, as will be shown later, many of the system-level considerations for CT-ΔΣ modulators also directly apply to I-ΔΣ modulators.

A I-ΔΣ modulator, in its most simplified form, consists of a loop filter (integrator), a quantizer (comparator), and a feedback network (resistor), as shown in Fig. 12(a). The resulting architecture is an error-feedback system that utilizes two key concepts: oversampling and noise shaping. In contrast to a Nyquist-rate ADC, a ΔΣ modulator is sampled at a frequency much higher than the signal bandwidth such that the output signal is recovered from the *averaged* bitstream

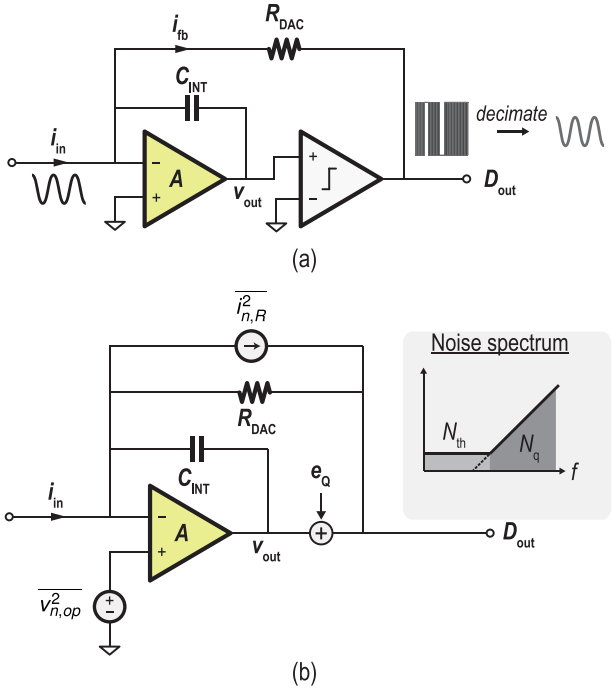

Fig. 12. Single-ended schematic of a 1st-order I-ΔΣ (a) with resistive feedback and (b) noise model with quantizer modeled as additive noise source.

sequence rather than an instantaneous quantization result. In a stable modulator, the negative feedback ensures that the *average* capacitor current is zero; otherwise, the voltage across the capacitor would be unbounded. Therefore, on average, $\overline{i_{\mathrm{in}}} = \overline{i_{\mathrm{fb}}}$, which results in a signal transfer function (STF) of

$$STF = \frac{\overline{v_{\mathrm{out}}}}{\overline{i_{\mathrm{in}}}} = -R_{\mathrm{DAC}}. \quad (15)$$

It can also be shown that the STF in the frequency domain is a $sinc$ function, which means that the modulator filters signals at integer multiples of f_{s}. This inherent anti-aliasing property is another advantage of a I-ΔΣ modulator such that it does not require extra filters to band-limit the noise. Compared to the aforementioned TIAs and CC, a I-ΔΣ modulator includes a highly nonlinear block – the quantizer, which directly adds a quantization error, e_{Q}, to the output, as shown in Fig. 12(b). To analyze the noise transfer function (NTF) from e_{Q} to the output, a CT ΔΣ can be rearranged into separate CT and discrete-time (DT) domains for simplicity [94]. In this way, the NTF is

$$NTF = 1 - \frac{A_0}{1 + A_0}z^{-1} \quad (16)$$

where A_0 is the dc gain of the integrator. Therefore, an ideal integrator results in a high-pass NTF that shapes most of e_{Q} away from the signal band. Such noise shaping behavior allows a ΔΣ modulator to achieve high resolution using only a coarse quantizer, which can even be a single-bit comparator, significantly relaxing the system's design complexity and area/power requirements.

A I-ΔΣ modulator can be directly connected to the sensor [95]–[99] or used after a current-mode AFE such as a

CC [77], [80]. For applications where the sensor is held at a constant dc bias voltage, direct quantization is superior in terms of noise performance, thanks to the inherent anti-aliasing of a CT ΔΣ. On the other hand, the latter scheme is generally employed in applications where voltage modulation is necessary (*e.g.*, cyclic voltammetry) such that the AFE shields the sensor voltage variation from changing the virtual ground of the modulator to achieve better linearity. Even though DEM can be used to eliminate the flicker noise of the current mirrors in a CC, having an additional stage unavoidably increases the total input-referred noise such that the shot noise of the CC usually limits the overall system.

The dynamic range of a I-ΔΣ modulator is determined by its loop filter order, quantizer resolution, and oversampling ratio ($OSR = f_s/(2f_b)$, where f_b is the signal bandwidth) while the feedback limits its input range. There has been work with higher-order modulators [41], but most low-bandwidth, moderate resolution sensor interfaces can get by with a 1st- or 2nd-order, single-bit design. To avoid having a prohibitively large OSR or current references spanning orders of magnitude, I-ΔΣ modulators with a duty-cycled DAC [97] or input [77] have been proposed where the reference (or input) is pulse-width modulated to achieve higher sensitivity and larger dynamic range with little power overhead or hardware complexity. However, this technique is only applicable to dc input signals and sensitive to charge injection from the sampling switch. Introducing a digital filter in a 1st-order loop has also been proposed to achieve multi-bit quantization and feedback with negligible power overhead [96], [98], [100].

Discussion on ΔΣ modulators can be found at both ends of the spectrum – too mathematical or too hand-wavy, neither of which provides helpful insight to new designers. In the following, general considerations for a I-ΔΣ modulator will be addressed in conjunction with a design strategy based on rules of thumb, aiming to equip the readers with practical tools to tackle the design of a I-ΔΣ modulator for their sensor.

B. Gain, Bandwidth, and Stability

Since a ΔΣ modulator is a data converter with a digital output, the concept of gain and bandwidth is different from the previous discussion of TIAs and CCs. In this section, the same analysis will be carried out for the integrator instead. Nevertheless, as will be shown later, the integrator's gain and bandwidth in a ΔΣ are tightly related to the specifications such as the OSR and f_s of the modulator.

The integrator is by far the most important block of a ΔΣ modulator as it is crucial to the overall linearity, in-band noise (IBN), and energy efficiency of the system. The most popular realization of an integrator in a ΔΣ modulator is to connect an OTA in feedback with a capacitor. An OTA with infinite gain and bandwidth means the integrator is linear. However, with finite dc gain, the integrator is referred to as a "lossy" integrator, as not all charge integrated on the capacitor corresponds to a voltage change at the output. A lossy integrator and the quantizer's nonlinear nature can lead to the occurrence of dead-zones, where inputs smaller than a specific level do not affect the digital output. In the frequency domain, a lossy integrator pushes the zero of the NTF in (16) away from dc, increasing the quantization noise in the signal band. A general rule of thumb is that the amplifier's open-loop dc gain in a single-loop modulator should be roughly equal to its OSR [101], *i.e.* $A_0 \approx OSR$, such that the additional quantization noise is less than 1.2 dB. The OSR of a ΔΣ can be chosen based on the target signal-to-quantization noise ratio (SQNR), as

$$SQNR_{\text{pk}} = \frac{3\,(2L+1)\,M^2 OSR^{2L+1}}{2\pi^{2L}} \tag{17}$$

where L is the order and M is the number of levels in the quantizer. The OTA bandwidth is another important design consideration as it can cause integrator gain errors and increase the total IBN. Through simulation, it is suggested that for a single-loop modulator, there is no significant IBN degradation if the GBW of the amplifier is roughly equal to f_s [101].

The stability of a 1st-order ΔΣ can be guaranteed if the input signal does not exceed the reference range. However, as the number of integrators increases in higher-order systems, stability becomes much less intuitive. Designers must rely on simulations or tools such as the *Delta-Sigma Toolbox* by Schreier to decide the scaling coefficients for each integrator and feedback path to maintain stable operation [102].

C. Noise

Assuming the flicker noise of the integrator and feedback DAC are eliminated with chopping or DEM, the modulator's IBN comprises both the thermal noise, N_{th}, and the quantization noise, N_q, that is shaped by the loop filter. It can be shown that decreasing N_q (by increasing the OSR or NTF order) has less than a linear power tradeoff, while decreasing N_{th} by 2× increases the power consumption by the same factor in a constant g_m/I_D design. As a result, a larger N_{th} can be tolerated with less power for the same total IBN. Therefore, in a typical ΔΣ design, the total IBN is strategically partitioned such that N_{th} accounts for most of the IBN budget for good power efficiency. A good rule of thumb is to keep N_q ~12 dB lower than N_{th} [94].

Neglecting the noise contribution from N_q and the latter stages in a higher-order design, the total input-referred (thermal) noise of a I-ΔΣ modulator can be expressed as

$$\overline{i_n^2} = \overline{i_{n,\text{DAC}}^2} + \overline{v_{n,\text{op}}^2}\left(\frac{1}{Z_s \parallel Z_{\text{fb}}}\right)^2 \tag{18}$$

where $\overline{i_{n,\text{DAC}}^2}$ is the thermal noise from the feedback DAC, and the second term in (18) is the integrator's input-referred voltage noise reflected into a current by the impedance seen at the input node (*i.e.* the parallel combination of the sensor, Z_s, and feedback, Z_{fb}, impedances). The feedback DAC can be realized as resistive (R-DAC), capacitive (C-DAC), or current-steering (I-DAC). It can be shown that R-DACs typically have better noise performance (>3 dB), but I-DACs are much smaller and easier to implement with a large dynamic range using techniques such as current-splitting [103]. C-DACs are less sensitive to clock jitter but necessitate an OTA with sufficiently high linearity due to the sharp transient current. Worse yet, C-DACs compromise the inherent anti-aliasing property

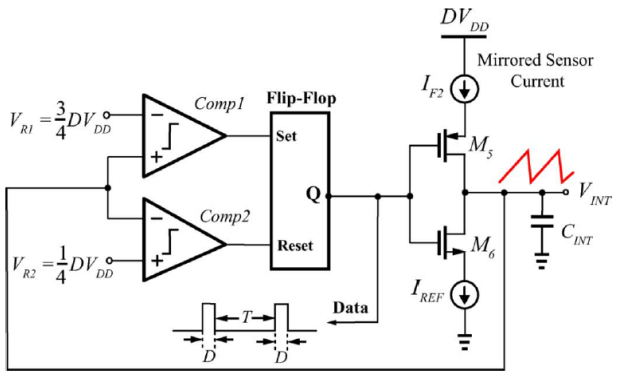

Fig. 13. Implementation of a current-to-frequency converter [107].

of CT-ΔΣ by sampling the virtual ground, which is a less popular choice [94]. There are other "noise-like" behaviors in a I-ΔΣ modulator, such as inter-symbol interference (ISI) and clock jitter. However, it is beyond this paper's scope to discuss all the nonidealities in a ΔΣ modulator.

VI. Current-to-Frequency Converter

A. Overview

I-to-F converters are another type of current-mode AFE that converts the sensor current into a time-domain pulse train whose frequency is directly proportional to the current magnitude [104]. Therefore, I-to-F converters achieve direct current quantization without an explicit ADC, significantly saving area, power, and complexity, and thus are often found in applications where the area is the most critical factor, such as implantable healthcare devices [105]–[107]. Another motivation for using an I-to-F converter is that the frequency/duty cycle modulated output waveform is intrinsically compatible with backscatter communication (load shift keying) – a wireless transmission technique often found in implantable/RFID system-on-chip (SoC) to greatly reduce the total power consumption by pushing the digitization and transmission burden to the host side.

B. Gain, Bandwidth, and Stability

I-to-F converters can be implemented by a current-starved ring oscillator whose oscillation frequency is proportional to the input current [105] or a pulse position modulator [106], [107]. An example of the latter is shown in Fig. 13, and the basic operation principle is as follows: the input current is mirrored to isolate the sensor from kickback. The mirrored current, I_{F2}, charges a capacitor, C_{INT}, until V_{INT} exceeds a pre-defined threshold voltage (*e.g.*, $3/4{\cdot}DV_{DD}$) of the comparator, *Comp1*, which flips the SR-latch output. Then, a reference current, I_{REF}, discharges C_{INT} until V_{INT} drops below the lower threshold voltage (*e.g.*, $1/4{\cdot}DV_{DD}$) of *Comp2*. Therefore, the duty cycle, D, and period, T, of the I-to-F converter output can be expressed as

$$T = \frac{DV_{DD}C_{INT}}{2I_{F2}} \tag{19}$$

$$D = \frac{DV_{DD}C_{INT}}{2I_{REF}}. \tag{20}$$

As such, the sensor current can be derived from the D/T ratio with respect to I_{REF} without precisely needing to know the values of C_{INT} or DV_{DD}. In the context of a wireless implantable system, where the I-to-F converter is connected to a backscatter switch for data transmission, the D/T ratio should be chosen to be less than unity (or <20% in [106]) such that the switch is open for most of the transmission period. This means I_{REF} should be a fraction [106] or larger [107] than the sensor current, depending on the orientation of the current sources. However, the absolute value of I_{REF} can be subject to PVT variation; therefore, a calibration step might be necessary to measure I_{F2} at the expense of added complexity and power overhead.

In Fig. 13, the windowed comparator (*Comp1* and *Comp2*) continuously compare V_{INT} to 3/4 and 1/4 of the reference voltage (DV_{DD}), respectively. Therefore, *Comp1* and *Comp2* should be implemented as NMOS and PMOS inputs, respectively, to ensure enough headroom for all transistors. Unfortunately, gain mismatch between the comparators results in an error in the output waveform. This behavior will be further discussed in the following section. The comparator bandwidth should be large enough to minimize error from the propagation delay for the narrowest pulse width, T_{min}, for the given signal range and C_{INT} (*e.g.*, ∼5× larger for 99% accuracy). Specifically,

$$\frac{g_m}{2\pi C_L} > \frac{1}{5T_{min}} \tag{21}$$

where g_m and C_L are the input pair transconductance and load capacitance of the comparators, respectively.

C. Noise

The noise contributors and noise-like nonidealities in an I-to-F converter consist of the thermal noise from the current sources, comparators, and reference voltages, as well as the nonidealities introduced by the comparators, *e.g.* offset and propagation delay. It can be shown that comparator offset only leads to a dc error in the final D/T ratio since the offset is constant for both the charge and discharge phase, therefore not affecting the overall linearity of the converter. However, the comparator propagation delay is signal-dependent as it takes more time to resolve to the correct state when V_{INT} is approaching the thresholds *slowly*, as in the case for a small input current. Thus, comparator delay introduces a signal-dependent variation in T and a dc offset in D, increasing the system's nonlinearity.

VII. Low-Leakage PCB Design Guidelines

In high-precision current-sensing applications, low leakage is required to measure current signals in the sub-pA range. Sometimes, the best effort in designing an ultra-sensitive AFE is ruined if a designer does not take care in reducing potential sources of leakage that exist between the AFE and off-chip sensors or test equipment. For a standard FR4 PCB shown in Fig. 14(a), where the chip is wire-bonded to the PCB (chip-on-board packaging) to reduce packaging parasitics, several things can cause leakage on the order of tens of pAs if preemptive measures are not taken, specifically: 1) surface contaminants

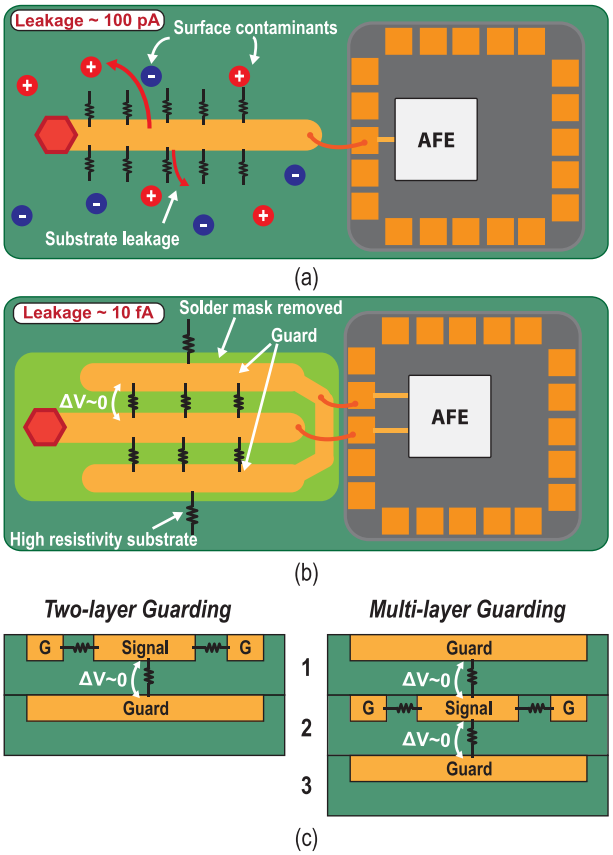

Fig. 14. Overview of leakage sources from PCB (a) with standard FR4, (b) proper PCB design for low leakage [108], and (c) cross-sectional view of two- and multi-layer guarding.

(flux residue), 2) surface charge (solder mask), and 3) substrate leakage [108]. Worse yet, PCB leakage is PVT dependent which makes it difficult to calibrate. In the following, PCB design and preparation practices such as guarding and cleaning are described (Fig. 14(b)). These techniques have been shown to reduce the PCB leakage to the low-fA level.

Guarding is a technique to protect the sensitive trace by surrounding it with another trace driven by a low impedance source. As such, guarding minimizes the potential difference between the signal trace and the guard traces, thereby significantly reducing the signal trace leakage [109]. Guarding is especially important if the PCB resistivity is low relative to the sensor impedance. For example, the typical resistance of a standard FR4 PCB is on the order of 10 GΩ. Under a 1-V difference between the signal and substrate, there will be a leakage current on the order of 10 pA if guarding is not implemented, which is unacceptable for fA – pA range sensing applications. However, conductive guard traces close to the signal trace can be another source of parasitic input capacitance, which designers should account for given the noise implications. In a lab setting, the guard is usually provided by the measurement equipment (*e.g.*, Keithley SourceMeter). However, in a practical deployment, designers need to provide the guard voltage by generating a replica of the signal voltage. In a TIA, this is usually the same voltage used to bias the sensor, V_{CM}. As shown in Fig. 14(c), guard traces should also be placed below and on the sides (on the same plane) of the signal trace. In multi-layer PCBs, the signal trace can also be sandwiched between two layers of guard traces.

Removing the solder mask is another useful PCB technique for leakage mitigation. Solder masks are generally used to reduce moisture infiltration into the PCB material and for ease of soldering. However, solder mask tends to accumulate surface charge that can causes leakage. Therefore, the solder mask should be removed around the guard and sensitive traces when designing a low-current measurement system.

The PCB substrate is a subtle but important consideration. Among them, FR4 glass epoxy is the most common insulating substrate on the market. However, when performance is the uttermost concern, PCBs with ceramic hybrid substrates, such as Rogers 4003C, typically have 1,000× higher resistivity than standard FR4. They have been shown to have ~5 fA of leakage, ~20,000× lower than standard FR4 [108]. Rogers substrates are often used in microwave and high-speed circuits but also show good performance in low-current applications by significantly reducing substrate leakage. Some designers forego the PCB connection entirely and "air solder" the input as air is an excellent dielectric.

Lastly, an assembled PCB should be adequately cleaned to remove surface contaminants such as dust or flux residue, contributing to leakage. In a typical cleaning protocol [110], the PCB is soaked in acetone for roughly ten minutes, followed by aggressively scrubbing with isopropanol. Then the PCB is rinsed with deionized water for a few minutes, blow-dried with nitrogen gas, and baked for 2 hours at 85 °C before use. Cleaning has been shown to reduce PCB leakage by more than 20× compared to an unwashed PCB.

VIII. Discussion

The development of ultra-sensitive sensors has spurred the need for higher and higher performance AFEs. Among these, CMOS designs have achieved state-of-the-art performance with ever-increasing sensitivity, dynamic range, and power efficiency. Such constant improvements over prior works are often made possible by innovative circuit design. Therefore, although this paper's scope is beyond just CMOS AFEs, Table II shows recent trends in CMOS current-sensing AFEs over the last decade. In the following, the four architectures described previously, *i.e.* TIA, CC, I-ΔΣ, and I-to-F converters, are compared on a system-level, aiming to provide readers with strategic design consideration to select the front-end topology best suited for their application.

R-TIAs provide a reasonable balance between key design parameters such as the gain-bandwidth product (GBW), power, and noise among the various front-end topologies. Therefore, R-TIAs are very versatile and can be found in an extensive range of applications with a wide range of specifications. However, as described in Section III, the transimpedance limit exhibits a quadratic power increase for large bandwidths making an R-TIA design for high-speed applications (*e.g.*, optical communications) typically consume tens of mW. Thermal noise from the feedback resistor also relegates R-TIAs to be

TABLE II
STATE-OF-THE-ART CMOS CURRENT SENSING FRONT-ENDS

Ref	Topology	Process (nm)	Gain	Input Range	BW (Hz)	IRN (fA/√Hz)	C_{noise} [a] (pF)	DR [b] (dB)	Power (mW) @ Supply (V)	Area [c] (mm^2)	Application
[60]	C-TIA	350	60 MΩ	10 nA [d]	4 M	4	1	60	45 @ ±1.5	0.34	General
[62]	C-TIA	180	10 M – 10 GΩ	100 µA	7.1 – 5.7 M	1,700 – 30,000	15	46	5.2 @ ±0.9	0.12	Ultrasound
[63]	C-TIA	350	0.86 – 7 GΩ	1 nA	4.4 k	6.25	-	68	12.5 @ 3.3	0.02	Nanopore
[61]	R-TIA	130	100 MΩ	1.5 nA	1M	41	1	31	5 @ 1.5	0.2	Nanopore
[55]	R-TIA	180	2.6 k	15 µA	8.5 G	11,600	0.2	24	81 @ 1.8	0.25 [e]	Optical Receiver
[56]	R-TIA	65	20 k	20 µA	10 G	7,000	0.1	29	23 @ 1.2	0.12	Optical Receiver
[58]	R-TIA	65	500 Ω	100 mA	40 G	19,800	-	88	55.2 @ 1.2	0.6	Optical Receiver
[59]	R-TIA	130	30 – 4,500 Ω	5 mA	27 G	20,000	-	64	313 @ 3.3	1.12	Optical Receiver
[66]	R-TIA	180	1 M – 1 GΩ	20 nA	8 k – 2 M	5.5 – 140	5	66	9.2 @ 1.8	0.07	General
[72]	CG-TIA	130	50 k	30 µA	6.3 G	27,000	1	23	108 @ 1.2	0.08	Optical
[88]	CC	500	1 – 15 A/A	50 µA	1 – 3 M	5,700	-	74	0.28 @ 3.3	0.127	General
[77]	CC + I-ΔΣ	500	1 – 32 A/A	16 µA	0.5	141	-	54	0.241 @ 5	0.157	Electrochemical
[80]	CC + I-ΔΣ	130	1 – 1/1000 A/A	1 mA	100	9,100	-	60	0.029 @ 3	0.16	Electrochemical
[96]	I-ΔΣ	350	-	2.8 µA	10	6,957	-	77	0.017 @ 1.5	0.5	pH
[98]	I-ΔΣ	180	-	1.1 µA	10	30	-	78	0.05 @ 1.8	0.11	Biosensing
[99]	I-ΔΣ	180	-	10 µA	1.8	74.5	-	160	0.295 @ 1.8	0.2	Biosensing
[100]	I-ΔΣ	55	-	200 µA	4 k	31,600	-	140	1.011 @ 1.2	0.585	General
[104]	*I*-to-*F*	180	-	11.6 µA	10 k	11.6	-	140	5.22 @ 1.8	0.091	Biosensing

[a]Input capacitance used for noise characterization [b]$20\log(I_{MAX}/I_{MIN})$ calculated at a fixed-gain setting [c]Active area (per channel)
[d]Frequency-dependent input range [e]Estimated
BW: bandwidth, IRN: input-referred noise

the worst in noise performance. On the other hand, C-TIAs have been shown to achieve the lowest input-referred noise (<10 fA/$\sqrt{}$Hz) by taking advantage of a noiseless feedback element. Despite the need for a second differentiator stage, its noise contribution is negligible due to the large gain from the integrator stage. As a result, C-TIAs are usually favored in low-noise applications. However, they are prone to saturation and require either periodic resetting [91] or a continuous feedback path to discharge the signal's dc component. Such reset techniques require clock generation and/or alter the C-TIA frequency response (*e.g.*, bandpass in [60]); therefore, they are generally not employed in wideband applications. The additional differentiator stage typically makes the overall C-TIA consume more power than its R-TIA counterpart. The effect of charge injection due to the reset switch was characterized for electrochemical sensors in [91]. The average current integrated onto the working electrode was more than 4× compared to a CC designed with the same power consumption and sampling frequency. Thus, one should consider the impact of having the sensor directly connected to a front-end that is chopped. Unlike R-TIAs or C-TIAs, CG-TIAs operate in open-loop such that a large input capacitance will not de-stabilize the amplifier. CG-TIAs are generally used in high-speed optical links where the PD parasitic capacitance is large given the bandwidth, and noise is not the most critical concern. CG-TIAs suffer from limited headroom.

The primary purpose of having a CC in a current-sensing AFE is to provide a low input impedance and voltage bias to the sensor while having moderate gain (<10 A/A) to relax the noise requirement of the following stages. A CC's gain is defined by a current mirror ratio, which is often chopped or rotated with DEM for high resolution at the cost of additional power. The transistors that cannot be chopped in a CC must be sized large enough to mitigate flicker noise

for a low-bandwidth design. CCs have been shown to have better current efficiency due to the class-AB operation and are particularly helpful in cases where a large voltage excursion needs to be applied at the sensor side (*e.g.*, scanning the working electrode in cyclic voltammetry) due to their ability to maintain linear current conveying across a wide input common-mode voltage range, which is typically unwanted for an amplifier, as in the cases for a TIA and I-$\Delta\Sigma$ modulator.

In cases where the sensor is biased at a constant dc voltage, a I-$\Delta\Sigma$ modulator can be used to directly quantize the signal for the best power efficiency. Due to oversampling, I-$\Delta\Sigma$ modulators typically target low bandwidth signals ($<$10 kHz). Unlike TIAs, I-$\Delta\Sigma$ modulators can theoretically achieve an extremely large dynamic range ($>$80 dB) by properly choosing the order, OSR, and quantizer resolution. An even larger cross-scale dynamic range ($>$120 dB) was reported using a current-steering DAC with a programmable range setting. For example, in [99], the input polarity was asynchronously flipped whenever the integrator output is close to saturation as detected by a windowed comparator. This technique essentially eliminates the need for resetting the C-TIA and allows continuous integration to achieve a state-of-the-art dynamic range of 160 dB with high linearity (7 ppm integrated nonlinearity). In [98], a sub-pA resolution was achieved by incorporating a digital prediction filter in a single-bit I-$\Delta\Sigma$ modulator to realize the equivalent of multi-bit quantization with negligible power overhead. However, the input impedance of a I-$\Delta\Sigma$ is quite high, and noise peaking needs to be considered for capacitive sensing.

Last but not least, I-to-F converters achieve direct quantization with very little hardware by converting the input current level to a frequency/duty cycle modulated waveform suitable for backscatter communication systems, such as often encountered in IoT devices. The current sources should be sized large or chopped if the resolution is limited by flicker noise. The input pairs of the comparators should also be sized large to increase the g_m/I_D ratio for low offset and input-referred noise. The passive capacitor can be replaced by an active integrator which provides a virtual ground for the current sources. However, the area and power overhead of an additional amplifier conflict with the incentive of using an I-to-F converter in the first place; therefore, this design is not generally used.

IX. Conclusion

Current sensors transduce current signals in response to stimuli from everyday life, spanning macroscopic signals such as temperature, pressure, and light to the microscopic regime such as biomolecular binding events. Their versatility has led to broad deployment in environmental, automotive, industrial, and medical applications. This article first reviewed examples of such sensors to gain an understanding of the application-specific requirements and nonidealities. While understanding the sensor is crucial, a complete sensing system requires engineers to know front-end design as well. This article then discussed the primary design considerations for three common current-sensing architectures, namely the transimpedance amplifiers (R-TIA, C-TIA, and CG-TIA), current conveyor (CC), current-mode delta-sigma modulator (I-$\Delta\Sigma$), and current-to-frequency (I-to-F) converters. R-TIAs provide a reasonable balance between key parameters such as gain-bandwidth product, power, and noise; therefore are the most commonly used. However, they are not suitable for high-speed or ultra-low-noise applications due to noisy shunt feedback and tightly coupled design parameters, such as the input impedance, transimpedance gain, stability, and bandwidth. C-TIAs are a low-noise variation for R-TIAs by utilizing a noiseless feedback element but require an auxiliary path (*e.g.*, dc servo loop or reset switch) to avoid saturation. CG-TIAs are the open-loop version of R-TIAs that do not suffer from instability with a large input capacitance but tend to be noisy and have limited transimpedance gain when resistively loaded. The transimpedance gain can be increased by using a CC. CCs have current gain and are usually paired with a current-mode ADC such as I-$\Delta\Sigma$ when there is a need to decouple the sensor from the ADC (*e.g.,* to provide low input impedance or voltage excitation). I-$\Delta\Sigma$ modulators have been gaining popularity as front-ends for resistive sensors and are best suited for applications where a large dynamic range is required (*e.g.,* biosensors where a small signal is superimposed on a significantly larger background signal). Despite not being as popular as the other AFEs, I-to-F converters are used in applications where size and power are of the most critical concerns, such as wireless systems. Last, this paper provided low-leakage PCB design guidelines that should be followed for high-sensitivity current front-end designs.

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