An Electrochemical CMOS Biosensor Array Using Phase-Only Modulation With 0.035% Phase Error and In-Pixel Averaging

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***Abstract*—This paper presents a 16 × 20 CMOS biosensor array based on electrochemical impedance spectroscopy (EIS), a highly sensitive label-free technique for rapid disease detection at the point-of-care. This high-density system implements polar-mode detection with phase-only EIS measurement over a 5 kHz - 1 MHz frequency range. The design features predominantly digital readout circuitry, ensuring scalability with technology, along with a load-compensated transimpedance amplifier, all within a 140 × 140 μm^2 pixel. The architecture enables in-pixel digitization and accumulation, which increases the SNR by 10 dB for each 10× increase in read-out time. Implemented in a 180 nm CMOS process, the 3 × 4 mm^2 chip achieves state-of-the-art performance with an rms phase error of 0.035% at 100 kHz through a duty-cycle insensitive phase detector and one of the smallest per pixel areas with in-pixel quantization.**

***Index Terms*—Point-of-care (PoC), electrochemical impedance spectroscopy (EIS), biosensor array, phase-to-digital converter.**

I. Introduction

POINT-OF-CARE (PoC) testing is a promising patient-centric paradigm that enables rapid biomarker detection near the patient, rather than the lengthy turn-around time associated with centralized facilities. PoC testing facilitates the diagnosis and monitoring of chronic diseases and deadly infections. The key objective of PoC testing is to allow for quick medical decision-making without sophisticated laboratory equipment so that appropriate treatment can be implemented and managed, leading to improved health and economic outcomes.

Some applications, such as DNA microarrays [1], [2], aptamer arrays [3], [4], and immunosignaturing [5], require high-density biosensor arrays consisting of hundreds to thousands of individually addressable sensors on a monolithic substrate for multi-analyte detection. These biosensor microarrays conventionally rely on optical detection methods like fluorescence and absorbance spectroscopy, exploiting light-biomolecule interactions to detect and quantify diverse analytes [6], [7], [8], [9]. However, these techniques require bulky optics [10], making them unsuitable for PoC applications.

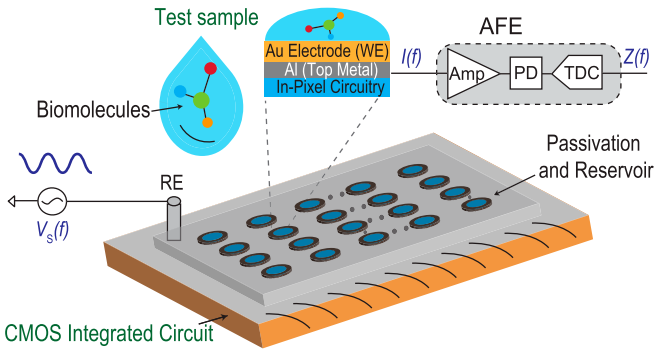

Fig. 1. Overview of a high-density CMOS-based EIS biosensor array.

Electrochemical biosensors are an attractive alternative to optical techniques due to their accuracy, speed, and simplicity [11], [12], [13], [14], [15]. Their ease of integration with CMOS circuits makes them highly miniaturizable and cost-effective. Electrochemical impedance spectroscopy (EIS) is a real-time, label-free sensing technique that measures changes in the interfacial properties of the electrode-electrolyte interface [16], [17], [18]. In EIS, a low-amplitude sinusoidal voltage signal (∼5-10 mV) swept across a frequency range (mHz – MHz) is applied to the sensor surface, and the induced current is measured to back-calculate the impedance (Fig. 1).

Fast Fourier transform (FFT) and frequency response analysis (FRA) are typical measurement techniques for the impedance analysis of electrochemical cells [19]. FFT analysis yields faster results using a multi-frequency input (*e.g.*, multi-sine, step/pulse waveforms, etc.) but requires anti-aliasing filters and a digital signal processor to extract each frequency component and correct nonlinearity errors. It is suitable for time-variant systems with single-site testing. In contrast, FRA applies a single-frequency sinusoidal stimulus and sweeps the input to characterize the impedance across the frequency range of interest. This minimizes the signal processing effort and the effects of distortion from the cell, simplifying the measurement circuitry and making it more suitable for high-density arrays [15], [19].

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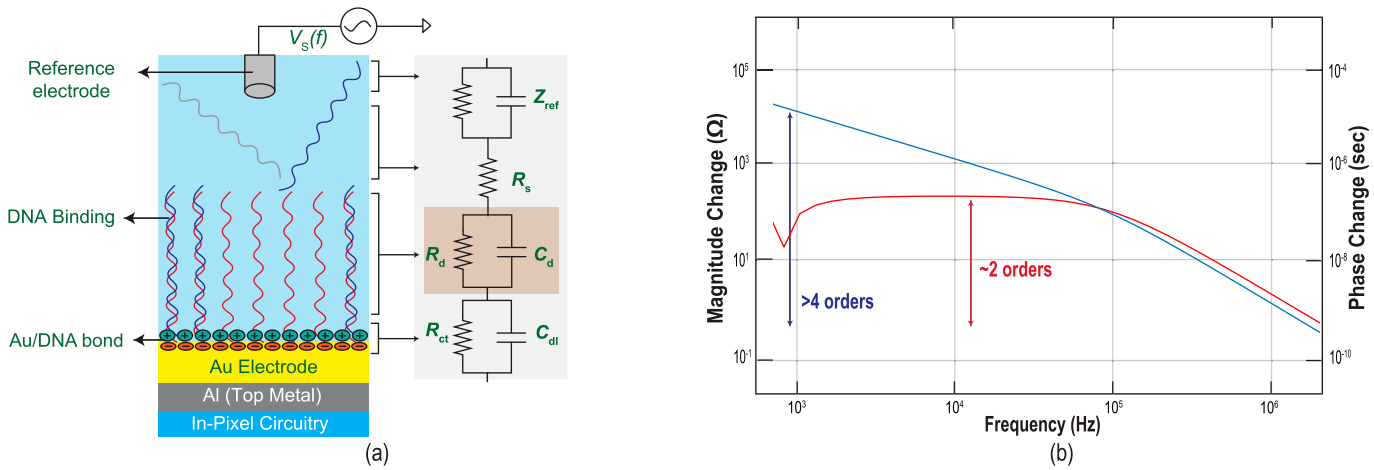


Fig. 2. (a) Equivalent electrode impedance model annotated with contributing factors (ions, DNA, double-layer capacitance, etc.). (b) Simulation results demonstrating the change in magnitude and phase before and after DNA hybridization.

Within FRA, the architectures can be classified based on the data interpretation strategy used. Nyquist ($Re\{Z\}$ vs. $Im\{Z\}$) and Bode ($|Z|$ and $\angle Z$ vs. frequency) plots are common representations for impedance spectroscopy. Unsurprisingly, the circuit architecture often falls out of the choice of data representation. Many designs implement *I*/*Q* demodulation with lock-in detection to capture the real and imaginary parts of the impedance [20], [21], [22]. This architecture consists of two identical channels with resource-heavy multipliers and low-pass filters. Moreover, the accuracy is highly sensitive to synchronization between the measured and demodulation quadrature signals. Lock-in detection employs one of three modulation schemes: pure sine, square, or pseudo-sine wave. Pure and pseudo-sine wave modulations introduce frequency-dependent phase errors in the reference generation block and bandwidth-limited readout circuits. The induced frequency-dependent errors necessitate complex calibration schemes or incorporate extra blocks like a phase-locked loop (PLL) [23]. Alternatively, polar mode (magnitude/phase) detection [24], [25] eliminates the quadrature signal generation and demodulation, avoiding such synchronization issues. However, it requires separate magnitude and phase detection blocks with minimal design overlap and different specifications [26]. The magnitude block, in particular, requires a high dynamic range [21], which makes its design especially challenging in an area-constrained setting.

This paper presents a 16 × 20 CMOS biosensor array with on-chip electrodes using phase-only EIS over a frequency range of 5 kHz – 1 MHz, as shown in Fig. 1. This high-density array has in-pixel averaging, which improves the SNR by 10 dB for each 10× increase in readout time when operated in fixed frequency time scan mode. This is accomplished using a phase modulation detection scheme, which relaxes the circuit complexity and lets each pixel have its own time-based digitizer. Combined with a mostly-digital architecture and transimpedance amplifier (TIA), this approach has one of the smallest areas per pixel with on-chip sensors and quantization, making the entire chip scalable with technology. The chip achieves a state-of-the-art phase error of 0.035% at 100 kHz through a duty-cycle insensitive phase detector. Hybridization and aptamer-antigen binding experiments demonstrate the intended use case where a single sample is run and assayed for multiple analytes. This paper extends the work originally reported in [27].

The rest of this paper is organized as follows: Section II explains the phase modulation detection technique. Section III analyzes the system architecture and compares it against [27], followed by the circuit-level implementation in Section IV. Section V presents the results of the electrical and biological measurements. Finally, concluding remarks are given in Section VI.

II. Phase Modulation Detection Technique

To appreciate the motivation behind using a phase modulation detection scheme, it is essential to understand the equivalent circuit model of the system and the changes it undergoes during a binding event. DNA is used as an example to explain the underlying principle, but this models any affinity interaction. Each on-chip electrode is immobilized with single-stranded DNA (ssDNA) capture probes. The probe sequence is complementary to the target DNA, providing the assay's specificity. When the sample is added, it selectively hybridizes with the probe to form double-stranded DNA (dsDNA). Fig. 2(a) shows the equivalent circuit using the well-known Randles circuit model of the electrode-electrolyte interface. In this model, R_s captures the ohmic resistance of the electrolyte, which depends on the solution salinity [28]. This is followed by a parallel combination of R_d and C_d, which model the diffusion layer consisting of the target and capture DNA probes. Finally, the electrode interface is described through the double-layer capacitance, C_{dl}, shunted by the charge transfer resistance, R_{ct} [28]. The contribution of R_{ct} can be neglected since the process is non-faradaic [26]. When the DNA hybridizes, the diffusion layer's charge distribution is altered, decreasing C_d [20], [29].

To comprehend its impact on impedance modulation, the change in magnitude and phase are plotted in Fig. 2(b). The Bode plot is derived by subtracting the magnitude and phase plots of the equivalent electrode impedance model shown in Fig. 2(a) before and after DNA hybridization. Using typical

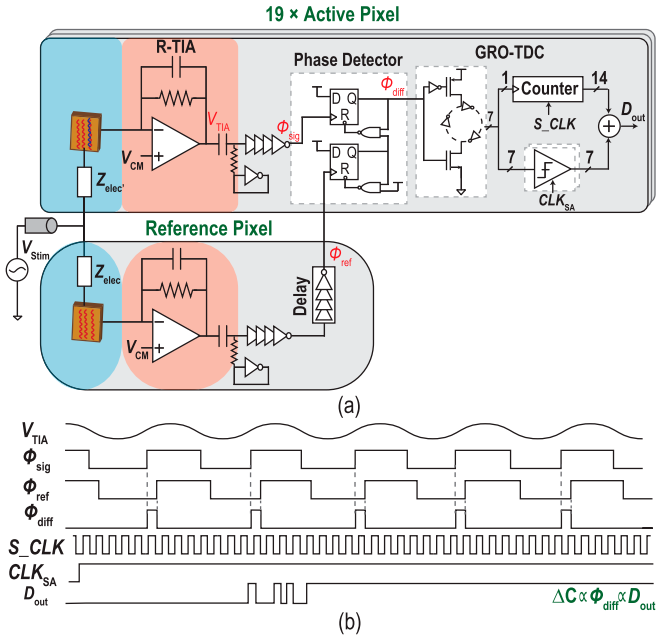


Fig. 3. (a) Block diagram of the in-pixel circuitry and (b) waveforms at each stage demonstrating operation.

values for a 100 × 100 μm^2 gold electrode in 4× saline-sodium citrate (SSC) buffer (C_{dl} = 4.5 nF, R_d = 10 MΩ, R_s = 1 kΩ, C_d = 3 nF), the simulation shows the system acting like a low-pass filter, settling to R_s at higher frequencies. SSC buffer is commonly used for hybridization and washing in assays with nucleic or ribonucleic acid species. The DNA hybridization-induced capacitance shift alters the filter cut-off frequency, leading to an ∼8.5% change in magnitude and phase in the 1 kHz–1 MHz range. Notably, the absolute magnitude change exceeds the absolute phase change by more than 100×. This results from the inherent folding property of the inverse tangent function that characterizes the system's phase. Consequently, utilizing only the phase of the complex impedance to detect binding simplifies the readout circuitry for two key reasons: 1) Removing the magnitude detector conserves power and area, and 2) The magnitude detection block requires more resources due to the wider dynamic range.

III. Architecture

A. System-Level Implementation

The biosensor chip consists of a 16 × 20 pixel array, of which one row serves as reference pixels, and the remaining 19 are active pixels. The active pixels in each column share a reference pixel located in the middle of the column to minimize the routing delay. Fig. 3 depicts the block diagram of the in-pixel circuitry. Each pixel consists of an on-chip electrode, a transimpedance amplifier, and a phase detector followed by a time-based ADC. The reference pixel has an identical electrode and amplification circuitry with an extra delay cell. An excitation voltage applied through an off-chip reference electrode induces a current amplified by a resistive feedback transimpedance amplifier (R-TIA). This design implements EIS over the 5 kHz – 1 MHz frequency range where the induced currents are in the μA range, requiring a modest transimpedance gain, which is neither area-limiting nor a major noise contributor. Hence, an R-TIA was chosen instead of a capacitive-feedback TIA.

The phase information is extracted from the zero crossings. An inverter chain after the R-TIA transforms the analog output into a rail-to-rail square wave, φ_{sig} and φ_{ref} from the signal and reference electrode, respectively, while maintaining the zero crossings. The phase of φ_{sig} is then compared with φ_{ref} via a duty-cycle insensitive D flip-flop (DFF)-based phase detector (PD) to produce a pulse, φ_{diff}, whose width is linearly proportional to the phase difference. This pseudo-differential measurement cancels common-mode variation, such as temperature drift and process variation. A delay cell was added in the reference path to avoid extremely narrow φ_{diff} pulses for near-zero phase difference, which would degrade the SNR of the system and cause a dead zone in the time-to-digital converter (TDC). A 250 ns delay was implemented to account for noise and mismatch from the in-pixel circuitry. This architecture is mismatch-tolerant, as the mismatch between the reference and signal path is converted into a constant offset at the PD output.

The pulse width is traditionally digitized using an oscillator-based TDC where the counter output corresponds to the number of delay elements that have transitioned during φ_{diff}. A gated ring oscillator (GRO)-based TDC enhances this process through first-order noise shaping of its quantization noise by preserving the oscillator state between measurements [30]. In short, each pixel's dedicated TDC allows in-pixel pulse averaging, enabling a trade-off between the readout time and noise. The accumulation of N pulses scales the signal by N, while the noise, which adds in power, scales by $\sqrt{N}$. This improves the SNR by 3 dB for every doubling of the integration time, assuming the phase noise is spectrally white within the frequency range of interest. The per-pixel TDC approach also eliminates a complex switching network with a shared ADC architecture. The digital output, D_{out}, is read using a serial peripheral interface (SPI).

Two key modifications were made to enhance the performance and robustness compared to the previously reported design [27]. First, the TIA was changed from Miller compensated to load compensated, reducing the area by >2×. This is crucial for minimizing pixel area while enhancing stability against process, voltage, and temperature (PVT) variation and electrode impedance. Second, the PD was upgraded to an edge-sensitive implementation, improving the linearity by ensuring monotonicity and insensitivity to the input duty cycle. This also makes the circuit mismatch and PVT robust.

B. Frequency Compensation of the TIA

The small-signal model of the sensor interface consisting of an electrochemical cell and the TIA is shown in Fig. 4(a). A simplified model of the electrochemical cell [Fig. 2(a)] is used for hand calculation purposes. The amplifier is modeled as a single-pole amplifier with an open-loop transfer function $a(s)$ and feedback resistor R_F. The block diagram illustrates the strong coupling between the TIA and electrochemical cell,

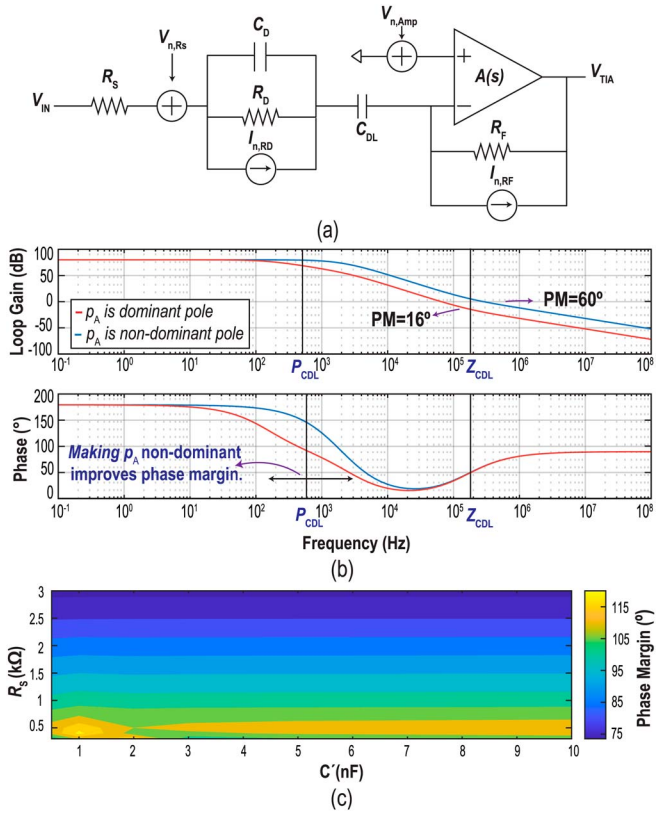


Fig. 4. (a) Simplified schematic of the AFE with sensor model. (b) Bode plot annotated with dominant poles and zeroes. (c) Simulated phase margin across electrochemical cell values ($n = 60$).

with multiple poles and zeros. Given that electrochemical cell impedances are significantly influenced by variables such as the voltage, electrolyte concentration, and electrode surface area, a comprehensive analysis of the stability of this system is crucial.

The loop gain, $L(s)$, and closed-loop voltage gain, $H(s)$, of the block diagram can be derived as

$$L(s) = a(s)\frac{Z_{\text{elec}}}{R_{\text{F}} + Z_{\text{elec}}} \approx \frac{a_0}{1 + {}^{s}/_{p_{\text{A}}}} \frac{1 + sR_{\text{S}}C'}{1 + sR_{\text{F}}C'} \tag{1}$$

$$H(s) = \frac{V_{\text{out}}(s)}{V_{\text{in}}(s)} = \frac{-a(s)R_{\text{F}}}{(1 + a(s))Z_{\text{elec}} + R_{\text{F}}} \approx \frac{a_0 R_{\text{F}} sC'}{\Delta(s)}, \tag{2}$$

where Z_{elec} is the impedance of the electrochemical cell, $\triangle(s)$ is a second-order polynomial, $C' = C_{\text{D}}||C_{\text{DL}}$, and a_{o} and p_{A} are the dc gain and the open-loop pole of the amplifier, respectively. The derivation neglects the pole-zero doublet due to R_{D} as it has a negligible impact on the phase response and assumes $R_{\text{s}} \ll R_{\text{F}}$, which is typical of electrochemical AFEs. A detailed analysis can be found in [31].

The transfer function $H(s)$ confirms the system's bandpass behavior. The double-layer capacitance, C_{DL}, is large and generates a pole in $L(s)$ at a few Hz and a zero at higher frequencies [Fig. 4(b)]. The conventional p_{A}-dominant pole approach to mitigate load sensitivity is unsuitable here for two reasons: 1) It necessitates a large capacitor to realize a pole less than a few Hz (below the pole from C_{DL}), leading to a significant area increase,

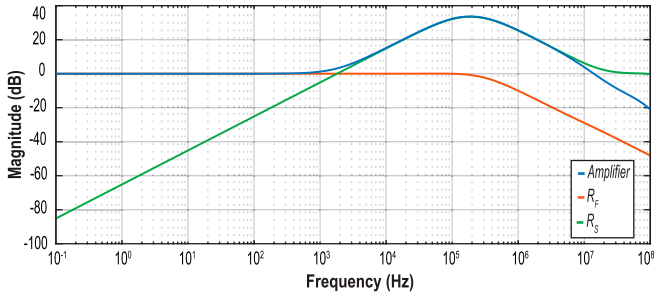


Fig. 5. NTFs of the electrochemical cell and the TIA.

and 2) An additional sizable feedback capacitor around the TIA is needed to counteract the two poles now near dc, further increasing the area. Both factors negatively impact the feasibility of a per-pixel ADC in a biosensor array.

To ensure stability in an area-efficient manner, this work adopts "load compensation" [31], which uses the electrode impedance (*i.e.*, C_{DL}) to realize the dominant pole of the system. There is, however, a corner case where the solution resistance is large ($R_{\text{s}} > 1$ kΩ), making the pole and zero from the electrochemical cell closely spaced, leading to poor stability. To deal with this case, a small Miller capacitor C_{m} is added inside the TIA to separate the non-dominant poles. Note that this pole is normally *not* the dominant pole, so it is not strictly Miller compensation. To further make the system resilient to electrochemical cell variation, an extra zero is added using a small feedback capacitor connected between the input and output terminals of the R-TIA. Fig. 4(c) plots the phase margin of the design across variations of electrochemical cell parameters, demonstrating that the compensation technique is robust. Note that variations in cell parameters were simulated to ensure the phase never crosses below 0°, confirming that phase margin is an appropriate measure of stability and its traditional definition is applicable.

C. Noise Analysis

To design a noise-efficient AFE for high sensitivity, it is important to understand the relative noise contributions. The noise transfer functions (NTFs) were derived for each noise source as

$$NTF_{\text{AMP}} \approx H(s)\frac{1 + sC'(R_{\text{F}} + R_{\text{S}})}{sC'R_{\text{F}}} \tag{3}$$

$$NTF_{\text{R}_{\text{F}}} = \frac{a(s)R_{\text{F}}}{1 + a(s)} \tag{4}$$

$$NTF_{\text{R}_{\text{S}}} = H(s). \tag{5}$$

The electrochemical cell noise can be modeled using the Johnson–Nyquist formulation (*i.e.*, $4k_{\text{B}}TR_{\text{s}}$) for non-faradaic electrodes [32]. Due to the typically high value of R_{D}, the resulting noise current is minimal, rendering its contribution negligible in this context. Furthermore, the parasitic capacitances from the electrostatic discharge (ESD) protection diodes and electrode are small enough to contribute negligibly to the total capacitance at that node. Fig. 5 shows that NTF_{AMP} exhibits gain peaking due to C' within the relevant frequency range,

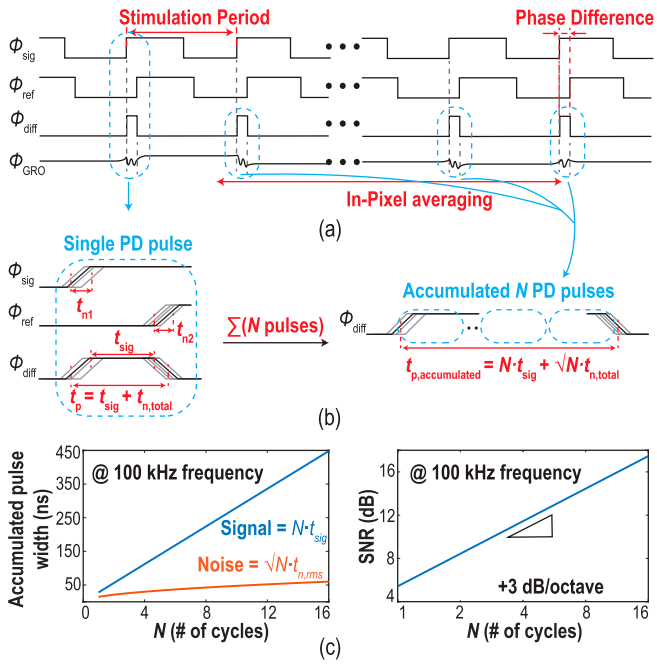
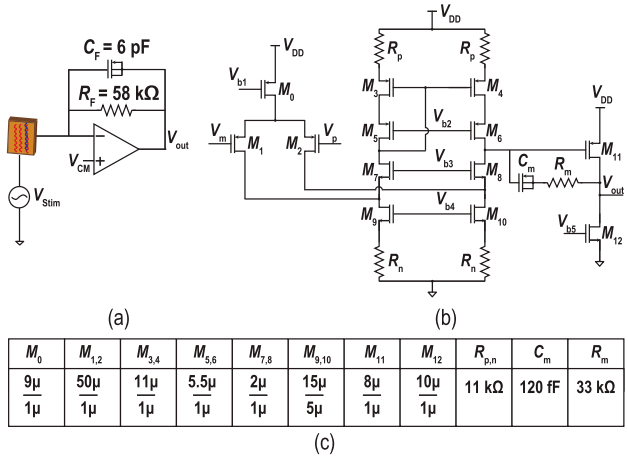


Fig. 6. (a) Waveforms showing the concept of phase difference averaging by accumulating several PD pulses. (b) A single PD pulse with jitter before and after accumulation, and (c) simulation results showing the SNR increasing by 3 dB with every 2× integration time.



M_0	$M_{1,2}$	$M_{3,4}$	$M_{5,6}$	$M_{7,8}$	$M_{9,10}$	M_{11}	M_{12}	$R_{p,n}$	C_m	R_m
9µ / 1µ	50µ / 1µ	11µ / 1µ	5.5µ / 1µ	2µ / 1µ	15µ / 5µ	8µ / 1µ	10µ / 1µ	11 kΩ	120 fF	33 kΩ

(c)

Fig. 7. (a) Schematic of the R-TIA. (b) Circuit implementation of the amplifier and (c) sizing.

highlighting the critical role of the amplifier design. Although NTF_{Rs} closely follows NTF_{AMP} in this frequency range, its noise contribution is negligible due to the low value of R_s. Moreover, the noise from R_F remains below that of the amplifier for modest values (as applied in this design), establishing the amplifier as the dominant noise source. Lastly, the PD compares the phase of the signal and reference pixels, φ_{sig} and φ_{ref}, translating the noise at the TIA output into jitter in the PD output ($T_{jit,PD}$), which can be calculated as

$$T_{jit,PD} \approx \sqrt{2}\frac{V_{n,tot}}{A_{TIA}\omega_s}, \tag{6}$$

where A_{TIA} is the output swing of the TIA, ω_s is the EIS frequency, and $V_{n,tot}$ is the total integrated noise of the blocks preceding the PD.

D. In-Pixel Averaging

The TDC performs the pulse width to digital conversion of φ_{diff} by turning on the GRO when φ_{diff} is high and gating the oscillator to preserve the phase during the off-state, as shown in Fig. 6(a). The phase change of one stage in the GRO in each stimulation period ($T_{stim} = 1/f_{stim}$) is:

$$\varphi_{GRO} = 2\pi f_{GRO} T_{stim} D, \tag{7}$$

where f_{GRO} is the free-running oscillator frequency, and D is the duty cycle of φ_{diff}. Therefore, D can be obtained by quantizing and normalizing φ_{GRO} to f_{GRO}, and the quantized phase of the GRO provides inherent first-order noise-shaping since φ_{GRO} is an integrated version of φ_{diff} when the GRO is not reset [30].

Each PD pulse contains the desired phase difference, t_{sig}, due to the sensor impedance change but is corrupted by noise, $t_{n1,2}$, from the sensor, R-TIA, and other circuitry that is subsequently converted into jitter, as shown in Fig. 6(b). Multiple PD pulses accumulate in the GRO to improve the SNR. The accumulation of N PD pulses enhances the SNR by 3 dB for each doubling of the integration time, assuming the phase noise is spectrally white within the frequency range of interest. The SNR improvement relaxes the TIA and TDC noise requirements since it is no longer necessary to lower the phase noise of a single pulse down to sub-ns. As simulated in Fig. 6(c), with a signal equivalent to 1° at a 100 kHz stimulus frequency and 14 ns_{rms} of jitter, the SNR increases from 5.4 to 17.4 dB by increasing the integration time of the TDC from 10 µs (a single PD pulse) to 160 µs (16 PD pulses).

IV. Circuit Implementation

A. Electrodes

The working electrode (WE) is realized using the topmost metal (metal 6) and placed above the TIA. The electrode has a 100 × 100 μm^2 passivation opening, which is subsequently post-processed to create gold-plated electrodes. Metal layers 4 and 5 shield the electrode from the rest of the circuitry. The electrode size was chosen to be large enough to be functionalized using a robotic spotter. On-chip ESD protection was implemented in each pixel using two p+/n-well diodes (0.2 μm^2) between the electrode and V_{DD} or ground, respectively. The connection between the electrode and the input of the R-TIA was made through a 160 Ω resistor and another pair of identical diodes connected to V_{DD} and ground.

B. R-TIA

The R-TIA was implemented using a two-stage, folded-cascode amplifier with a ~58 kΩ feedback resistor, R_F, and a 6-pF feedback capacitor, C_F, as shown in Fig. 7. The µA-level induced current from the electrochemical cell means the TIA output swing is ~200 mV. Using a 1.8-V supply voltage, the PMOS input pair ($M_{1,2}$) is biased in subthreshold saturation for noise efficiency with a g_m/I_D of ~20.5 S/A. The input pair's flicker (1/f) noise is reduced by selecting PMOS transistors and using large devices. Chopping is avoided to prevent the injection

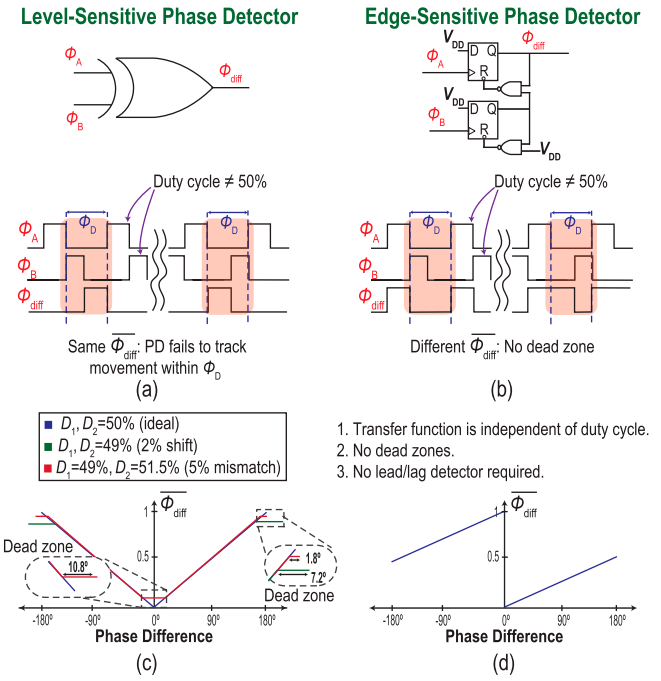


Fig. 8. Schematics and waveforms showing the dead zone of an (a) XOR-PD and (b) DFF-PD. Transfer functions with duty cycle offset and mismatch of an (c) XOR-PD and (d) DFF-PD.

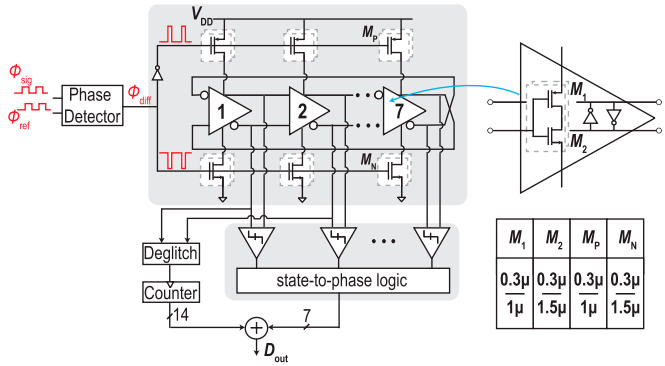


Fig. 9. Schematic of the GRO and phase quantizer.

of switching noise into the WE, which can impact measurement accuracy [33]. The load transistors ($M_{3,4,9,10}$) are biased in saturation and use source degeneration to attenuate the flicker noise. The amplifier's simulated 1/*f* noise corner frequency is ~6 kHz, and the thermal noise floor is 30 nV/$\sqrt{\text{Hz}}$. The second stage provides a low output impedance to drive the feedback resistor. In simulation, the unloaded dc gain is nominally 104 dB and >89 dB across process corners and temperature.

The amplifier achieves a ~75 MHz unity-gain bandwidth. The small Miller capacitor creates a ~15 kHz non-dominant pole, which helps to improve the phase margin when R_s is large (*i.e.*, >1 kΩ). Since the top metal layer is used as an electrode, the design excludes metal-insulator-metal (MIM) capacitors, and the congested interconnect makes using metal-oxide-metal (MOM) difficult. Consequently, all capacitors are implemented using moscaps. The amplifier consumes 140 µW, with less than 25% used in the bias circuitry.

C. Phase Detector

The phase of the pixel, φ_{sig}, is compared with the output of the reference pixel, φ_{ref}, to calculate the phase shift of the electrochemical cell, φ_{diff}. An XOR-based PD, a commonly used phase detector in polar mode-based EIS systems [21], [24], [27], stands out for its simplicity as a single logic gate. The average value of its output is linearly related to the phase difference between the two inputs. However, due to its inability to differentiate between rising and falling edges, the XOR gate is sensitive to variation in the input duty cycle, leading to a degradation in output linearity. Fig. 8(a) illustrates this through two input signals, φ_A and φ_B, with non-50% duty cycles, D_A and D_B, respectively. Any phase change of φ_B within the overlap region, φ_D, cannot be captured by the XOR-PD, making it a 'dead zone' in the output characteristic curve, as shown in Fig. 8(a) and 8(c). The dead zone's location, either near 0, π, or both, depends on the polarity of the duty cycle error and mismatch. Deviation in the duty cycle (*D*-50%) is directly related to the width of the dead zone. Circuit non-idealities and PVT variation in the common-mode-setting self-biased inverter can cause a shift in the duty cycle, while mismatch leads to disparities in the duty cycles, D_A and D_B. This reduced the linear range of [27] and made it highly sensitive to operating conditions.

Ref [34] uses pulse generators and an S-R latch for the intended outcome yet lacks measurement results or discussion on PVT sensitivity. Inserting a divide-by-2 DFF-based clock divider before the XOR gate to rectify the input signal duty cycle does not address the problem, as it introduces additional phase wrapping every quarter cycle, further complicating the phase output unwrapping process. Other duty-cycle correction circuits [35], [36] were considered but are resource-intensive compared to the DFF-based phase detector.

To resolve this issue efficiently regarding power and area, we used a duty-cycle insensitive DFF-based PD, a prevalent phase/frequency detector circuit found in type-II PLLs [37], modified for single-ended output, as shown in Fig. 8(b). It is an edge-triggered sequential state machine that avoids dependence on the duty cycle of the inputs [Fig. 8(d)]. The DFF-based PD is mismatch and PVT tolerant, a critical feature for arrayed applications where the reference may be distant from the signal pixel. Unlike charge-pump-based PLLs that focus on the average value of the output differences, the PD is single-ended to avoid additional circuits for interfacing with the TDC. The edge-triggered nature of the DFF-based PD yields a monotonic transfer function, facilitating the differentiation between phase leading or lagging between reference and signal pixels. This also eliminates the lead/lag detector [21], saving an extra output bit.

D. TDC and Digital Interface

Fig. 9 shows the TDC implementation using a 7-stage pseudo-differential GRO to balance noise and power trade-off with φ_{diff} as the gating signal. Each stage is a latch-based delay cell selected for its superior 1/*f* noise performance. The GRO was sized such that the leakage current introduces negligible error in the off-state [38]. Simulation demonstrates that the GRO output decreases by

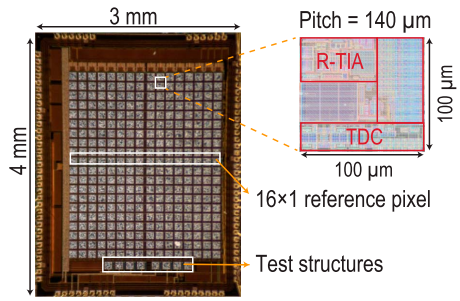


Fig. 10. Annotated chip micrograph.

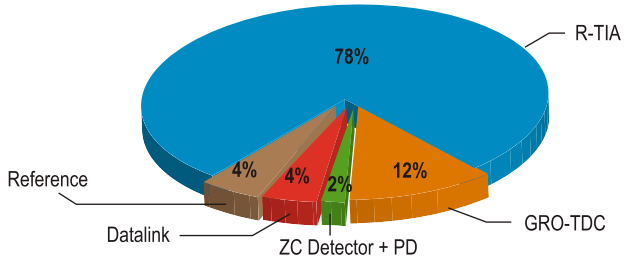


Fig. 11. Power distribution under worst-case (maximum f_{stim}).

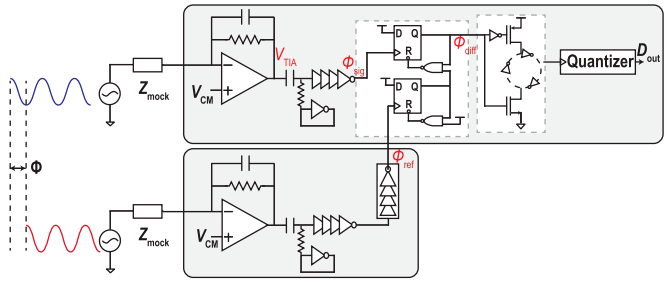


Fig. 12. Measurement setup for characterization.

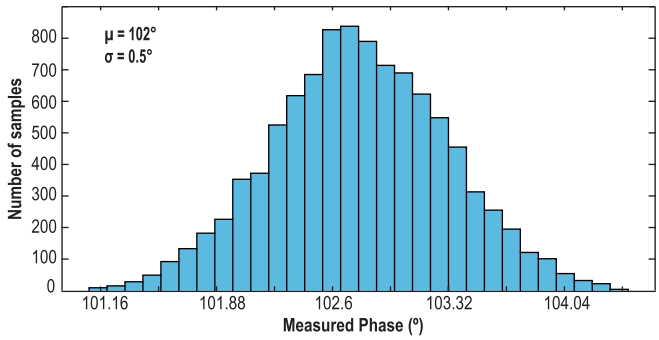


Fig. 13. Measured noise of a single cycle of φ_{diff}.

14.4% (134 mV/ms) in the worst-case scenario (5 kHz input). The post-layout free-running GRO frequency is ∼10 MHz, with a 3σ variation of 10.43% across chips and <1% across pixels within the same chip. The GRO converts the duty cycle of φ_{diff} to the phase domain, φ_{GRO}, for quantization, where the phase is stored as a voltage on the parasitic capacitance (∼12 fF) at the output node of each stage when the GRO is off.

The phase is digitized using a coarse and fine structure where a 14-bit ripple counter increments every 2π rad phase change of φ_{GRO}. Measuring the ring oscillator state using clocked sense amplifiers adds $\pi/7$ fine quantization levels. The GRO output is passed through a deglitch circuit before the counter to avoid double-counting oscillator transitions. The counter was designed for a 10 ms integration time without overflowing. The sense amplifiers are implemented with dynamic comparators with a preamplifier [39]. The preamplifier reduces the kickback noise of the latch. In simulation, it was found that the worst-case kickback was 107 mV due to the small GRO capacitance. The sense amplifier clock was thus synchronized with the readout frequency of f_{stim}/N rather than f_{stim} to further minimize kickback noise to the GRO by reducing the error injecting into GRO output per cycle.

The combined coarse and fine data from the counter and the latch conversions provide a 21-bit digital output for each pixel. The array is read out using an SPI bus, where the outputs of the 16 pixels in each row are concatenated (336 bits) to balance the number of output ports (16) and readout time. Thus, the clock frequency for the SPI is 336× the readout rate.

V. Measurement Results

This design was fabricated in a 180 nm CMOS process with a 1.8 V supply, occupying 3 × 4 mm^2. As shown in Fig. 10, there are 16 columns, each with 19 signal pixels and one shared reference pixel in the middle. Each pixel has an active area of 140 × 140 µm^2 with a 100 × 100 µm^2 electrode. A test structure at the bottom of the chip, consisting of a copy of the signal and reference pixel, was used for characterization. The measured power consumption per channel was 197 µW. The power distribution shown in Fig. 11 corresponds to the simulated power at f_{stim} = 100 kHz for a full-scale φ_{diff} of π. The contribution of the reference pixel, P_{ref}, is accounted for by adding $P_{ref}/19$ to each signal pixel. Of the 197 µW power consumption/channel, ∼78% of the power is consumed by the R-TIA, while the GRO-TDC and datalink take 16%.

A. Electrical Characterization

The electrical performance was characterized using test structures on the chip with a mock electrochemical cell as a substitute for both signal and reference electrodes, as shown in Fig. 12. The equivalent impedance was matched with the theoretical values for a gold-plated 100 × 100 µm^2 electrode (the same as the on-chip electrodes) in 4× SSC (C_{dl} = 4.5 nF, R_d = 10 MΩ, R_s = 1 kΩ, C_d = 3 nF). The noise of a single cycle of φ_{diff} was characterized by providing a constant 90° phase shift between the reference and a signal pixel at a test frequency of 100 kHz. The output jitter of φ_{diff} was measured using a frequency counter (Keysight 53220A) and input-referred to the equivalent phase error. Fig. 13 shows a histogram of the measured phase with an RMS noise of 0.5° around a mean value of ∼102°. The 12° phase offset (330 ns) is due to the designed delay chain in the reference pixel (simulated = 10.45°). Fig. 14 demonstrates that the in-pixel averaging technique provides an SNR improvement of +10 dB per 10× integration time. This design is thermal noise limited up to 100 cycles (1 ms), after which the R-TIA's 1/f noise dominates.

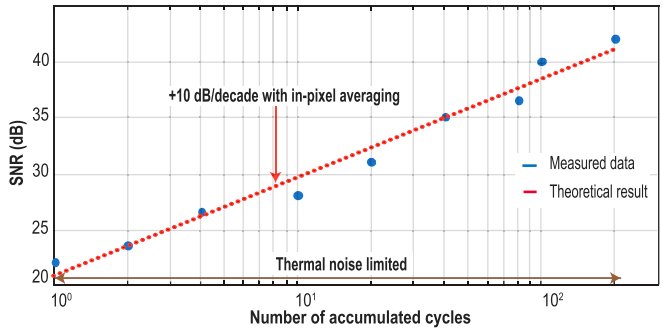


Fig. 14. Measured SNR improvement with the in-pixel averaging by accumulating multiple cycles.

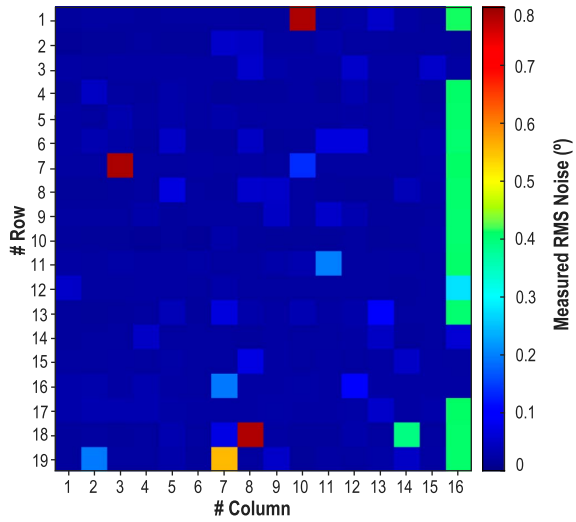


Fig. 15. Heatmap of the GRO-TDC noise.

The entire 19 × 16 array was analyzed to characterize the noise of the GRO-TDC across all pixels. This was tested using unprocessed electrodes, meaning the TIA input was weakly grounded through parasitic capacitance. With the PD output pulled high, this measurement captures only the GRO-TDC noise. The noise of each pixel was averaged over 200 cycles, and the resulting heatmap is presented in Fig. 15. The GRO-TDC noise, averaged across a 19 × 16 pixel array, is 0.1°_{rms}.

The linearity was measured by applying two sinusoids with a phase shift between the reference and signal pixel using an arbitrary function generator (Tektronix AFG3022C) at 100 kHz. Fig. 16 shows the transfer function over the phase full-scale range of 180° with an offset of 9.8° (∼250 ns) matching the designed delay chain in the reference pixel and an RMS linearity error of 0.035%. The efficacy of the proposed edge-based phase detector is compared with that of a level-sensitive phase detector in Fig. 17 by comparing transfer functions at three test frequencies (50, 100, and 500 kHz). Fig. 17(a) shows the presence of dead zones in [27], degrading the linearity, which were eliminated in this design [Fig. 17(b)].

B. Electrode Fabrication

Each sensor incorporates an exposed top aluminum layer within the standard process (effectively a bond pad). However,

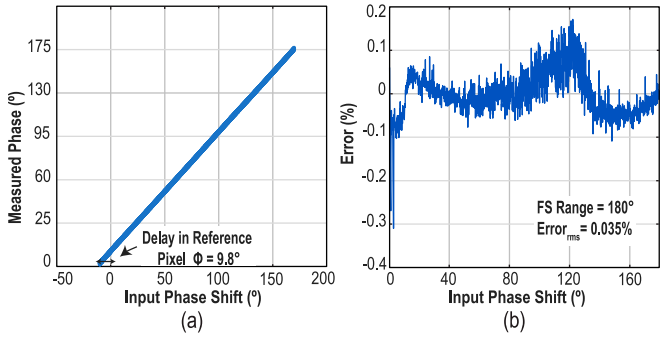


Fig. 16. Measured pixel (a) transfer function and (b) linearity.

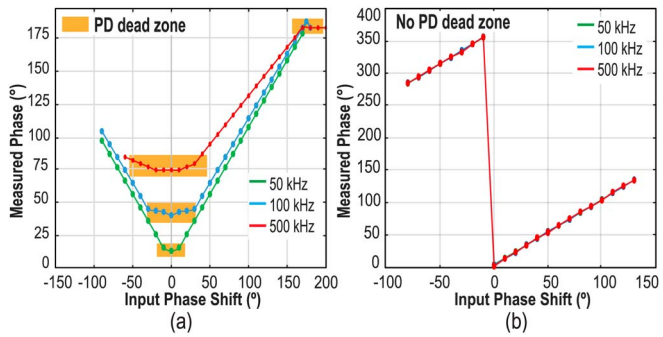


Fig. 17. Comparison of the transfer functions of (a) level-sensitive [27] and (b) edge-sensitive PDs.

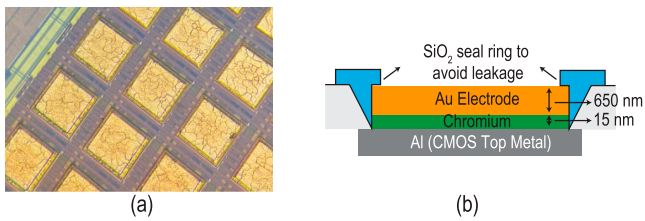


Fig. 18. (a) Image of gold electrode array. (b) Cross-section drawing of post-processed CMOS electrode.

aluminum is not electrochemically compatible, thus requiring a more stable metal. Gold (Au) was chosen as it is easy to immobilize DNA through Au-thiol bonding. A film stack consisting of a 15 nm chromium (Cr) adhesion layer followed by 600 nm of Au was sputtered (Denton Discovery 635) and selectively removed using a liftoff process. Sputtering was used rather than an electroless plating process (ENIG), making the electrodes more durable and stable than the previous iteration [27]. During initial testing, it was discovered that this approach is susceptible to fluid incursion near the electrode edges, corroding the underlying aluminum metallization. We could have etched the aluminum and deposited Au above the tungsten metal 5-6 vias, as in [40], but developed an alternative approach where a SiO_2 ring was deposited around each electrode, enhancing containment and protection, as shown in Fig. 18. Using this approach, the electrodes were stable in a phosphate-buffered saline (PBS) solution for more than 24 hours without any visible or electrical signs of corrosion.

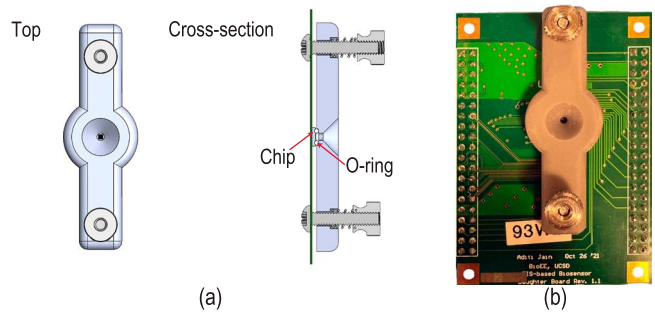


Fig. 19. (a) Rendering of flow cell and (b) photograph of assembled flow cell.

C. Flow Cell

We used chip-on-board packaging where the die is directly wire-bonded to a printed circuit board (PCB). The PCB incorporates fiducials to position the die properly for the flow cell. The wire bonds were partially encapsulated, leaving the electrodes exposed. An open-well flow cell for electrochemical testing was designed using SOLIDWORKS and 3D printed (FormLabs 3B), as shown in Fig. 19. It has a 150 µL well above the electrode array to hold the sample. An o-ring is sandwiched between the chip and the flow cell to protect the wire-bonding encapsulant from the solution [see Fig. 19(b)]. Knurled nuts and springs control the compression force and ensure adequate sealing. Holes on the PCB are used to align the flow cell. The reference electrode is attached from the top, allowing various materials to be used.

D. Biological Measurements

The functionality of the circuitry and post-processed electrodes was confirmed through the measurement of phase changes associated with varying ionic strength, C_{buf}. Modifying C_{buf} induces changes in the electrode impedance where R_s has an inverse relationship with the concentration. At low ionic concentrations, C_{dl} is approximately proportional to the square root of the concentration due to the increase in the Debye length [41]. Thus, at 100 kHz, the phase is

$$\phi_{\text{elec}} \approx 90^\circ - \tan^{-1}\omega R_s C_{\text{dl}} \propto \sqrt{C_{\text{buf}}}. \tag{8}$$

The experiment employed a 2-electrode configuration with the on-chip electrode used as the working electrode and a silver wire as the reference electrode [Fig. 20(a)]. Starting with an initial sample of 85 µL of 1× SSC, small volumes of 20× SSC were serially added to increase the buffer strength from 3× to 5×. Fig. 20(b) shows the measured real-time change in phase. The transient signals coincide with the fluid additions as the ions diffuse and C_{dl} is perturbed before settling to the nominal values. These data closely agree with the theoretical results according to (8), both offset-corrected.

Before running assays on the chips, experiments were conducted to determine the optimal experimental parameters (*i.e.,* the EIS frequency and dc bias for the particular redox reporter concentration and buffer system). Ideally, these measurements should be performed on the same electrodes, but we did not have on-chip electrodes available to measure with an external potentiostat, so we used gold screen-printed electrodes (DropSens 220AT) as a proxy. Cyclic

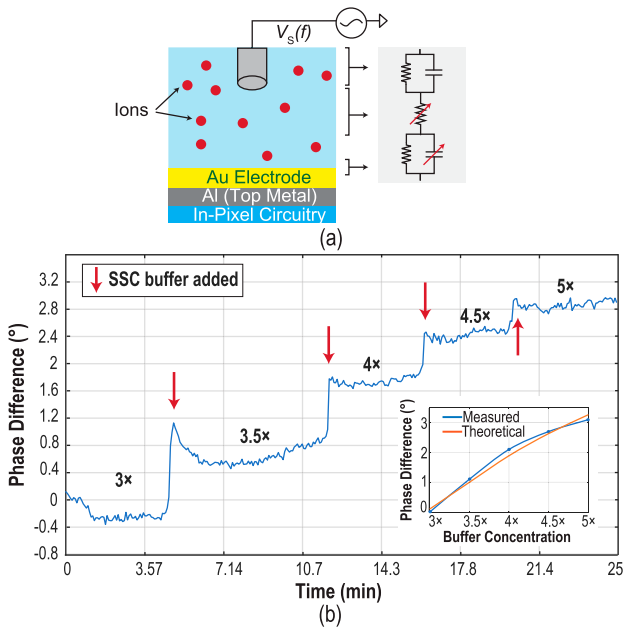


Fig. 20. Phase change due to increasing SSC buffer concentration on an individual sensor ($n = 1$).

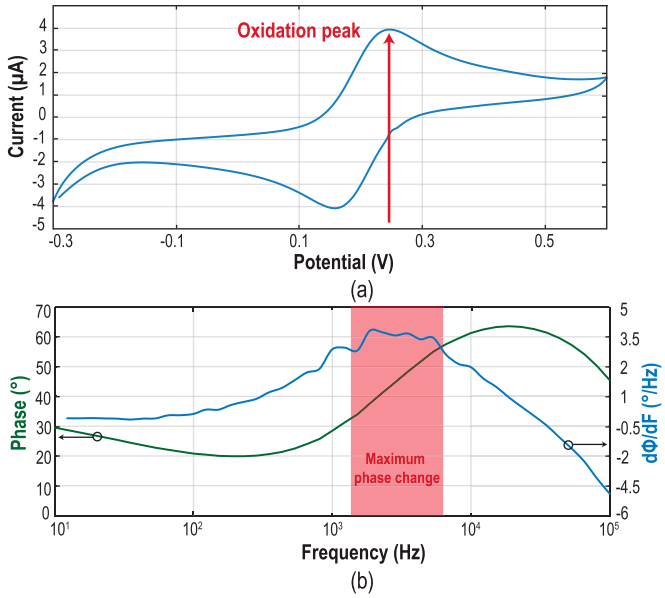


Fig. 21. Measured (a) voltammogram and (b) phase on a gold screen-printed electrode in 5 mM ferri-/ferrocyanide and 5× SSC.

voltammetry (−0.3 to 0.6 V, 10 mV step, and 50 mV/s scan rate) measurements were collected from an unfunctionalized electrode in 5× SSC with 5 mM of ferri-/ferrocyanide ($[Fe(CN)_6^{3-/4-}]$) using an off-the-shelf potentiostat (PalmSens 4). It was found that the optimal dc bias for EIS experiments was 250-mV to bias the cell at the oxidation peak [see Fig. 21(a)]. Next, an EIS measurement (10 mV amplitude, 10–100 kHz) using this dc bias was performed on the cell. As shown in Fig. 21(b), the maximum phase change occurred at 5 kHz. These parameters were used for all subsequent measurements.

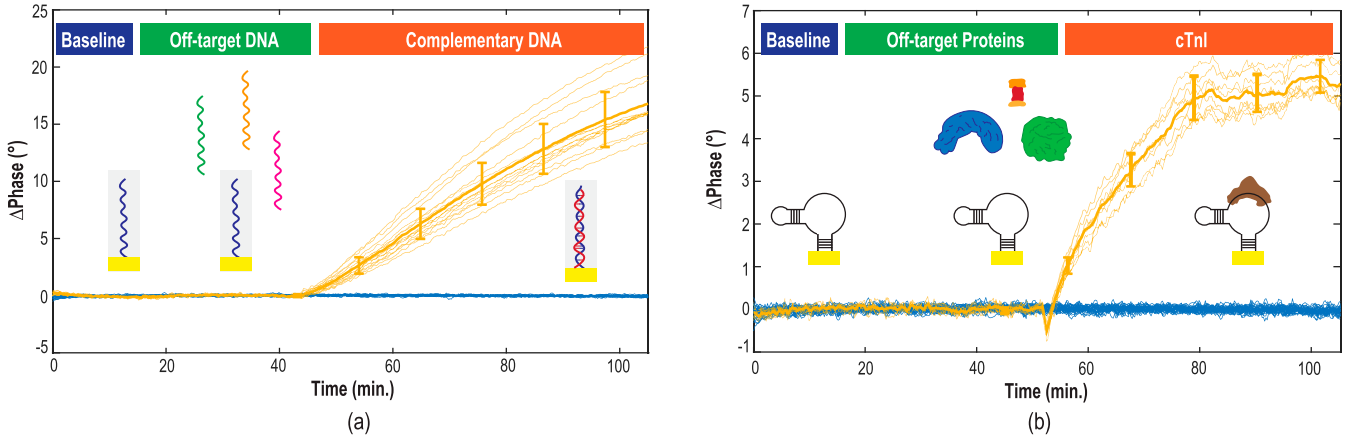


Fig. 22. Measured real-time (a) DNA hybridization and (b) aptamer-antigen binding. Error bars represent $\pm 1\,\sigma$.

TABLE I
PERFORMANCE SUMMARY AND COMPARISON TO THE STATE-OF-THE-ART

Parameter	[15]	[20]	[21]	[22]	[24]	[34]	[43]	[44]	[45]	This Work
Technology [nm]	130	350	500	130	350	180	180	180	250	**180**
Supply [V]	1.2	3.3	3	0.6	3.3	0.9	–	1.5	2.5	**1.8**
On-chip electrodes?	Yes	Yes	No	Yes	No	No	No	No	No	**Yes**
Num of sensors	64	100	–	12	–	–	–	–	–	**320**
Num of readout channels	16	100	1	12	1	1	1	1	1	**320**
Area/channel [μm^2]	60,000	10,000	60,000	4,000	70,000	400,000	35,000	300	48,000	**19,600**
Power [mW]	0.67	84.5	0.006	0.0146	0.32	28	0.395	0.016	<10	**63**
Power/channel [μW]	42	845	6	0.05	320	28000	220	16	<10,000	**196**
On-chip ADC?	In-Pixel	No	Yes	In-Pixel	In-Pixel	In-Pixel	In-Pixel	No	Yes	**In-Pixel**
Frequency range [Hz]	$0.1-10^4$	$10^2-5\times10^7$	$0.1-10^4$	$1-5\times10^3$	$10^{-4}-10^5$	$100-10^6$	$5\times10^{-4}-5\times10^4$	–	$10^3-2\times10^6$	**$5\times10^3-10^6$**
Quadrature signal source required?	Yes	Yes	Yes	Yes	No	No	No	No	Yes	**No**
Magnitude error [%]	–	–	0.32% @ 10 Hz	–	0.28% @ 10 kHz	2.5%	0.19%	–	1%	–
Phase error [%]	–	–	2.7% @ 1 kHz	–	0.12% @ 10 Hz	2.2°	0.08%	0.1% for Res, 0.4% for Cap	1.3°	**0.05°/0.035% @ 100 kHz**

Next, we functionalized the chip sensor electrodes with a DNA aptamer. Briefly, the sensor surface was cleaned by washing with ultra-pure water and then isopropyl alcohol, followed by UV-Ozone (UVOTECH Helios 500) treatment for 10 minutes to remove any organic residues. 20 μL of 1 μM thiolated troponin aptamer (5′→3′: Thiol-C6-TTT TTT CGT GCA GTA CGC CAA CTT TTC TCA TGC GCT GCC CCT CTT) [42] reduced with tris(2-carboxyethyl)phosphine (TCEP) was spotted on a subset of the sensors and incubated overnight at 4°C. The chips were subsequently incubated with 20 μL of 1 mM 6-mercapto-1-hexanol (MCH) to block the remaining electrode surface for 30 minutes. After the surface modification, the chips were thoroughly washed with deionized water to remove unbound molecules and stored at 4°C for up to one week.

We then measured DNA hybridization using the chip where 16 sensors were functionalized with the aptamer. The phase was read continuously for the duration of the experiment (105 minutes). Initially, 100 μL of 5 mM ferri-/ferrocyanide in 5× SSC buffer was added to the flow cell, and the phase was recorded for 15 minutes to observe the baseline. Next, 1 μL of 100 μM off-target DNA (AAT AGT CCC ACA ATT GAC GT) was added to achieve a final off-target concentration of 1 μM and measured for 30 minutes. Finally, an additional 1 μL of 100 μM complementary DNA (AAA ATG AGA AAA GTT G) was added, and measurements continued for another 60 minutes. The phase is plotted as the difference from the starting value ($\mu = 67.9°$). As shown in Fig. 22(a), the baseline signal is stable with minimal drift and no response to the off-target DNA. After adding complementary DNA, a classic binding curve was observed ($\mu = 16.8°$). The sensor-to-sensor variation ($\sigma = 2.4°$) is likely due to non-uniform probe attachment since the sensors were hand-spotted. As a final confirmation that the signal was due to specific binding, we added 10 μL of 8 M urea

to denature the DNA. The sensors functionalized with DNA subsequently relaxed back to their initial phase over 30 minutes (data not shown), confirming that the interaction was specific and due to the DNA-DNA interaction.

We repeated a similar experiment, however, this time with cardiac troponin I (cTnI) antigen (Abcam ab283299). The sensors were prepared similarly. A baseline signal was recorded in 100 µL of 5 mM ferri-/ferrocyanide and 1× PBS for 15 minutes. Next, 5.3 µL of 1 mM bovine serum albumin (BSA) was spiked into the flow cell for a final concentration of 50 µM and measured for 30 minutes. Then, cTnI was added to achieve a final concentration of 250 pM and measured for 60 minutes. Fig. 22(b) shows the measured real-time plot where minimal non-specific binding occurs during the BSA phase, and a specific response due to the aptamer-antigen interaction ($\mu = 5.3°$) was observed.

While these experiments demonstrate the ability to perform DNA and antigen assays on this chip, they are insufficient to assess parameters such as the limit of detection, dynamic range, and reproducibility. Furthermore, comparing this technique with classical EIS (*i.e.*, magnitude and phase) would be interesting, but we cannot measure this with the current circuits and do not have on-chip electrodes without the readout circuitry. Future work will focus on better assessing the biological performance of this approach.

E. Comparison to the State-of-the-Art

Table I compares the performance of this work with that of recently published EIS CMOS biosensors. This work achieves the highest pixel density and one of the smallest pixel areas with an in-pixel analog front-end and quantizer. Leveraging phase-only polar modulation and mostly digital circuitry, it achieves a state-of-the-art phase error of 0.035% (0.05°), which is >2× better than current benchmarks, enabling highly sensitive bioassays.

VI. Concluding Remarks

This work reports a 16 × 20 electrochemical CMOS biosensor array employing polar mode detection using a phase-only EIS method to track binding events. Within each pixel (140 × 140 μm^2), the phase change is measured using a load-compensated TIA, edge-sensitive phase detector, and a first-order noise-shaping time-to-digital converter, eliminating the need for quadrature signal analysis. This predominantly digital design offers 10 dB noise reduction for every 10× additional data points through in-pixel averaging. It achieves 0.035% RMS error using a duty-cycle insensitive phase detector and one of the smallest areas per pixel with in-pixel quantization.

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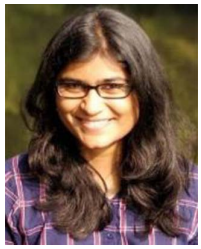

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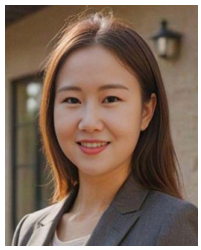

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