An ECG Chopper Amplifier Achieving 0.92 NEF and 0.85 PEF with AC-coupled Inverter-Stacking for Noise Efficiency Enhancement

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BIO Sensors & Electronics

Outline

- Motivation and Introduction
- Noise Efficiency Enhancement by OTA Stacking
- ECG Amplifier Architecture
- Circuit Implementation
- Simulation Results
- Conclusion

Motivation

World of IoTs and m-Health

↓

Miniaturized Wearable & Implantable Devices

- Automated, remote monitoring
- Early detection/diagnosis

<u>Major Challenges:</u>

- Continuous reliable monitoring via a small integrated unit
- Ultra-low power sensing circuits with long battery life

ECG Acquisition Amplifier

Amplifies weak, low-bandwidth physiological signals → **Power consumption is noise-limited**

Noise Efficiency Factor (NEF) → noise-current trade-off

$$NEF = v_{\mathrm{ni,RMS}} \sqrt{\frac{2I_{\mathrm{tot}}}{V_{\mathrm{T}} 4 k_{\mathrm{B}} T \pi BW}}$$

Power Efficiency Factor (PEF) → noise-power trade-off

$$PEF = NEF^2 \, V_{\mathrm{DD}}$$

I_{tot}: amplifier current, $v_{\mathrm{ni,RMS}}$: input referred noise, BW: bandwidth,
V_{T}: thermal voltage, T: temperature, k_{B}: Boltzmann's constant

Noise Efficiency Limitation

For a differential amplifier if

- only input diff-pair noise
- devices in sub-threshold

κ: gate-coupling coefficient
typically ~ 0.7

Fundamental NEF Limit

$$\boldsymbol{NEF_o = \sqrt{\frac{2}{\kappa^2}} \cong 2.02}$$

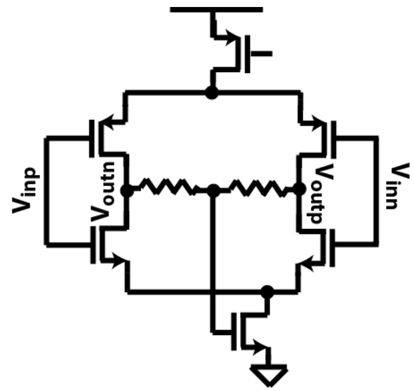
NEF Improvements: Prior Art

- Current Reuse [1]:

$$\boldsymbol{NEF = NEF_o/\sqrt{2}}$$

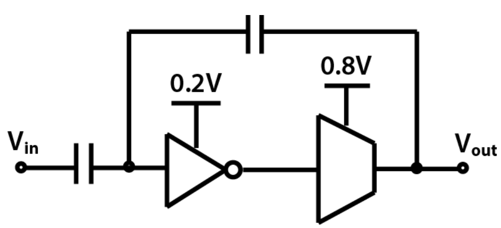
Inverter-based OTA

$$G_{\mathrm{m}} = g_{\mathrm{mn}} + g_{\mathrm{mp}}$$



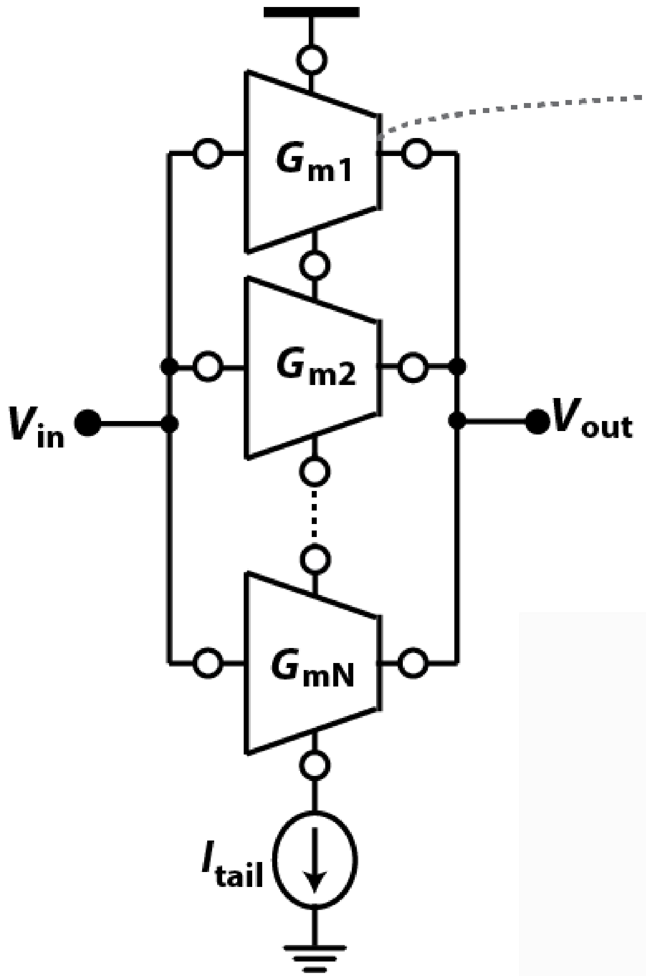
- Dual Supply [2]:

$$\boldsymbol{PEF \cong PEF_o/4}$$

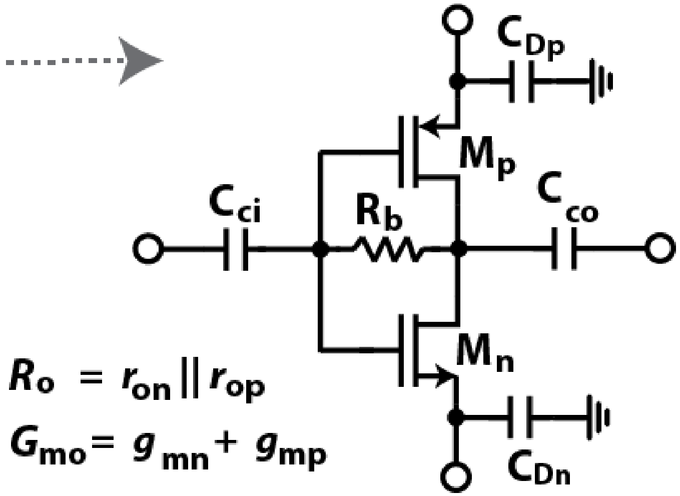


[1] - Chae TNSRE '09
[2] - Yaul ISSCC '16

Proposed Stacked OTA

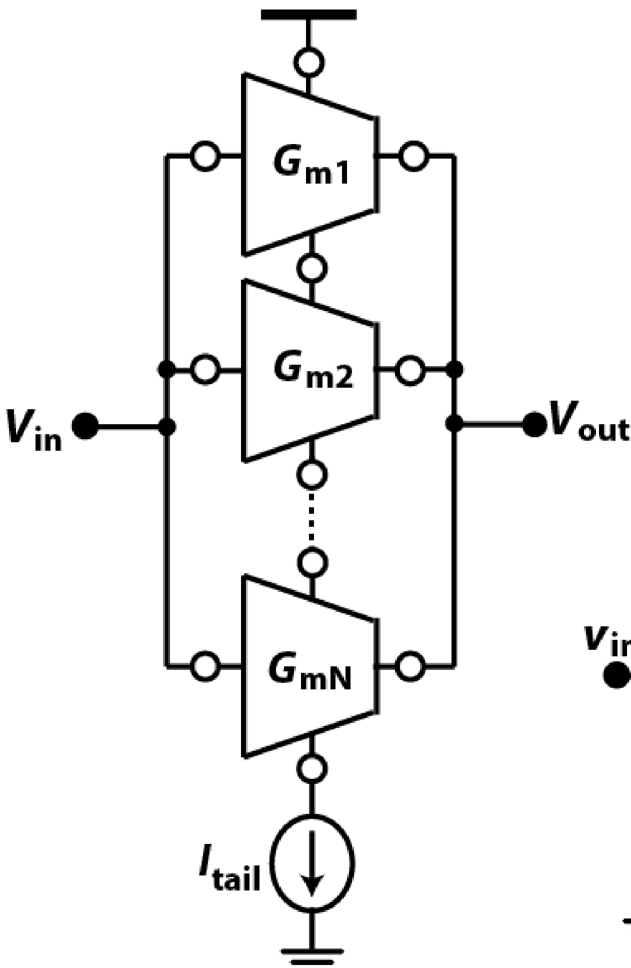


Stacked OTA



AC-coupled inverter-based transconductor

Proposed Stacked OTA



G_m **boosting:** $\boxed{G_m = NG_{mo}}$ [3]

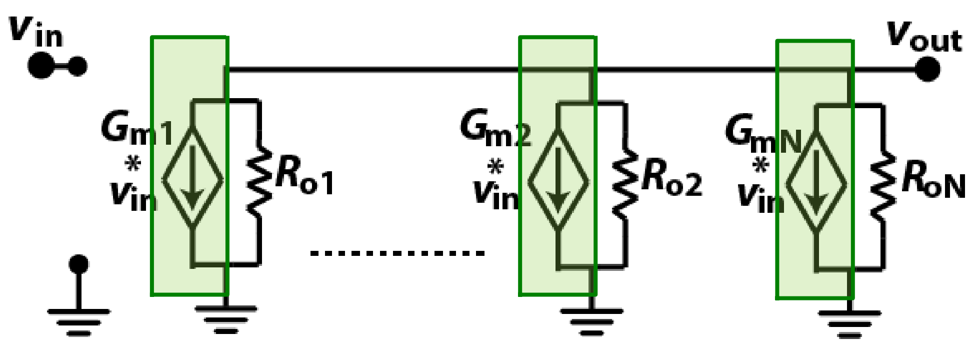
$$R_{out} = R_o/N$$

$$A_v = G_m R_{out} = G_{mo} R_o$$

G_m, R_{out}: compound transconductance, output impedance

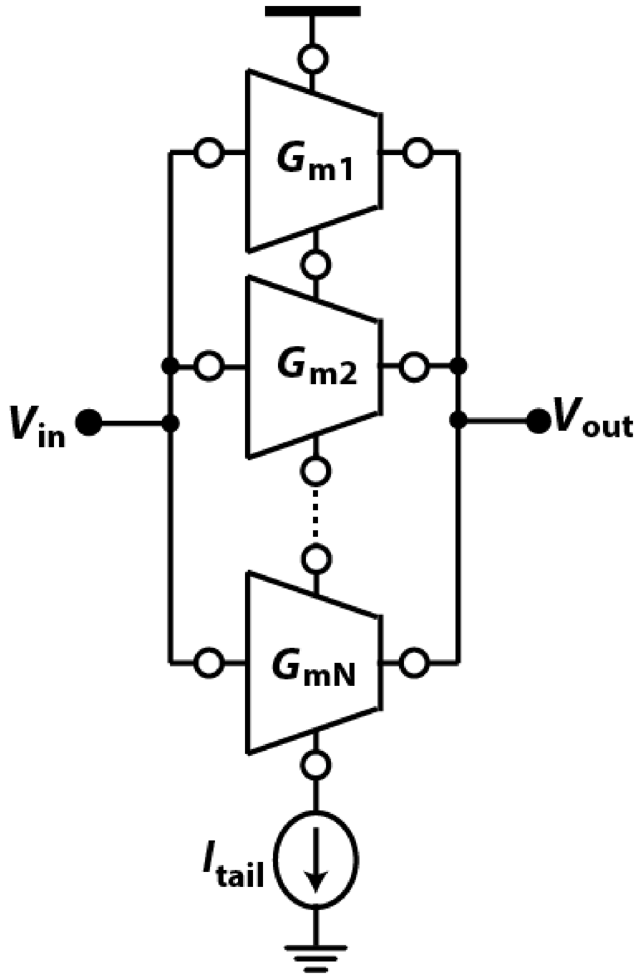
G_{m0}, R_o: single inverter transconductance, output impedance

A_v: OTA Gain



[3] - Iguchi ISSCC’16 (crystal oscillator start-up)

Proposed Stacked OTA



G_m boosting: $\boxed{G_m = NG_{mo}}$

Input-referred noise:

$$\overline{v^2_{\text{ni,thermal}}} = \frac{4k_B T\gamma}{\boldsymbol{N} G_{mo}}$$

$$\overline{v^2_{\text{ni,flicker}}} = \frac{1}{4\boldsymbol{N}f}\left[\frac{K_n}{C_{ox}(WL)_n} + \frac{K_p}{C_{ox}(WL)_p}\right]$$

γ, C_{ox}, K_n, K_p: device parameters $(WL)_{n,p}$: device sizes

$\overline{v^2_{ni}}$: input referred noise PSD

Noise efficiency enhancement:

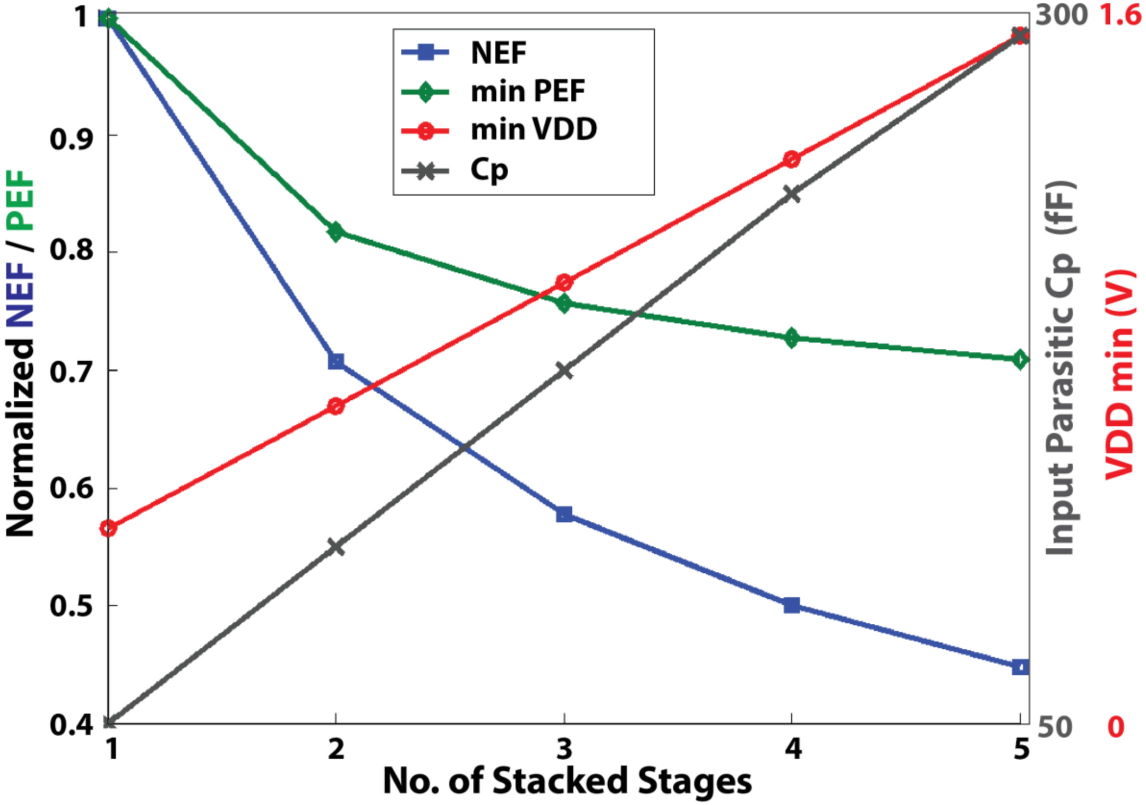
- $\sqrt{2N}$ times improvement in NEF
- $2N$ times improvement in PEF (same V_{DD})

For a differential implementation:

2-stack NEF limit : 1.01
3-stack NEF limit : 0.82

Trade-offs

Inverter-Stacking Trade-offs:



$V_{\mathrm{DD,min}} = NV_{\mathrm{INV}} + V_{\mathrm{tail}}$

$NEF \propto 1/\sqrt{N}$

$PEF_{\mathrm{min}} \propto V_{INV} + V_{\mathrm{tail}}/N$

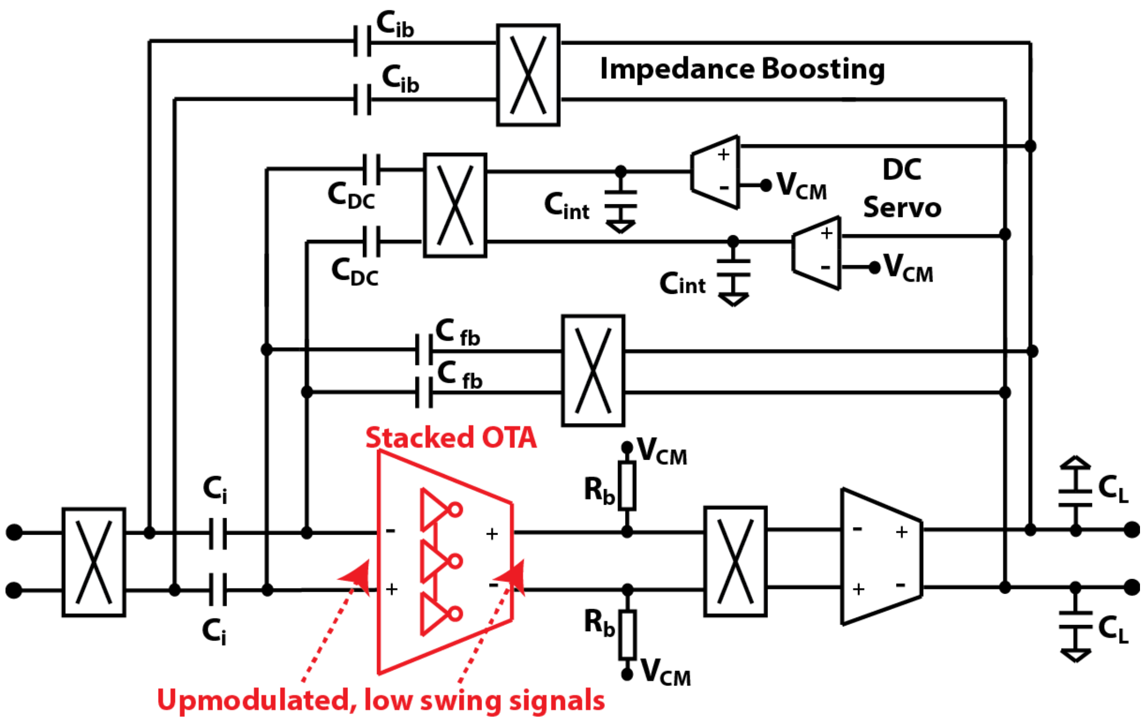
V_{INV}, V_{tail}: voltage headroom for single inverter, tail source

Normalized minimum PEF:

- 2-stack: 0.82
- 3-stack: 0.75
- 4-stack: 0.72

3-stack with 1 V supply is optimal

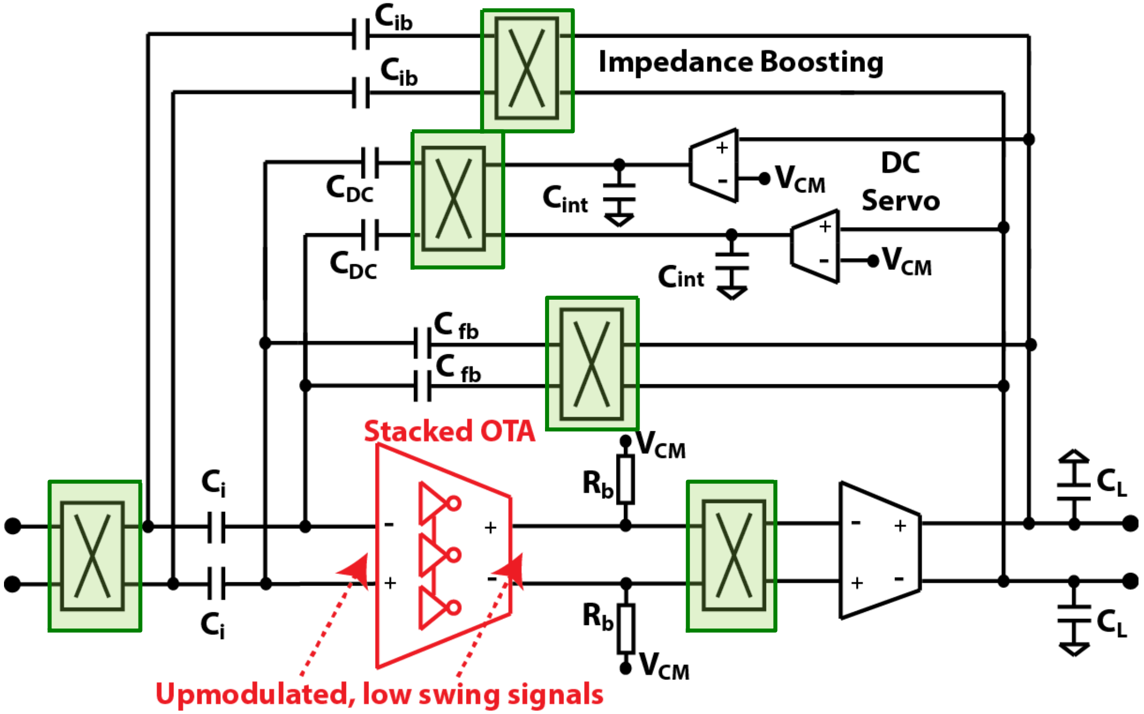
ECG Amplifier Architecture



Key Challenges:

- AC-coupling of low bandwidth ECG (~250 Hz) would require very large capacitors
- Signal swing with OTA stacking is limited

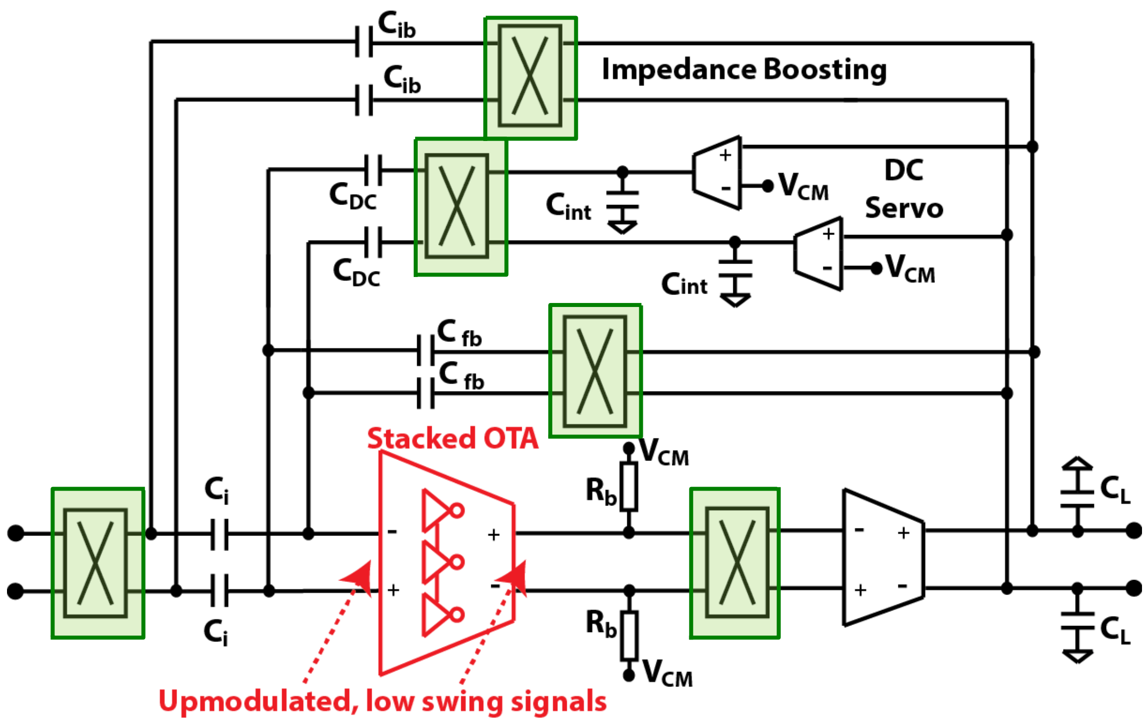
ECG Amplifier Architecture



Key Challenges:

- AC-coupling of low bandwidth ECG (~250 Hz) would require very large capacitors
- Upmodulate to a higher (chopping) frequency → simpler ac-coupling
- Signal swing with OTA stacking is limited
- First stage with low signal swing

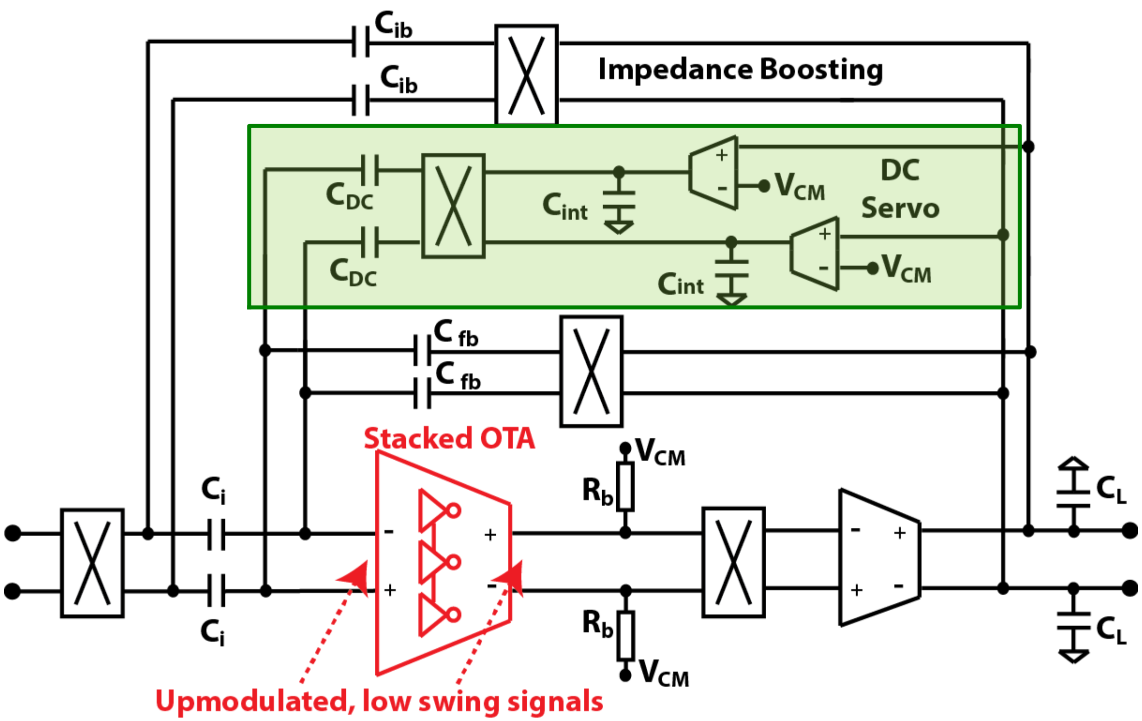
ECG Amplifier Architecture



Other Requirements:

- Low in-band flicker noise
- High CMRR (for 60Hz noise)
- Electrode polarization offset
- High input impedance
- 2^{nd} stage DC bias

ECG Amplifier Architecture



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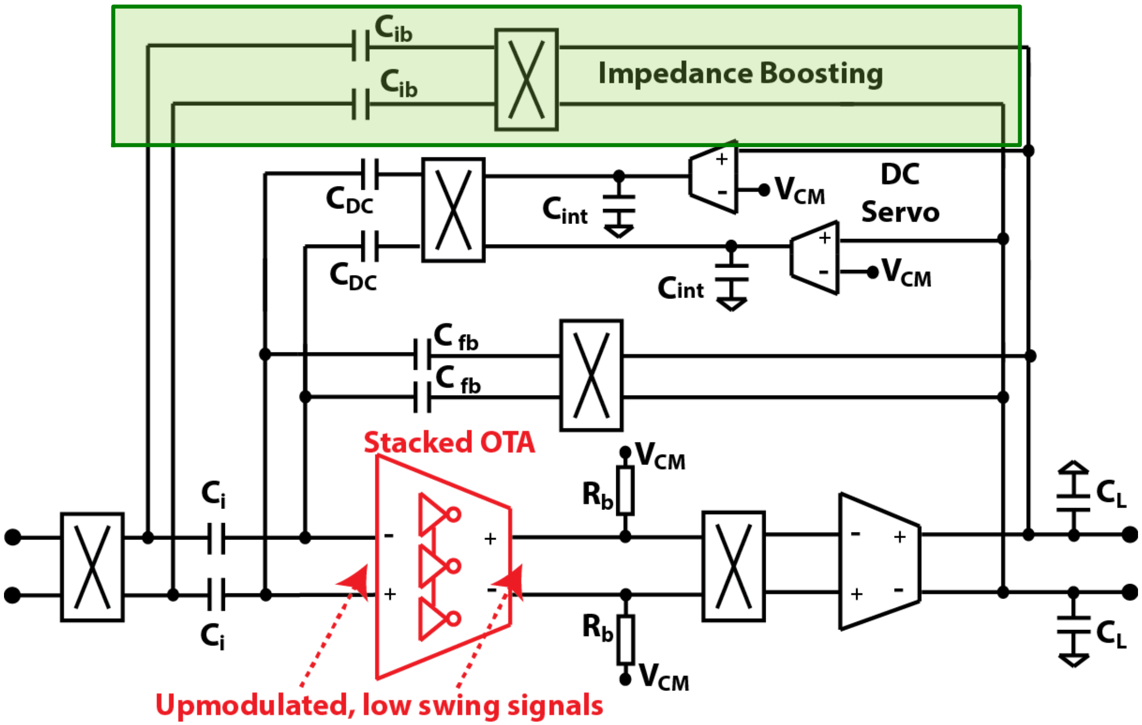

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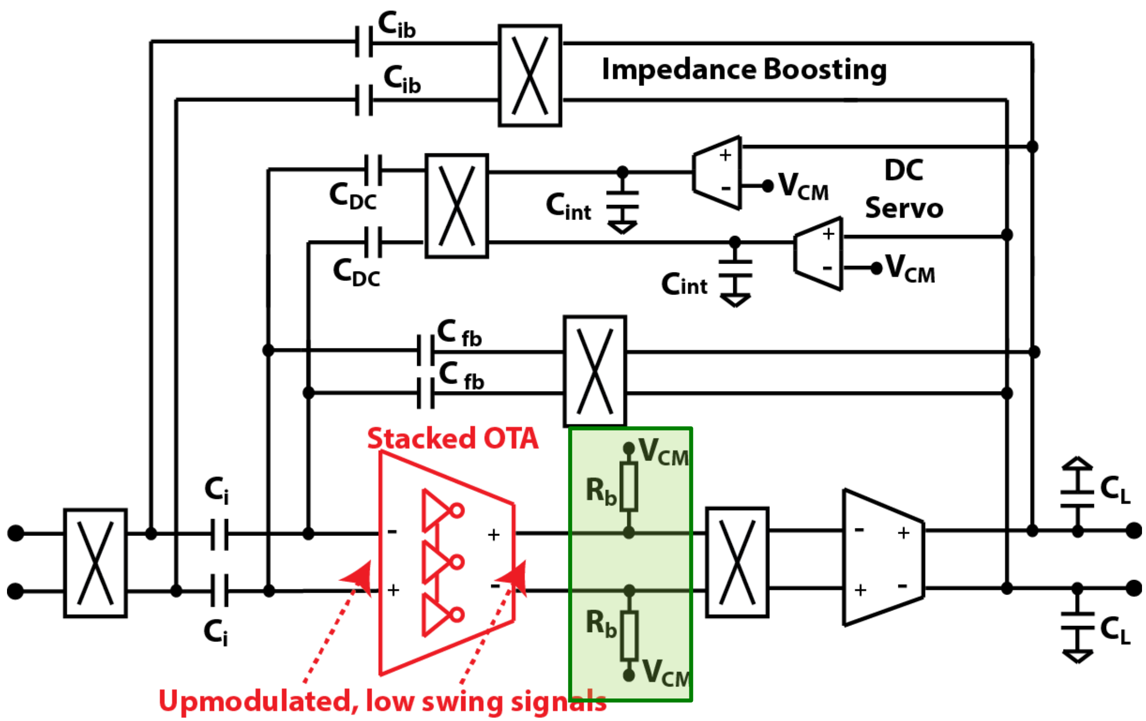

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- High input impedance
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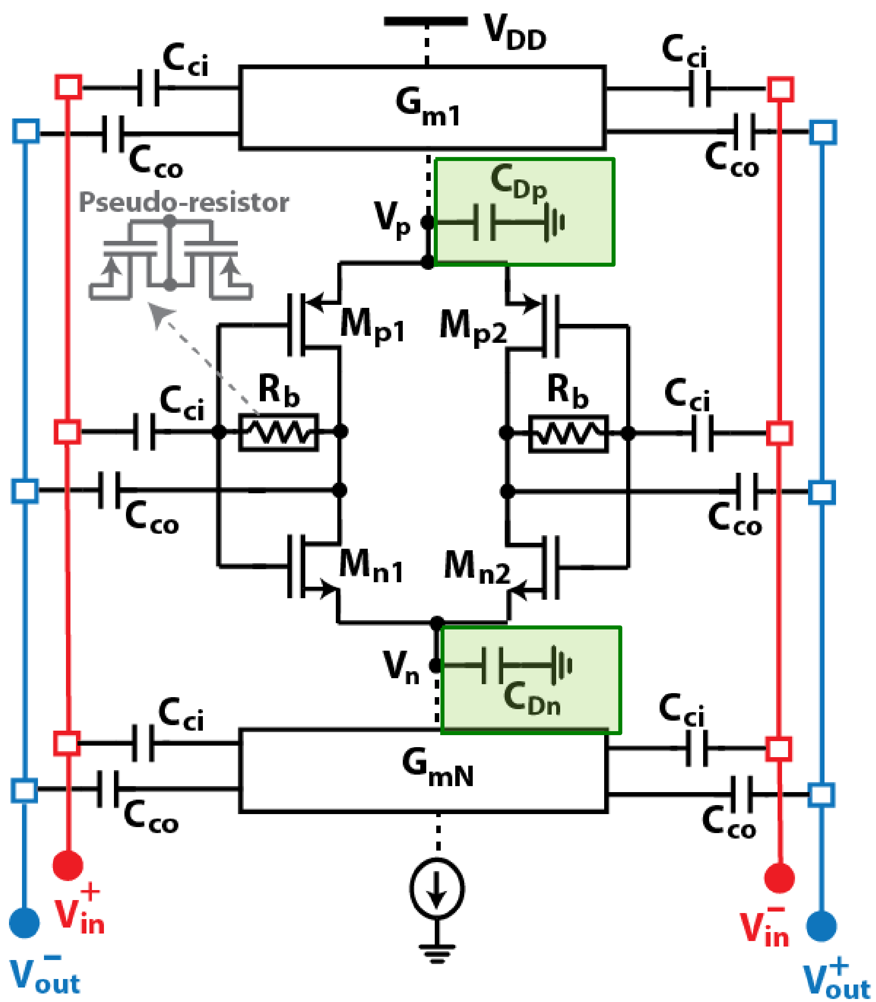
Circuit Implementation

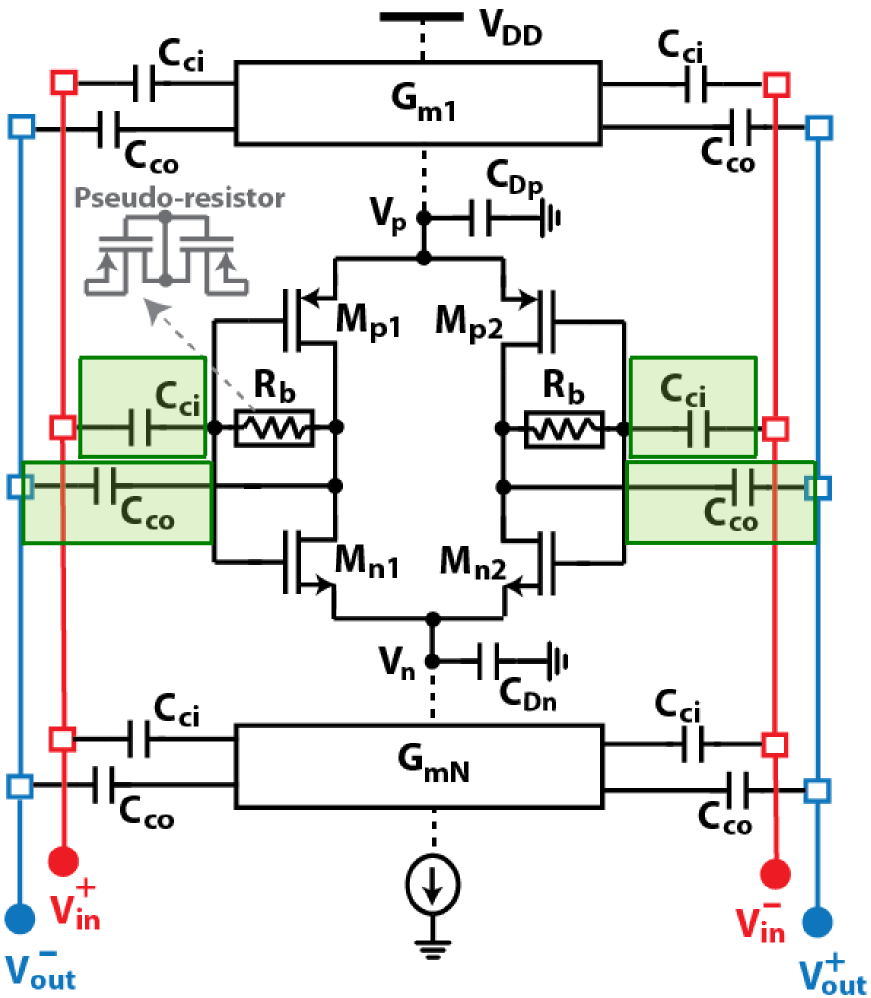
Fully Differential Stacked OTA:



- C_{ci}, C_{co}, $C_{\mathrm{Dn,p}}$ → low impedance (ac-shorts) at the chopping frequency (5 kHz)
- $C_{\mathrm{Dn,p}}$ are 25 pF MOS capacitors to account for $1/g_m$ source impedance ~ 6MΩ. (40×40 $\mu\mathrm{m}^2$)
- Differential operation aids the decoupling with source nodes acting as virtual shorts.

Circuit Implementation

Fully Differential Stacked OTA:

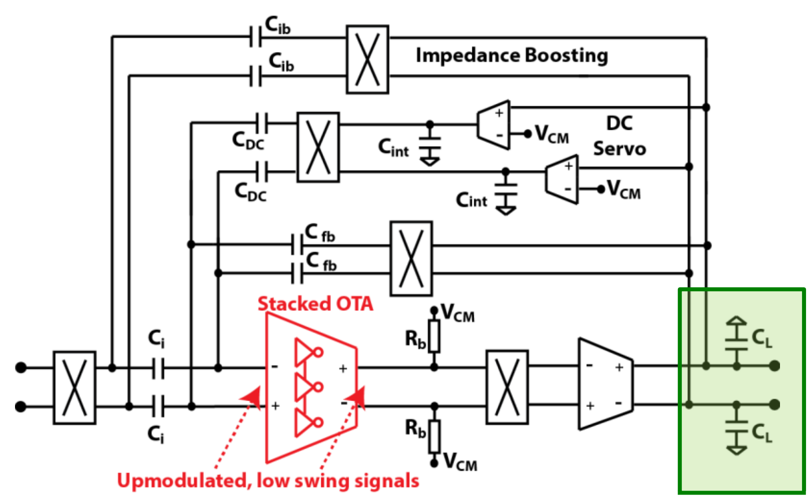


Mid-band gain:

$$A_{\mathrm{M1}} = -\left(\frac{C_{\mathrm{Ci}}}{C_{\mathrm{ci}} + C_{\mathrm{in,tot}}}\right) G_{\mathrm{mo}} R_{\mathrm{o}} \left(\frac{N C_{\mathrm{co}}}{N C_{\mathrm{co}} + C_{\mathrm{L1}}}\right)$$

Large C_{L1} required for Miller compensation

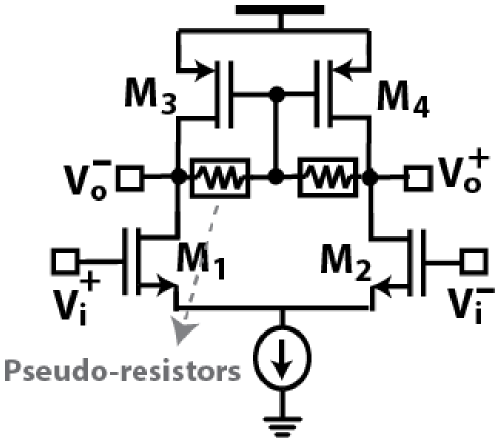
→ Use load compensation used instead



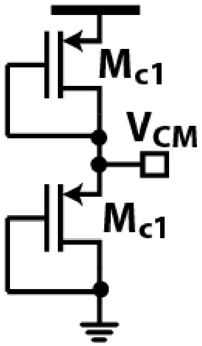
$C_{\mathrm{Ci,o}}$ are 4 pF MOM capacitors

Circuit Implementation

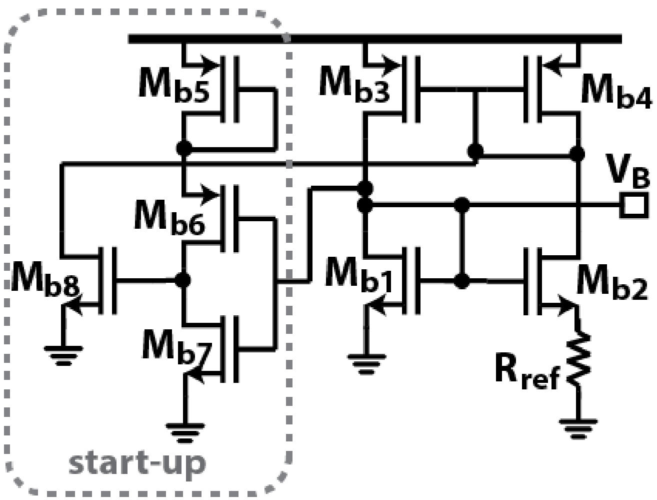
2^{nd} stage OTA:



V_{CM} generation:

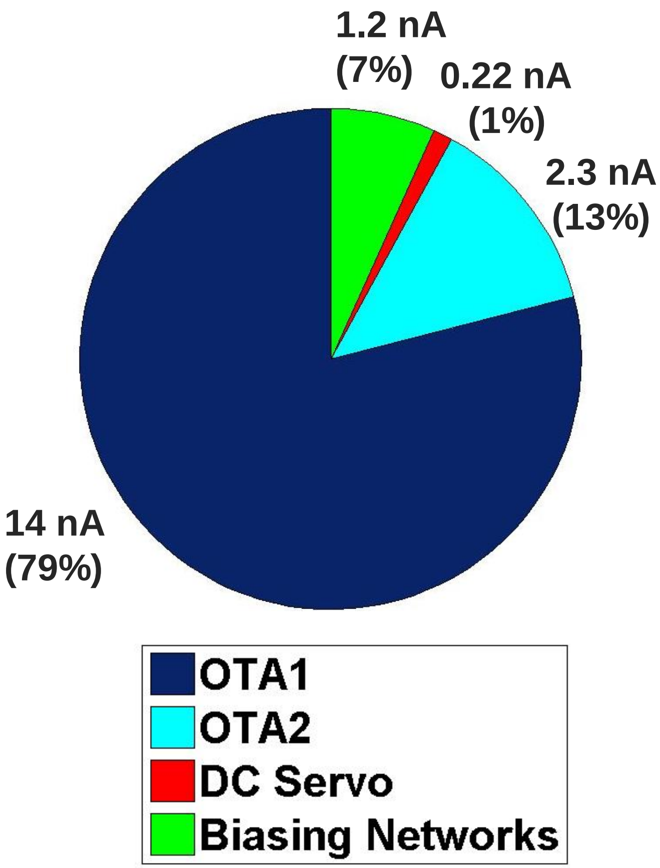


Constant-G_m bias:



Design Summary:

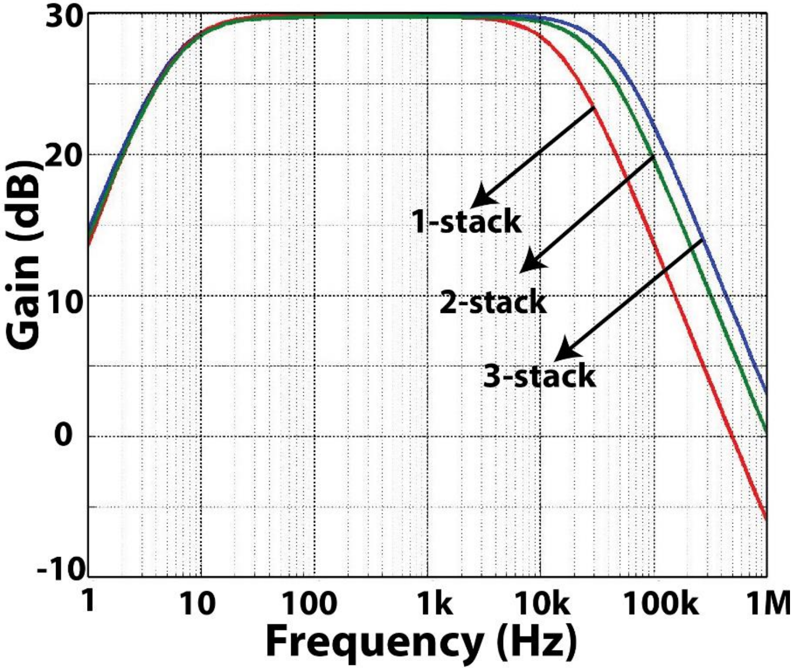
- 1 V Supply



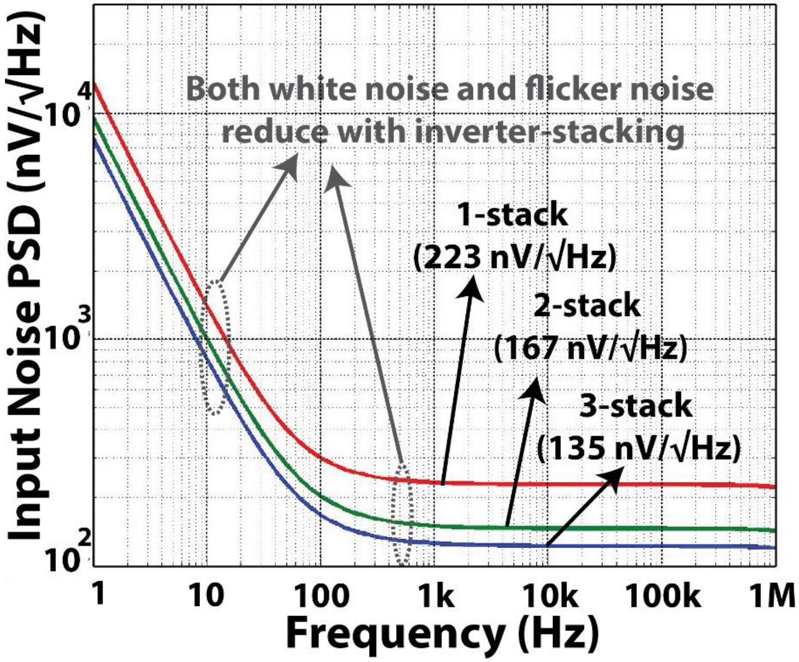
Simulation Results

Stacked OTA simulations

Open-loop gain

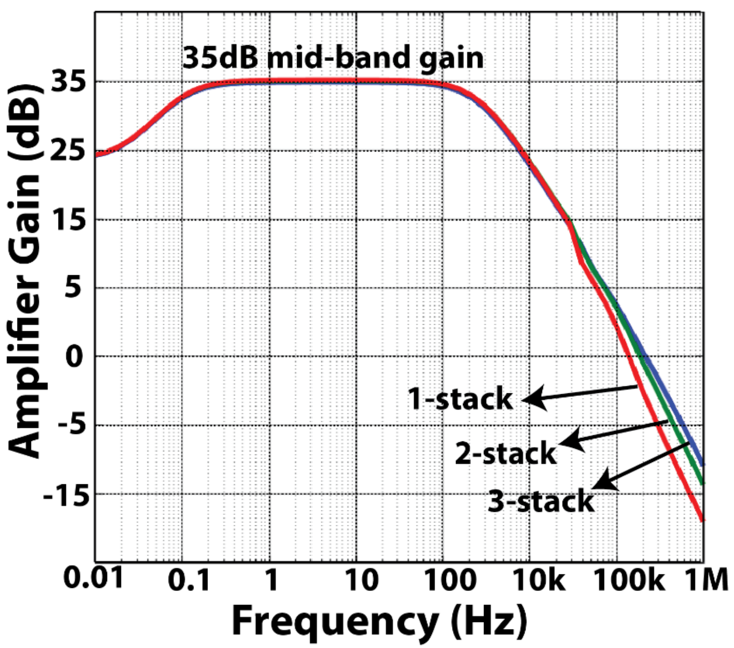


Input-referred noise

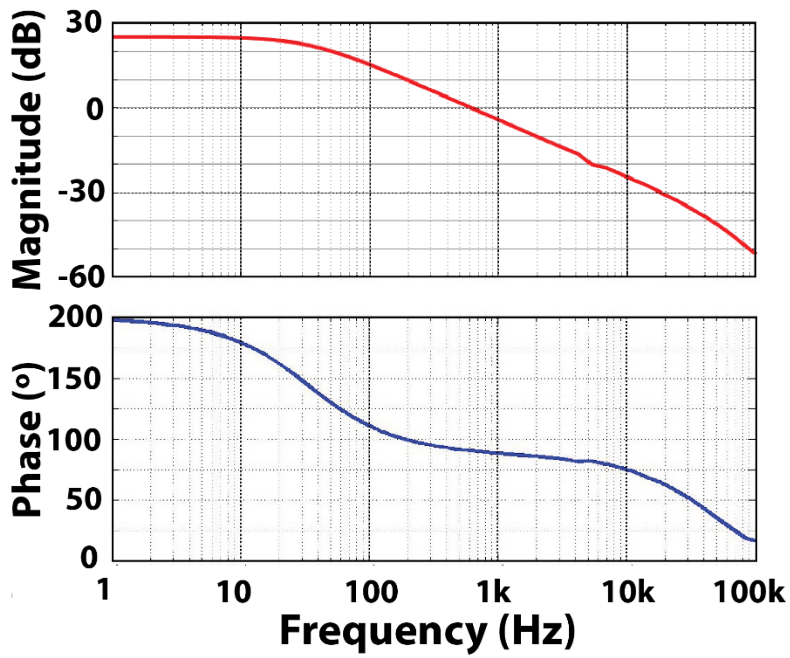


Closed-loop amplifier simulations

Amplifier differential-mode gain (using PAC analysis)



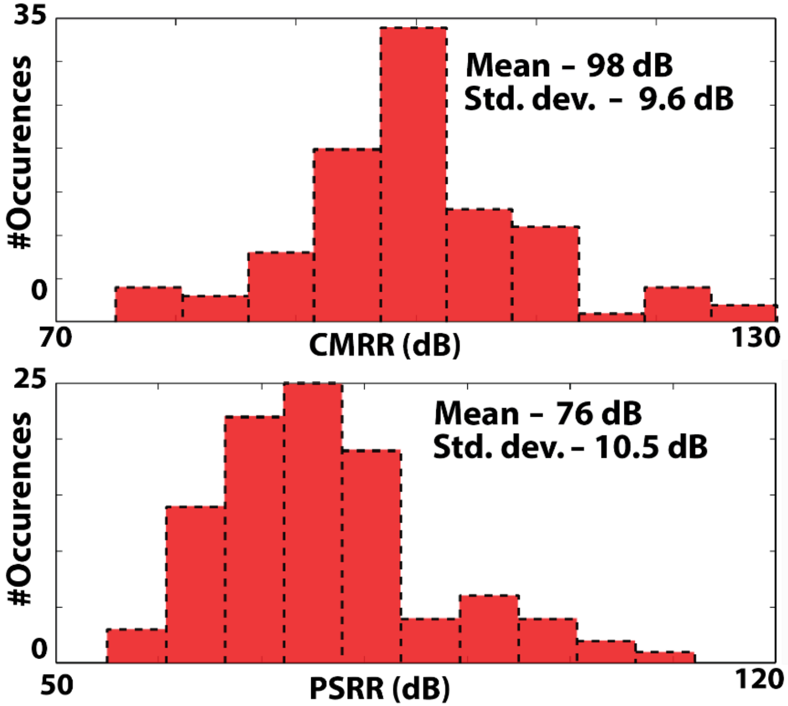
Amplifier loop-gain (using PSTB analysis)



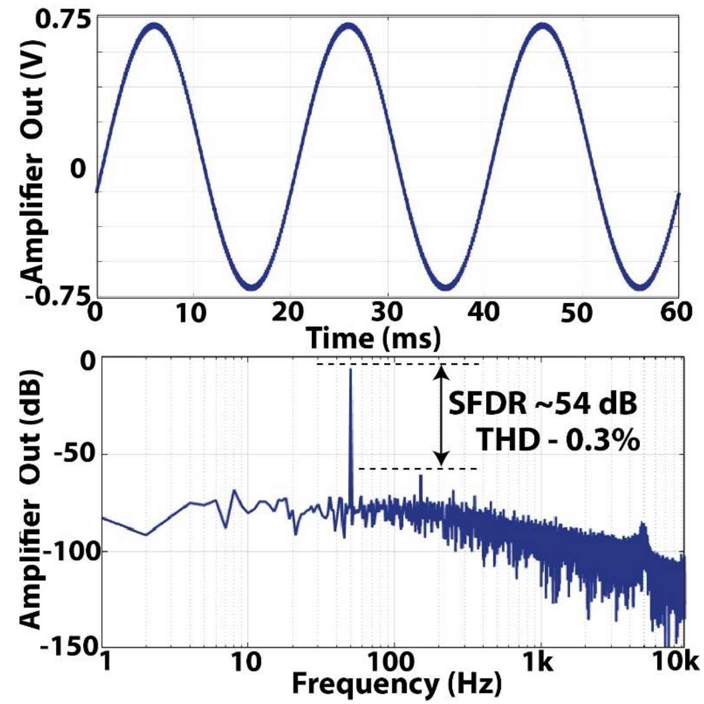
Phase Margin ~ 90°

Simulation Results

100 monte-carlo runs (over process and mismatch variations)



Amplifier transient response and spectra

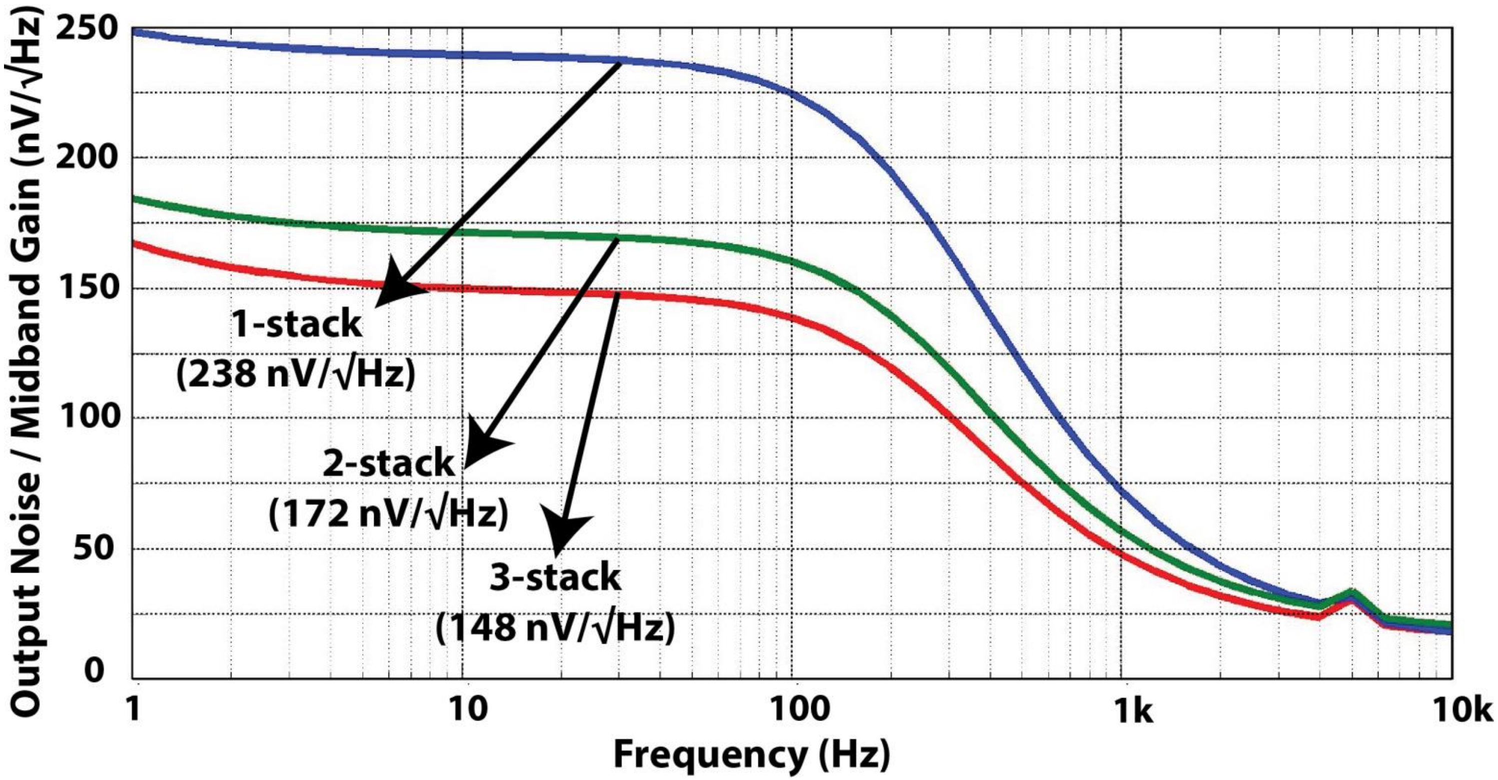


CMRR > 75 dB
PSRR > 60 dB

SFDR = 54 dB
THD = 0.3%

Simulation Results

Amplifier noise performance with inverter-stacking



148 nV/√Hz with only 14 nA!

Summary and Comparison

	This work #			Harpe ISSCC'15	Jeon ISSCC'14	# Song ISCAS'14	Yaul ISSCC'16	Han ISSCC'13	Chen VLSI'14
Application	ECG			ECG	ECG	Fetal ECG	EEG	EEG	-
Technology Node	65 nm			65 nm	65 nm	180 nm	180 nm	180 nm	180 nm
Supply (V)	1			0.6	0.6	1	0.2 and 0.8	0.45	1
Power (nW)	17.7			1	16.8	2,500	790	730	266
Current (nA)	17.7			1.67	28	2,500	987	1622	266
Gain (dB)	35			32	51 – 96	50	58	52	60
BW (Hz)	250			370	250	120	670	10,000	500
Input-referred Noise (nV/√Hz)	148[3]	172[2]	238[1]	1,400	253	21.8	36	29	54.9
CMRR / PSRR (dB)	>75 / >60			60 / 63	80 / 67	>60 / >80	85 / 74	73 / 80	89 / 92
NEF	0.92[3]	1.08[2]	1.51[1]	2.1	2.64	1.17	2.1	1.57	1.38
PEF	0.85[3]	1.17[2]	2.28[1]	2.64	4.1	1.37	1.6	1.12	1.9

Simulated Designs [1]1-stack [2]2-stack [3]3-stack

Best reported NEF of 0.92 and PEF of 0.85!

Conclusion

- AC-coupled Inverter-stacking for G_m-boosting leading to noise efficiency enhancement
- Best-reported NEF/PEF from simulations
- Useful technique particularly for IoT mHealth applications

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