An ECG Chopper Amplifier Achieving 0.92 NEF and 0.85 PEF with AC-coupled Inverter-Stacking for Noise Efficiency Enhancement

Somok Mondal and Drew A. Hall
University of California, San Diego, La Jolla, CA, USA 92093

***Abstract*—This paper presents an ultra-low power chopper-stabilized amplifier intended for portable or implantable ECG applications. A new technique to fundamentally improve the noise efficiency of such amplifiers is introduced that is based on G_m-boosting by AC-coupling up-modulated signals onto stacked inverters. Designed and simulated in a 65 nm CMOS process, the amplifier consumes 17.7 nW from a 1 V supply. An efficient current-reuse and better utilization of the supply voltage using the proposed technique by stacking three inverters leads to a best-reported Noise Efficiency Factor (NEF) of 0.92 and Power Efficiency Factor (PEF) of 0.85.**

I. Introduction

Demand for miniaturized wearable and implantable bio-sensors has increased dramatically over the past several years due to their ability to track and monitor our well-being unobtrusively within our daily routine. However, such sensors with a small form factor and the need for continuous acquisition of bio-signals like the electrocardiogram (ECG) have stringent power budgets, especially the implantable versions. An energy-efficient design is therefore critical for long lasting operation.

ECG sensing is typically performed by precision analog circuitry which amplifies weak, low bandwidth bio-signals while introducing minimal circuit noise. With the power consumption being noise-limited, achieving high noise efficiency has always been an important aspect in the design of such amplifiers for physiological sensing applications. The Noise Efficiency Factor (NEF) and the Power Efficiency Factor (PEF) are well-known metrics to quantify the performance of these amplifiers. The NEF, defined in [1], expresses the noise-current trade-off and is given as

$$NEF = v_{\mathrm{ni,RMS}}\sqrt{\frac{2I_{\mathrm{tot}}}{V_{\mathrm{T}}4k_{\mathrm{B}}T\pi BW}}, \tag{1}$$

where V_{T} is the thermal voltage, k_{B} is Boltzmann's constant, T is the temperature, I_{tot} is the total current drawn by the amplifier, BW is its bandwidth, and $v_{\mathrm{ni,RMS}}$ is its input-referred noise. For a differential amplifier using MOSFETs as the input devices operating in subthreshold and being the sole contributors to the noise, a theoretical limit for the noise efficiency, NEF_o can be found [2] to be

$$NEF_{\mathrm{o}} = \sqrt{\frac{2}{\kappa^2}} \cong 2.02, \tag{2}$$

where κ is the gate coupling coefficient, typically ~0.7.

This implies that with optimal sizing, a designer can, at best, achieve an NEF of 2.02. Overcoming this limit has therefore been the objective of several previous works. Employing inverter-based OTAs introduced in [3] to double the transconductance by reusing the current is a commonly used technique which reduces the NEF limit to 1.43. Further extensions to this current reuse concept are made in [4] with the input chopped at multiple frequencies being applied to stacked transistors and in [5] with the aid of partial OTA-sharing. However, the former technique suffers from the need for complicated demodulation requiring 4th order filters and a limited swing due to the open-loop operation whereas the latter can be adopted only for applications involving sensor arrays like neural recording. Since a lower NEF doesn't necessarily imply a lower power design, some have focused on reducing the PEF (defined as NEF^2V_{DD}, where V_{DD} is the supply voltage) by operating the first stage of a two-stage op-amp with a lower supply voltage (0.2 V) [6]. However, this technique has a design overhead requiring a low power DC-DC converter.

Towards this end, a new technique based on AC-coupled stacked inverters for chopper amplifiers is proposed where both the NEF and the PEF are fundamentally improved without introducing any overhead as in prior works. The NEF limit with the stacking of three inverters is reduced to 0.82. To demonstrate and compare the benefits, the technique has been employed in an amplifier designed for ECG acquisition. A best-reported NEF and PEF, to the best of the author's knowledge, is achieved from simulations of the circuit in a 65 nm CMOS technology.

II. Noise Efficiency Enhancement by OTA Stacking

The proposed concept of noise efficiency enhancement is presented in this section. Inverter-based stages that traditionally

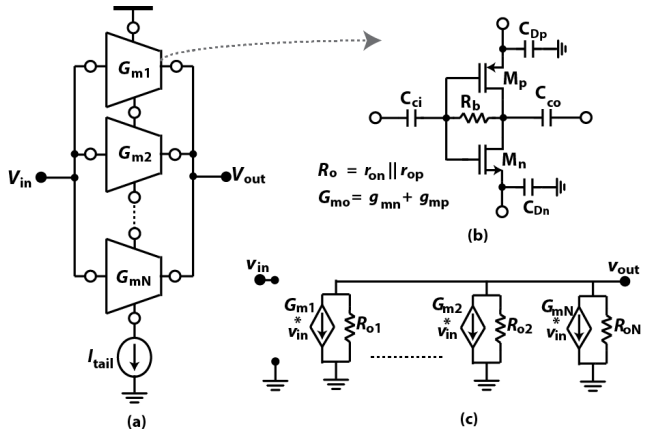

Fig. 1. Proposed (a) stacked OTA, (b) AC-coupled inverter-based transconductor, and (c) equivalent small-signal model.

offer a transconductance improvement of 2× are stacked on top of each other, as shown in Fig. 1(a). The inputs and outputs of each inverter stage are AC-coupled using capacitors C_{ci} and C_{co}, respectively. Capacitors C_{Dp} and C_{Dn} are used to decouple each stage from its stacked neighbor (Fig. 1b). With all the transistors biased to operate in subthreshold with the same drain current, each inverter stage has the same transconductance G_{mo} and output impedance R_o (Fig. 1c). The compound transconductance, G_m, from stacking N stages is NG_{mo}. While the G_m is increased by N, the compound output impedance, R_{out}, is reduced by $1/N$ meaning that the open-loop gain, A_v, of the of this multi-stacked OTA remains the same as that of a single stack, $A_v = G_m R_{out} = G_{mo} R_o$. A similar technique was used recently in a crystal oscillator to boost the G_m and improve the start-up requirement [7].

A. Input-Referred Noise

While this G_m boosting from amplifier stacking does not improve the gain, it results in lower noise. The thermal noise output current from each stacked inverter is uncorrelated corresponding to a total input-referred thermal noise PSD of

$$\overline{v_{ni,thermal}^2} = \frac{4k_B T\gamma}{NG_{mo}}, \quad (3)$$

where γ is a technology dependent noise coefficient. This shows that for the same current, there is an improvement in the thermal noise power by a factor of $1/N$ using the proposed technique. The flicker noise contribution of this stacked OTA can similarly be found by modelling each transistor's noise contribution as a voltage source in series with the gate. It can be shown that the total input-referred flicker noise PSD is

$$\overline{v_{ni,flicker}^2} = \frac{1}{4Nf}\left[\frac{K_n}{C_{ox}(WL)_n} + \frac{K_p}{C_{ox}(WL)_p}\right], \quad (4)$$

where $K_{n,p}$ are technology dependent constants for NMOS and PMOS devices, respectively, C_{ox} is the oxide capacitance per unit area, W and L are the transistor sizes, and f is the frequency. This noise source is also reduced by a factor of $1/N$.

B. Benefits of Enhanced Noise Efficiency

For a chopper amplifier where the flicker noise is removed, the improvement in the thermal noise translates to a $\sqrt{2N}$ improvement over the NEF_o in (2). Thus, the theoretical NEF limit using a 2-stack of inverters is improved by $\sqrt{4}$ to 1.01 and 3-stack of inverters is improved by $\sqrt{6}$ to 0.82. Better utilization of the available supply voltage also results in improvements in the PEF by $2N$ (assuming the same supply was used). Finally, the suppression of flicker noise results in another benefit with the filtering requirements for the up-modulated flicker noise in a chopper amplifier being relaxed. It should be noted that in this work, a differential circuit is considered since ECG requires rejection of common-mode artifacts. The single-ended counter-part exhibits a further lower NEF limit of 0.7 [8] which can also be enhanced by the same factor using this technique.

III. ECG Amplifier Architecture

Employing the proposed inverter stacking technique for an ECG application has a few key challenges that need to be addressed in addition to the typical application specific considerations. First, since the ECG is a slow varying signal with the useful signal content lying at frequencies less than 250 Hz, AC-coupling at baseband would require large capacitors. Second, with inverter stacking, the achievable output swing of the OTA is reduced. The amplifier architecture implemented for this work is shown in Fig. 2 and is similar to the ones presented in [9-10]. In the capacitive-feedback chopper amplifier, the first stage is implemented with the stacked OTA topology. The signals processed by this first stage are up-modulated by the chopper switches. The chopping action naturally lends itself to simple AC-coupling (as the signal of interest lies at the higher chopping frequency) and is possible with the use of smaller on-chip capacitors. Also, the output swing from this first stage is generally small, making the use of stacked inverters with reduced swing feasible.

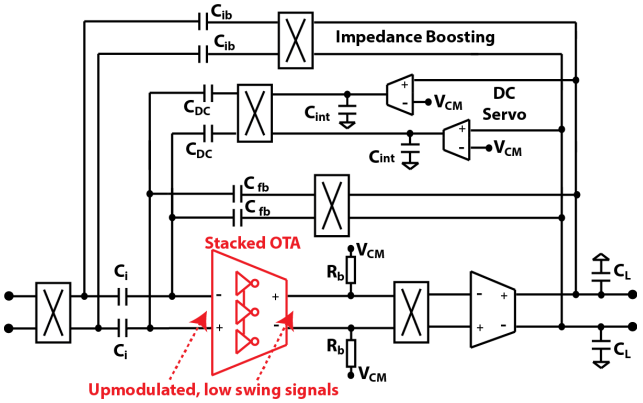

Fig. 2. Chopper stabilized amplifier architecture.

Down-chopping is performed at an intermediate node to suppress distortion due to chopper settling errors using the inherent feedback of the amplifier [9]. The DC bias for the transistors of the AC-coupled first stage are self-generated as discussed later, whereas biasing resistors are used for the second-stage to set an appropriate DC common-mode input voltage. This biasing resistor along with the coupling capacitors of the stacked OTA block DC/low frequencies, but since it is placed before the down-chopper, the associated up-modulated signal remains unaffected. A servo-loop is implemented to suppress the otherwise amplified DC electrode offsets appearing at the amplifier output by integrating it and cancelling the DC component at the input. Finally, a positive feedback-loop addresses the degraded input impedance by compensating the charge lost in the switched capacitor action of the input chopper modulator.

IV. Circuit Implementation

A fully-differential implementation of the inverter-stacked OTA is shown in Fig. 3(a). Each stage of the stacked OTA is self-biased using resistive feedback. All transistors are low-V_t devices and sized such that each inverter requires 280 mV headroom leaving 160 mV for the tail current source with a 1 V supply. All biasing resistors, including the ones used for biasing the second stage OTA input, are implemented with MOS pseudo-resistors.

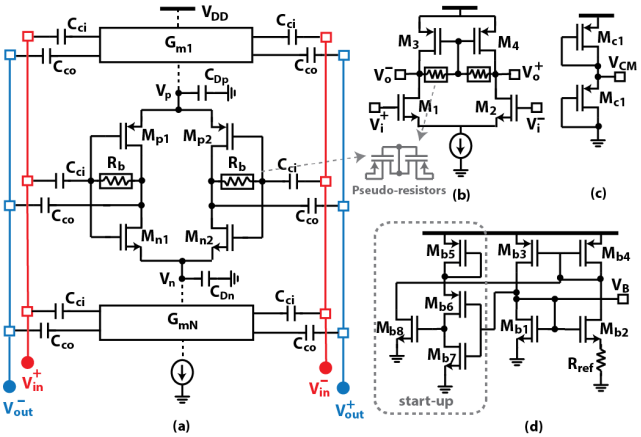

Fig. 3. Schematic of (a) fully differential stacked OTA and pseudo-resistors, (b) 2nd stage OTA, (c) V_{CM} generator, and (d) constant G_m bias.

For proper AC-coupling, the capacitors need to be sized such that their impedance at the chopping frequency (5 kHz) is smaller than the remaining circuit impedance seen at the associated nodes. In this work, thin-oxide MOS-capacitors offering high capacitance density (10× that of MOM-capacitors in this technology) have been used for all the coupling capacitors (C_{Ci}, C_{Co}, C_{Dn}, and C_{Dp}) whereas more precise MOM capacitors were used to realize the amplifier's feedback and input capacitors (C_i, C_{fb}, C_{int}, and C_{DC}). The voltage dependence of the MOS capacitance is not an issue since the first stage deals with low-swing signals and, as discussed later, the open-loop gain changes are negligible if appropriate large coupling capacitors are selected. The effect of any changes in the open-loop response are further suppressed by the feedback, provided the open-loop gain is sufficiently large. $C_{Dn,p}$ are 25 pF to account for ~ 6 MΩ impedance seen looking into the source nodes. A 40×40 μm^2 area suffices to realize these MOS-capacitors. It should be noted that due to the ultra-low device currents and g_m from the noise requirements for ECG applications, the $1/g_m$ impedance is sufficiently high and allows a practical capacitor value for on-chip implementation of C_D. Furthermore, nodes $V_{p,n}$ which are the source nodes of the differential pairs driven by a constant tail current act as virtual shorts for a differential-mode input hence inherently aiding the decoupling. The other input and output coupling capacitors (C_{ci} and C_{co}) appear between higher impedance nodes and exhibit easier AC-coupling. Additional considerations from the open-loop gain perspective are however needed for the selection of C_{ci} and C_{co}. The mid-band gain A_{M1} is attenuated by a capacitive divider as

$$A_{M1} = -\left(\frac{C_{ci}}{C_{ci}+C_{in,tot}}\right) G_{mo}R_o \left(\frac{NC_{co}}{NC_{co}+C_L}\right), \quad (5)$$

where $C_{in,tot}$ is the total input gate capacitance of the stacked OTA and C_L is the load seen by the OTA. A 4 pF value was chosen for C_{ci} and is sufficiently larger than the $C_{in,tot}$ of 165 fF in this design. If the two-stage op-amp was Miller compensated, C_{co} would need to be very large to not attenuate the signal given the effective load capacitance of $C_c(1-A_{v2})$ where A_{v2} is the second stage gain and C_C is the Miller compensation capacitor. Instead, we use load compensation by placing the dominant pole at the output node. For ECG applications with very low bandwidth, such load compensation

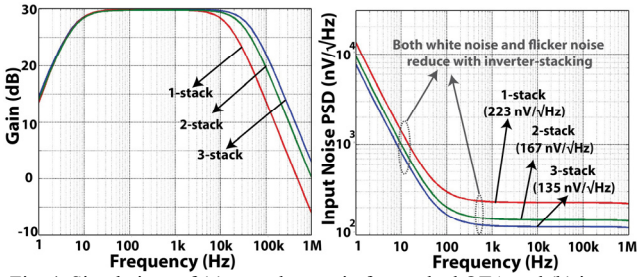

Fig. 4. Simulations of (a) open-loop gain for stacked OTA and (b) input-referred noise for different stacking configurations.

can be easily achieved and has been used in state-of-the-art designs [11]. With a C_L of 110 fF, the gate capacitance of the second stage, 4 pF, suffices for C_{co}. It should also be noted that C_{co} in series with the load doesn't degrade the bandwidth nor does C_{ci} in series with the parasitic gate capacitance degrade the OTA input capacitance while AC-coupling for noise efficiency enhancement.

The implementation of other auxiliary circuits is shown in Fig. 3. A conventional fully-differential amplifier (Fig. 3b) and single-ended differential amplifier are used for the second stage OTA and the servo-loop OTAs, respectively. Cascoded diode connected devices in subthreshold shown in Fig. 3(c) are used for generating a mid-supply common-mode voltage with low power consumption [11]. A constant-G_m circuit (Fig. 3d) is used for bias current generation. The amplifier is designed such that the first stage OTA consumes 14 nA, the second stage OTA 2.3 nA, the DC servo-loop OTAs 0.22 nA and the remaining biasing networks consume 1.2 nA from a 1 V supply.

V. Simulation Results

SPECTRE simulation results are presented in this section. Fig 4(a) shows the open-loop gain of the stacked OTA with appropriate loading. A HPF corner results from the coupling / DC-blocking capacitors. However this is not an issue since the signal of interest is up-modulated to 5 kHz and the OTA has sufficient bandwidth. This also indicates that a proper AC-coupling is realized for the up-modulated signal of interest. Furthermore, Fig. 4(a) highlights an additional benefit of the inverter-stacking – due to the G_m boosting, the bandwidth for processing up-modulated chopped signals is also increased which implies better settling behavior for the same low current. The input-referred noise for this stacked OTA is shown in Fig. 4(b). As discussed earlier, both the flicker and white noise are reduced with each additional stacking of an inverter-stage.

The closed-loop response of the chopper-stabilized ECG amplifier obtained using PAC-analysis is shown in Fig. 5(a). A

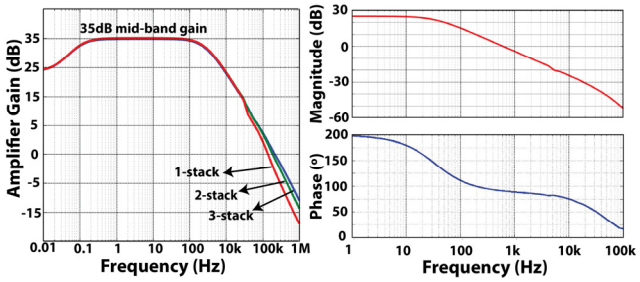

Fig. 5. Closed-loop amplifier simulations (a) differential-mode frequency response (using PAC analysis) and (b) loop-gain (using PSTB analysis).

TABLE I
PERFORMANCE SUMMARY AND COMPARISON TO STATE-OF-THE-ART BIO-AFES

	This work[#]			[11]	[12]	[13][#]	[6]	[14]	[4]
Application	ECG			ECG	ECG	Fetal ECG	EEG	EEG	-
Technology Node	65 nm			65 nm	65 nm	180 nm	180 nm	180 nm	180 nm
Supply (V)	1			0.6	0.6	1	0.2 and 0.8	0.45	1
Power (nW)	17.7			1	16.8	2,500	790	730	266
Current (nA)	17.7			1.67	28	2,500	987	1622	266
Gain (dB)	35			32	51 – 96	50	58	52	60
BW (Hz)	250			370	250	120	670	10,000	500
Input-referred Noise (nV/√Hz)	148[3]	172[2]	238[1]	1,400	253	21.8	36	29	54.9
CMRR / PSRR (dB)	>75 / >60			60 / 63	80 / 67	>60 / >80	85 / 74	73 / 80	89 / 92
NEF	0.92[3]	1.08[2]	1.51[1]	2.1	2.64	1.17	2.1	1.57	1.38
PEF	0.85[3]	1.17[2]	2.28[1]	2.64	4.1	1.37	1.6	1.12	1.9

[#] Simulated Designs [1]1-stack [2]2-stack [3]3-stack

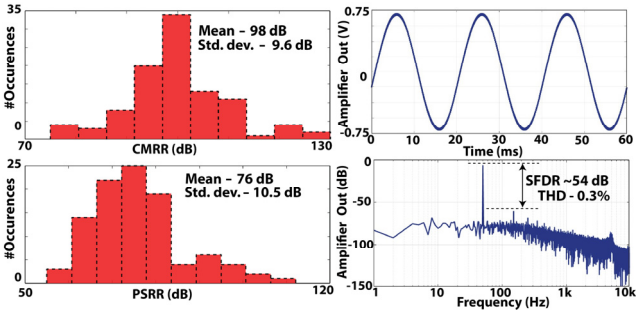

Fig. 6. Simulated amplifier (a) CMRR and PSRR for 100 Monte-Carlo runs (over process and mismatch variations) and (b) transient waveform and spectra for a full-scale sinusoid.

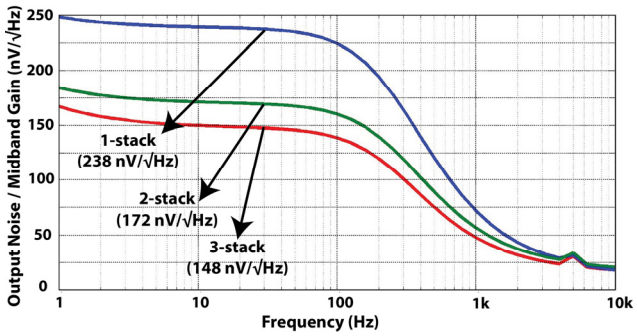

Fig. 7. Simulated amplifier output noise power spectral density divided by the mid-band gain.

gain of 35 dB is achieved, as set by the ratio of the input and the feedback capacitor. The servo-loop blocks DC signals creating a high-pass corner at 0.1 Hz while the amplifier bandwidth extends to 250 Hz. The magnitude and phase of the loop-gain simulated using PSTB analysis are shown in Fig. 5(b). The phase margin is close to 90º, which is typical in bio-signal applications that end up being overcompensated by using large capacitors to get a low bandwidth. The CMRR and PSRR are greater than 75 dB and 60 dB, respectively as obtained from 100 Monte-Carlo runs (Fig. 6a). A transient sinusoid with 1.5 V_{pp} differential swing and its spectra is shown in Fig. 6(b). The main benefit of the proposed work is shown in Fig. 7. The resulting input-referred white noise floor of the chopper amplifier for a single inverter OTA (N=1) is 238 nV/√Hz, reduces to 172 nV/√Hz for N=2, and further reduces to 148 nV/√Hz for N=3 while consuming the same current and thereby demonstrating the noise efficiency enhancement. The design is summarized in Table I and compared to current state-of-the-art.

VI. CONCLUSION

A technique for improving the noise efficiency in chopper amplifiers is presented. For the same current consumption, a G_m boosting leads to a lower thermal noise while additionally reducing chopper settling ripple due to improved first-stage bandwidth and relaxed filtering of the already lower up-modulated flicker noise. With the stacking of three inverters, the chopper amplifier for ECG applications consuming 17.7 nW from a 1 V supply achieves a best-reported NEF of 0.92 and PEF of 0.85.

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