A Sub-pA Current Sensing Front-End for Transient Induced Molecular Spectroscopy

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Abstract

We report an 8-channel array of low-noise (30.3fA/√Hz) current sensing front-ends with on-chip sensors for label-free, restriction-free biosensing. The analog front-end (AFE) consists of a 1st-order continuous-time delta-sigma (CT-ΔΣ) modulator that achieves 123fA sensitivity and 139dB cross-scale dynamic range over a 10Hz bandwidth while consuming 50μW and occupying 0.11mm^2 per channel. A digital IIR filter and a tri-level pulse width modulated (PWM) current-steering DAC are used to realize the equivalent performance of a multi-bit ΔΣ in an area/power efficient manner. This platform was used to observe protein-ligand interactions in real-time.

Introduction

Monitoring protein-ligand interactions is a crucial process in the drug discovery pipeline as most diseases (e.g., cancer and immune diseases) can be traced back to an abnormality in protein-protein/ligand interactions in the host. Conventional biosensing methods require ligand immobilization and/or protein labeling that can cause steric hinderance and produce substantial distortions in the binding kinetics. Transient induced molecular electronic spectroscopy (TIMES) is a recently reported immobilization-free, label-free biosensing technique [1] to monitor such interactions based on the charge redistribution profile as the biocomplex transiently interacts with an electrode, as shown in Fig. 1(a). Due to the lack of a label, the signal is small (~pA) requiring an ultra-sensitive AFE for detection.

To achieve sub-pA sensitivity, most AFEs use a ΔΣ modulator that oversamples the slowly-varying biosignal by a large oversampling ratio (e.g., OSR > 2^{10}) with 1b quantization, as in [2]. Multi-channel systems often forego multi-bit quantizers due to the area impact and instead opt for higher sampling rates and thus consume higher power in the loop filter. We instead propose an area efficient architecture using a digital IIR filter (essentially a 1st-order predictor) and a tri-level PWM DAC to achieve the performance of a ΔΣ with a 4b quantizer [Fig. 1(b)].

Architecture

The key idea here is to leverage the high OSR in ΔΣ modulators where a linear predictor can be used to estimate the value of the next sample given the previous N samples. The IIR filter is derived from the Taylor expansion of a linearly-varying input where the next state can be computed by the current state and its first derivative, i.e. the difference between two samples in a linear discrete-time system. The signal and noise transfer functions (STF and NTF) of the modified ΔΣ modulator are shown in Fig. 2(a). As expected, the NTF exhibits first-order noise shaping and the STF is unity in signal band thus obviating the need for a reconstruction filter at the output. With a 1b quantizer, the output of the IIR filter is a multi-bit signal that better approximates the input signal thus improving the SQNR. The filter coefficients were chosen such that the peak SNDR was >75dB. It is worth noting that there is a deterministic SQNR nonlinearity in Fig. 2(b) when the input becomes strictly less than one LSB of the IIR predictor. In this case, the quantization error can be modeled same way as in a multi-bit quantizer and thus the IIR-ΔΣ has the same SQNR performance as a 4b ΔΣ at small inputs where the sensitivity is needed.

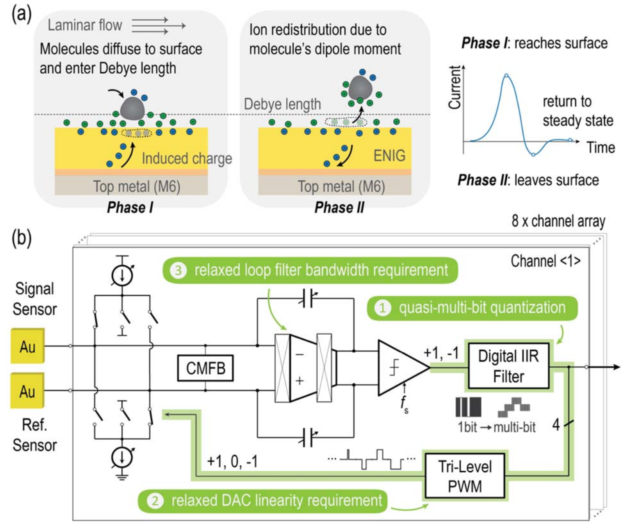

Fig. 1 – (a) TIMES signal model; (b) system architecture of IIR-ΔΣ.

A tri-level PWM DAC feeds a pulse-modulated current signal back to input to close the loop. The tri-level PWM is generated by digitally averaging two opposite two-level PWM ramps and thus the result is free of even-order harmonics and half of the original pulse amplitude, which leads to a 6dB improvement in jitter sensitivity [Fig. 2(c)]. When the input signal is small, the tri-level PWM DAC is turned off for most of the sampling period therefore shunting any thermal noise to the reference. As a result, the tri-level PWM relaxes the DAC linearity requirement from 4b to 3 levels, making it possible to use a single DAC element to achieve equivalent 4b feedback.

Circuit Implementation

The input current ranges from pA to μA depending on the concentration of the biomolecules. To support this wide range, the feedback current is generated on-chip from a 2b tunable current-splitting DAC that progressively scales the reference current, I_{REF}, from 1μA to 1nA in factors of 10× [Fig. 3(a)].

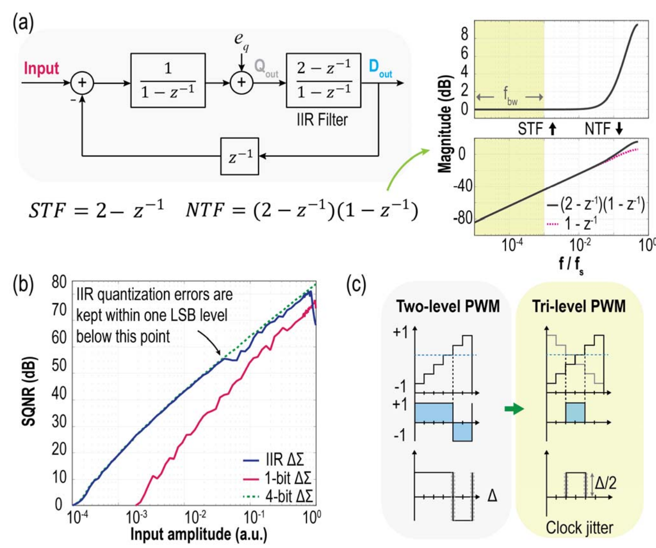

Fig. 2 – (a) Discrete-time model and STF/NTF; (b) simulated SQNR of IIR-ΔΣ; (c) tri-level PWM DAC logic.

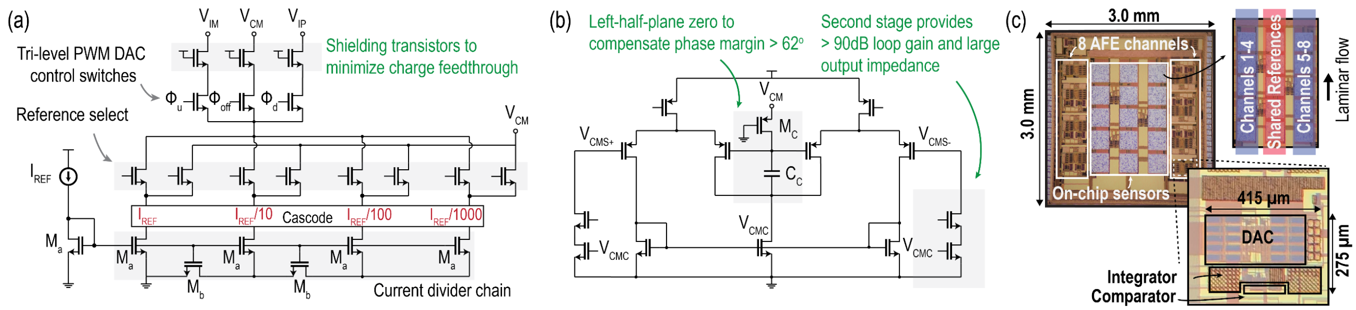

Fig. 3 – Circuit implementation of (a) current-splitting DAC and (b) continuous-time DDA CMFB; (c) annotated die photo.

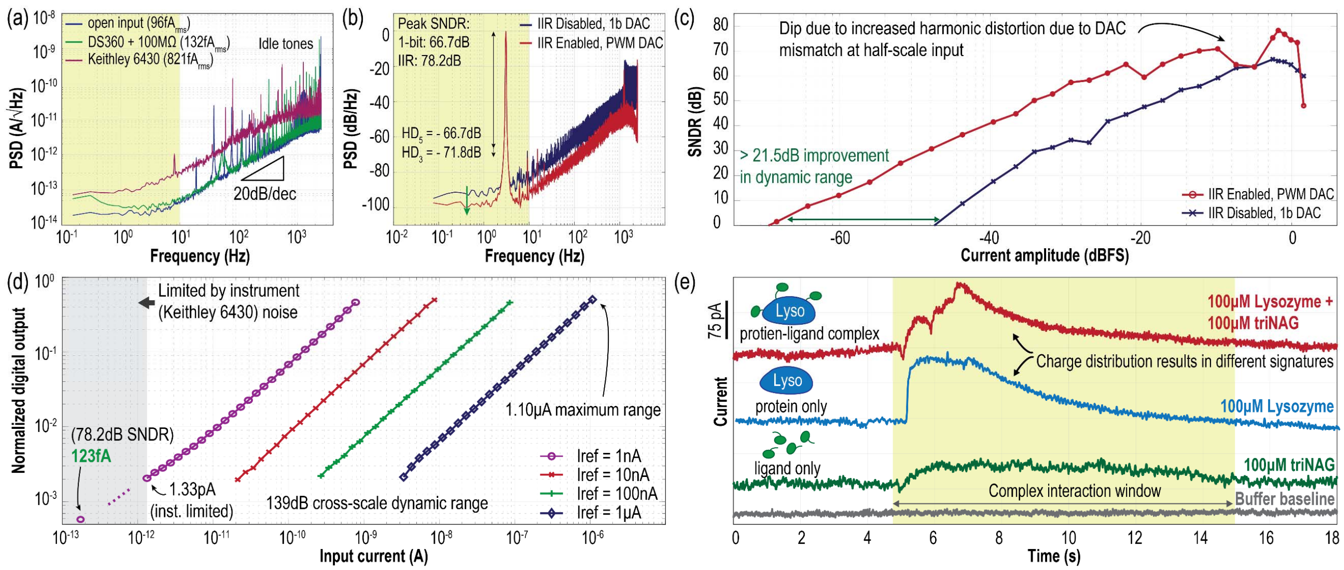

Fig. 4 – Measured (a) input-referred current noise PSD; (b) peak SNDR; (c) SNDR vs. input amplitude; (d) dc response; (e) *in-vitro* assay.

This current splitting technique is inherently linear and does not depend on the operating region of each transistor [3]. In the tri-state DAC, the drain voltage of each switch is always biased at V_{CM} to reduce switching noise.

A continuous-time CMFB circuit sets the dc voltage of the differential inputs [4]. The CMFB consists of a two-stage differential difference amplifier (DDA) to ensure large dc loop gain (>90dB) such that the common-mode offset is minimized [Fig. 3(b)]. In the DDA, a left-half-plane zero was introduced by connecting a 10pF capacitor, C_C, in series with a minimum sized PMOS device such that the phase margin was compensated to 62°. The integrator was implemented with a single-stage folded-cascode OTA (A_{DC}>84dB, UGBW>8MHz) and the comparator with a double tail latch. The IIR filter and PWM logic were implemented off-chip in an FPGA for flexibility.

Measurement Results

This circuit was fabricated in a 180nm CMOS process [Fig. 3(c)]. The measured power consumption was 50.3µW/ch. (integrator 57%, bias 21%, DAC 15%, CMFB 7%, synthesized digital logic <0.1%). For all measurements, the sampling frequency was 5kHz with an OSR of 250. The input-referred current noise PSD shown in Fig. 4(a) was measured with an open input and connected to different instruments achieving a total integrated input-referred current noise of 96.2fA_{rms} in a 100ms conversion time. Fig. 4(b) shows measured spectra with a peak SNDR of 78.2dB for a -2dBFS input – an 11.5dB improvement over a 1b ΔΣ. The dynamic range plot demonstrates that the modulator has performance commiserate with a multibit quantizer exhibiting a 21.5dB improvement in the dynamic range for low input amplitudes [Fig. 4(c)]. The system has a 139dB cross-scale dynamic range, as shown in Fig. 4(d).

Table I – Comparison of state-of-the-art current sensing AFEs.

	Stanaćević TBCAS'07	Li TBCAS'16	Sim TBCAS'17	Hsu ISSCC'18	Nazari TBCAS'13	**This Work**
AFE Architecture	Inc. ΔΣ	Inc. ΔΣ	ΔΣ	Hourglass ΔΣ	CC + SS ADC	IIR-ΔΣ
Process [µm]	0.5	0.5	0.35	0.18	0.35	0.18
Max Input [µA]	1	16	2.8	10	0.35	1.1
Resolution [fA] @ BW [Hz]	100 @ 0.1	100 @ 1	100,000 @ 10	100 @ 1.8	24,000 @ 100	123 @ 10
Conversion Time @ Min. Input [ms]	8,388	1,000	4	400	10	100
Input-referred Noise [fA/ √ Hz]	-	-	6,960	58.9	1,850	30.3
Fixed-/cross-scale DR [dB]	40* / 140	54.0* / 164	77.5	160	60.7 / 95	78.2 / 139
On-chip Sensors?	NO	NO	NO	NO	YES	YES
Num. of Channels	16	50	1	1	192	8
Area/ch. [mm²]	0.25*	0.157	0.5	0.2†	0.04	0.11
Power/ch. [µW]	3.4‡	241	16.8	295	188	50.3

* estimated from figures; † not include synthesized digital area for DEM; ‡ off-chip bias

Each 350×350µm sensor was post-processed by a standard ENIG process. We successfully demonstrated detection of the lysozyme-NAG_3 biocomplex. Each trace has a characteristic shape during the interaction window due to the dipole moment and charge locality [Fig. 4(e)]. Table I compares this work to the state-of-the-art. The proposed IIR/PWM modulation scheme enables a sub-pA multi-channel AFE while introducing virtually no power/area overhead to a conventional 1b ΔΣ.

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