A Pseudo-Virtual Ground Feedforwarding Technique Enabling Linearization and Higher Order Noise Shaping in VCO-Based $\Delta\Sigma$ Modulators

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Abstract—This article presents a third-order voltagecontrolled oscillator (VCO)-based analog-to-digital converter (ADC) that leverages pseudo-virtual ground (PVG) feedforwarding (FF), linearizing the VCOs and enabling higher order noise shaping with a single feedback digital-to-analog converter. This technique leads to a power-efficient ADC implementation with a wide dynamic range. The ADC is fabricated in a 65-nm process and achieves a 92.1-dB SNDR in a 2.5-kHz bandwidth. This results in a state-of-the-art 179.6-dB figure-ofmerit (FoM) among previously published VCO-based ADCs. The PVG FF technique allows the ADC to attain extremely high linearity, 123-dB peak SFDR, with a wide 1.8-V_{pp} differential input range. The ADC maintains performance with up to 200-mV variation on the 0.8-V supply and across temperatures from 0 to 70 °C.

Index Terms—Delta-sigma modulator, feedforward (FF) linearization, time-domain integrator, voltage-controlled oscillator (VCO)-based analog-to-digital converter (ADC).

I. INTRODUCTION

T HE rise of the Internet of Things (IoT) and distributed sensor nodes with machine learning and edge processing is driving the need for low-power, high-precision analogto-digital converters (ADCs). These highly digital systems on chip (SoCs) are best implemented in advanced process nodes that have low intrinsic gain and low supply voltages. These, unfortunately, make designing the high-performance amplifiers required in high-resolution delta–sigma ($\Delta\Sigma$) ADCs challenging [1].

Several techniques have been explored to enable low supply voltage operation, such as bulk input amplifiers, tailless inverters, and bulk biasing [2], [3], [4], [5]. However, these techniques often require removing the amplifier's tail biasing to maintain enough voltage swing at low supply voltages, which involves trading the power supply rejection

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Proposed PVG FF V_{IN} $V_{OD, I}$ VCO $PFD^{\Delta t_{out}}$ L(s) D_{DAC} D_{DAC} D_{DAC} D_{DAC} CCO response $V_{PVG,Gm} = V_{IN} - D_{DAC} \sim 5-10 \text{ mV}$ G_{OUT} V_{IN} $U_{DD, H}$ $V_{DD, L}$ $\Delta t_{out} = \int G_{m} K_{CCO} V_{PVG,Gm}$

Fig. 1. Benefits and challenges of VCO-based ADCs and the proposed PVG FF technique.

ratio (PSRR) and common-mode rejection ratio (CMRR) for swing, ultimately compromising the robustness. Another route is to exploit time-based encoding since it is supply voltage agnostic and benefits from the faster switching times in advanced process nodes. Time-domain architectures are frequently realized using a voltage-controlled oscillator (VCO) where VCOs have been used to implement analog operations such as amplification, filtering, and integration [6], [7], [8], [9], fundamental blocks needed in many mixed-signal systems. The most common use of these time-domain blocks is in $\Delta\Sigma$ ADCs, as shown in Fig. 1, where VCO-based integrators are popular due to their intrinsic phase quantization, openloop noise-shaping [10], and, more importantly, their supply agnostic operation due to the time encoding of the phase information.

While most early research on VCO-based ADCs focused on high-speed applications with bandwidths (BWs) above 10 MHz [11], [12], [13], [14], [15], the past decade has seen a growing interest in leveraging the small area and low supply operation of VCO-based ADCs for distributed sensing applications [16], [17], [18], [19], [20], [21]. These sensor front ends typically require a wide dynamic range (DR) and linearity to capture sensor signals accurately. However, achieving high linearity has been challenging since the voltage-to-frequency gain of VCO-based ADCs is nonlinear, limiting the spurious-free DR (SFDR) to only \sim 50 dB if used in open loop. As such, significant research effort has focused on linearization techniques, such as adding feedback and/or digital calibration [11], [18], [19], [20]. However, as shown in

0018-9200 © 2022 IEEE. Personal use is permitted, but republication/redistribution requires IEEE permission. See https://www.ieee.org/publications/rights/index.html for more information. Fig. 1, even with feedback, the first integrator swing can still be a few tens of millivolts due to the high-impedance node at the input of the integrator. This can limit the linearity and further cause quantization noise folding. Another challenge in time-domain $\Delta\Sigma$ architectures is that they are typically limited to first-order noise shaping. There have been attempts to increase the loop order, thus relaxing the requirement on the quantizer resolution and the oversampling ratio (OSR); however, these relied on hybrid voltage- and time-domain architectures [22], [23], [24], [25], which unfortunately lose the scaling advantages of the time-domain-only architectures.

A few time-domain-only $\Delta\Sigma$ architectures have achieved higher order noise shaping in a single loop. For instance, a second-order VCO-only architecture used a time-encoding integrator first stage, followed by a closed-loop, noise-shaped time-to-digital converter (TDC) [16], but it required adding additional blocks to reduce the quantizer path mismatch and improve the SFDR. In [26], third-order noise shaping is achieved through inner loop feedback. However, the first integrator is open loop, which significantly degrades the linearity. Critically, the performance of these higher order systems is lower than the first-order architecture due to the added complexity and still far from their voltage-domain counterparts.

This work reports an architecture building upon a typical time-domain capacitive digital-to-analog converter (CDAC)based $\Delta\Sigma$ with a VCO-based integrator as the 1st stage, as shown in Fig. 1. A transconductor, G_m, and a currentcontrolled oscillator (CCO) form the VCO core, while a phase detector (PD) extracts the phase difference between the pseudo-differential CCOs. Due to the closed-loop operation, a pseudo-virtual ground (PVG) is created at the ADC input, reducing the swing seen by the VCO and thus linearizing the system. The PD guarantees supply voltage resilience due to the time encoding. The core concept of the technique relies on feeding forward the residue at the PVG to change the loop dynamics and linearize the first integrator by having it only process the quantization noise. This work demonstrates a thirdorder, VCO-only $\Delta\Sigma$ ADC achieving 92.1-dB SNDR over a 2.5-kHz BW using the proposed PVG feedforward (PVG FF) technique. This approach enables a high DR due to the thirdorder noise-shaping and >120-dB SFDR due to linearization. The ADC consumes 4.4 µW from a 0.8-V supply achieving the best-reported Schreier SNDR figure-of-merit (FoM) for VCO-based ADCs at 179.6 dB. This article extends the work presented in [27].

The rest of this article is organized as follows. Section II discusses the loop filter design and architecture. Section III presents the circuit implementation, and Section IV presents the measurement results and a comparison to the state-of-theart. Concluding remarks are made in Section V.

II. LOOP FILTER DESIGN

A. Architecture

The proposed architecture is best explained by starting with the well-known cascade of integrators with feedback (CIFB) architecture shown in Fig. 2(a), where the loop is stabilized through a distributed feedback network. This structure leads



Fig. 2. Comparison of (a) CIFB, (b) CIFB w/ FF, and (c) proposed CIFB w/ PVG FF architectures. (d) Respective output spectra of each architecture.

to a natural implementation of the loop filter coefficients and is well known for its robustness and high anti-aliasing filtering [28]. However, it suffers from a few drawbacks that have pushed researchers to explore alternative architectures. Since the loop dynamics force the first integrator's output to cancel the digital-to-analog converter (DAC) output, the integrator input is very tonal, and the integrator output amplitude scales with the input amplitude. This limits the coefficient scaling, which increases the ADC's area and the noise impact from the subsequent stages, reducing the overall power efficiency. This input-dependent integrator output swing also increases the signal-to-quantization noise ratio (SQNR) degradation for a nonlinear integrator due to quantization noise folding [29].

Adding a feedforward path, as shown in Fig. 2(b), solves some of these issues. Since the DAC at the integrator output contains a scaled copy of the input, feeding forward the ADC input to the integrator's output cancels the signal component from the DAC [30]. The FF path thus reduces the integrator swing at the expense of signal transfer function (STF) peaking and reduced anti-alias filtering since the integrator is bypassed. The lower integrator output swing allows for more aggressive coefficient scaling and linearizes the integrator because it now mainly processes quantization noise. However, the FF path processes the full swing input signal and must be linear, despite the gain attenuation due to the first integrator. To abide by this strict linearity requirement, the FF path is typically implemented by a resistor connected from the input to the virtual ground of a closed-loop RC integrator further down the loop.

Finally, Fig. 2(c) shows the proposed PVG FF architecture block diagram. It builds on the FF architecture by noticing that for ideal signal cancellation, the FF/DAC nodes and the ADC input node perform the same operation, *i.e.*, V_{in} - V_{DAC} . While the path gains are different, the path gain ratios, *i.e.*, $G_2/G_{FF} =$ G_1 , are the same. This allows the signal to be fed forward from the ADC's PVG (the output of the first DAC) instead of the input with appropriate scaling. This enables the loop to operate



Fig. 3. Block diagram of a VCO-based PVG FF architecture.

with the same dynamics as the standard feedforward-based architecture while eliminating the internal feedback DAC(s) and having the FF path process only a small swing, helping with its linearization.

Behavioral simulations of the three architectures show how they perform in the presence of nonlinearities. Based on simulation results, a $G_{\rm m}$ -CCO integrator has ~50-dB SFDR for a 50-mV_{pp} swing, similar to previous work [19]. The spectra with a nonlinear first integrator, K_1 , and FF elements, $G_{\rm FF}$, are compared to the ideal CIFB architecture for a thirdorder loop filter. Fig. 2(d) shows that the CIFB has significant performance degradation when nonlinearities are introduced with noticeable tones and quantization noise folding. There is less quantization noise folding when the input is fed forward, but the FF element's nonlinearities still cause significant distortion. On the other hand, due to the reduced input swing of the FF element, the PVG FF architecture's performance is superior to the CIFB and the input-FF architectures with a similar SQNR as the input-FF but without the tones caused by the FF path nonlinearity. This demonstrates that using the PVG FF architecture, high SNDR can be achieved despite the large PVG swing. This leads to more power-efficient architecture as the linearity of the integrator and FF elements can be relaxed for a target SNR.

This architecture closely resembles the CIFF architecture as it uses FF to remove the need for internal DACs. It, therefore, shares characteristics of the CIFF loop filter family, such as STF peaking and reduced anti-aliasing. It should be noted that the CIFF architecture could not be implemented straightforwardly in a VCO-based ADC as the final integrator and quantizer are merged, and FF directly to the quantizer is not possible. Similarly, the PVG FF technique would not be easy to implement with a closed-loop voltage-domain integrator, as the integrator's gain attenuates the virtual ground node, and loading this node slows down the integrator.

B. Loop Design

A block diagram of a third-order PVG FF architecture implemented using VCO-based integrators is shown in Fig. 3. The feedback DAC generates a voltage that cancels the input voltage, leaving the residue voltage at the ADC's PVG. This voltage is converted to a current through a $G_{\rm m}$ -cell and fed to



Fig. 4. (a) ADC's scaled output for an OBG = 1.25 and OBG = 4.5. (b) PVG swing as a function of the OBG.

a pseudo-differential CCO. The CCO phase difference, $\Delta \varphi$, is extracted using a PD and then converted back into a current where it is combined with the FF path, which is implemented with a transconductor due to the relaxed linearity. The time-domain integration and current-domain summation operations are repeated for the second integrator before the final VCO-based integrator. The last integrator's phase is quantized and fed back to the input.

Designing the loop for a target SQNR depends on selecting key parameters, such as the quantizer resolution, OSR, and out-of-band gain (OBG). The target SNR was 95 dB in a 2.5 kHz BW; thus, the SQNR was designed to be 110 dB in Simulink, 15 dB above the target SNR, to ensure that the system is thermal noise limited and allow for some degradation when other non-idealities, such as chopping artifacts, parasitics, and DAC mismatch, are added later in the design phase. The DAC resolution was selected by trading off two parameters: the PVG node swing and the DAC layout complexity. Adding more bits results in a lower swing at the PVG node, allowing for better $G_{\rm m}$ -cell linearity and power efficiency. A 6-bit quantizer and DAC were selected to limit the maximum PVG swing and achieve the target SONR with a reasonable OSR while maintaining a simple enough DAC layout. An OSR of 80 is then needed to achieve the target SQNR, considering the first integrator's nonlinearity. These parameters are similar to the state-of-the-art voltage-domain ADC reported in [31], which allows one to compare timeand voltage-domain architectures.

The only remaining parameter to be selected is the OBG. Increasing the OBG results in a higher SQNR due to increased quantization noise filtering but affects the stability; thus, the lowest OBG achieving the target SQNR should be selected. Interestingly, the OBG increase also affects the PVG swing. As shown in Fig. 4(a), increasing the high-frequency gain creates "fuzziness" and increases the swing at the PVG. Fig. 4(b) shows a histogram of the integrator input where the swing increases by $\sim 4 \times$ from an OBG of 1.25–4.5. This increased swing causes the achievable SQNR to be limited by the integrator's nonlinearity due to quantization noise folding. This tradeoff is shown in Fig. 5, where the SQNR is calculated for a linear and nonlinear integrator. One can see that the SQNR has a shallow optimum for an OBG between 2 and 2.75, so we chose 2.5 to allow for coefficient variation. It should be



Fig. 5. SQNR versus the OBG for an ideal and nonlinear 1st stage.



Fig. 6. Block diagram of (a) frequency- and (b) phase-domain quantizers.

noted that this optimum point will depend on several factors, such as the OSR, number of bits in the DAC, and $G_{\rm m}$ -CCO linearity. The PVG swing also affects the maximum $g_{\rm m}/I_{\rm D}$ of the $G_{\rm m}$ -cell in the integrators, as a large swing requires a lower $g_{\rm m}/I_{\rm D}$ to avoid full current steering. The ADC's maximum signal amplitude (MSA) depends on the OBG; however, with a 6-bit DAC, the MSA is ~90% with <3% variation between an OBG of 1.25 and 4.5 due to the number of quantizer levels.

Another critical parameter for higher order VCO-based ADCs is the SQNR dependence on the CCO frequency, f_{CCO} , and matching [16], [32]. Two types of VCO-based quantizers have been reported in the literature—frequency- and phasedomain quantizers [14]. While these were used in hybrid voltage-/time-domain ADCs, they can also be used in timedomain-only architectures, as shown in Fig. 6. Frequencybased quantization, where the VCO-based integrator in the quantizer is followed by a differentiator acting as a gain stage [14], [16], is shown in Fig. 6(a). In this architecture, the loop dynamics force the time-domain encoding at the quantizer input to match the ADC input, thus leading to a pulse width modulated (PWM)-based polarity-dependent encoding of the input signal. This makes the quantizer sensitive to path mismatch (between the positive and negative quantization paths) and the preceding CCO's f_{CCO} due to the high-frequency content of the PWM encoding [16].

This is not the case for a phase-domain quantizer, where the quantizer acts as an integrator, and thus, the quantizer input is a representation of the derivative of the ADC input signal [14].



Fig. 7. SQNR versus the CCO frequency normalized to the sampling frequency.

The quantizer is fed the PFD output and the $G_{\rm m}$ -FF signal, thus relaxing the frequency requirement, as only part of the input is PWM encoded and requires that $f_{\rm CCO}$ just should be higher than $2f_{\rm s}$ to update the loop with the phase information at least once per sample. As shown in Fig. 7, this ensures loop stability and SQNR > 108 dB. The derivative encoding in the phasedomain quantizer also benefits from being independent of the input signal polarity, which significantly relaxes the matching between the pseudo-differential VCO-based quantizers and does not require mismatch improvement using a gated-inverted ring oscillator (GIRO), as was done in [16] and [33]. If $f_{\rm CCO}$ cannot be reached with the desired coefficient, it is possible to virtually increase it by tapping multiple phases of the CCO [6], [12].

C. Coefficient Scaling

In voltage-domain architectures, the internal nodes' swing in the loop filter is limited by the supply voltage of the operational amplifiers in the integrators. Therefore, the coefficients must be scaled to avoid saturation, as saturation would cause a large SNDR degradation and can push the loop into an unstable state. In time-based ADCs, this constraint on the voltage swing is transferred to the time domain. Thus, the coefficients must limit the phase difference between the pseudo-differential CCO, $\Delta \varphi$, to avoid phase wrapping in the PD. This highlights the importance of the PD implementation, as its gain directly affects the loop dynamics and the inner loop's DR. The most popular PDs are an XOR gate and a PFD. An XOR PD has a phase range limited to π (*i.e.*, the effective gain is $1/\pi$) and is duty cycle sensitive. On the other hand, a PFD-based PD has a $\pm \pi$ phase range and is edgetriggered. Maximizing the PD DR enables one to maximize the coefficient scaling and thus achieve better power efficiency. Therefore, a PFD-based PD was selected.

Referring to Fig. 3 and using the PFD's gain, the K_1 coefficient can be derived as

$$K_1 = G_{\rm m} K_{\rm CCO} I_{\rm p},\tag{1}$$

where $G_{\rm m}$ is the transconductance, $K_{\rm CCO}$ is the CCO's currentto-frequency gain, and $I_{\rm p}$ is the amplitude of the pulsed current source. The noise requirement sets $G_{\rm m}$, leaving $K_{\rm CCO}$ and $I_{\rm p}$ to achieve the target gain. $K_{\rm CCO}$ should be maximized (up to the limit allowed by the PFD) to allow for higher $f_{\rm CCO}$ and minimize $I_{\rm p}$, thus improving the power efficiency. The



Fig. 8. Block diagram of the proposed architecture and key coefficients.



Fig. 9. Schematic of the input transconductor with dead-band switch.

loop parameters were extracted from behavioral simulations and extensively studied to ensure that the loop remained stable and $\Delta \varphi$ was limited to 2π for all signals in the band of interest.

III. CIRCUIT DESIGN

The reported ADC is shown in Fig. 8 with the relevant coefficients, the sampling frequency f_s , and the chopping frequency f_{ch} . The ADC input is chopped and capacitively coupled through two 252-fF metal-insulator-metal (MIM) capacitors onto the PVG, a high-impedance node. Chopping pushes the flicker noise out of band and improves the ADC's CMRR. f_{ch} is set to $f_s/2$ to avoid quantization noise folding [34]. The output of each $G_{\rm m}$ -cell is chopped to ensure correct polarity in the loop. Due to the preceding gain, $G_{\rm m}$ and power of the second and third VCO-based integrators are scaled by 10×. The final CCO's $\Delta \varphi$ is quantized with a 6-bit gray counter. A segmented dynamic element matching (DEM) algorithm [35] is applied to the output to ensure that the multibit DAC has high linearity. The DEM output is resampled after $0.1/f_s$ (125 ns) to allow time for the logic to settle and synchronize the DAC.

A. G_m-Cells

A schematic of the first G_m is shown in Fig. 9 with the input chopper switches and ac-coupling capacitors. The input and DAC are capacitively coupled, and the input common-mode voltage, V_{cm} , is set through a pseudoresistor. All the G_m -cells share this node. The input chopper switches are clock boosted



Fig. 10. Schematic of the second and third integrator transconductors.

to $2V_{DD}$ to reduce the switches' ON-resistance and allow for inputs above V_{DD} while maintaining high linearity. Chopping the CDAC induces large differential-mode chopping artifacts at the high-impedance PVG node due to the sudden switching and settling of the DAC capacitors upon a polarity swap. These artifacts significantly degrade the ADC performance by pushing the $G_{\rm m}$ -cell out of saturation, causing harmonics and quantization noise folding. It was proposed in [31] to remedy this issue by adding dead-band switches that isolate the $G_{\rm m}$ -cell from the large differential artifact. By opening the dead-band switches for a short time around the chopping instant, these artifacts are converted to common-mode charge injection and attenuated by the $G_{\rm m}$ -cell's CMRR [16], [31]. This allows the ADC's performance to be minimally impacted by the artifacts and maintain a high SQDR. An on-chip pulse generator creates the 30-ns dead-band pulse and boosts the gate to $V_{\rm CM} + V_{\rm DD}$ to guarantee that the PMOS switches remain OFF even with artifacts above V_{DD} .

The first $G_{\rm m}$ -cell is implemented with NMOS thickgate oxide devices to minimize gate leakage and sourcedegenerated by a 3-bit programmable resistor. The $G_{\rm m}$ -cell's current and source degeneration provide coefficient tuning and linearity adjustment post-fabrication to optimize the loop filter coefficients and SNDR. The output current is down-chopped and connected directly to the CCO for maximum current reuse and power efficiency. The second- and third-stage CCO inputs combine the FF path and the PFD-driven integration pulse currents. Due to the architecture's relaxed FF path linearity requirement, the FF $G_{\rm m}$ -cells are implemented with standard differential pairs using thick-gate oxide devices for low gate leakage and biased in weak inversion ($g_{\rm m}/I_{\rm D} > 15$), as shown in Fig. 10.

To ensure a fast and sharp rise time of the PFD-driven pulsed current sources, they are never turned off and instead shunted to a replica CCO in the OFF state, similar to a currentsteering DAC [36], thus maintaining a relatively constant $V_{\rm DS}$ across the current source. The switch does not require any calibration or specialized synchronization as this pulser appears after the integrator; thus, any error is shaped when input-referred. The power cost of this is negligible since $2I_{\rm p1} + 2I_{\rm p2} \approx 150$ nA. This has significant performance benefits, as demonstrated in the simulation results shown in Fig. 11(a), where the circuit is simulated for a 40-ns pulse with and without the replica branch. Without the replica circuit, the



Fig. 11. Simulated (a) voltage and (b) current transient waveforms with and without the replica circuit.

current source's V_{DS} settles slowly to its nominal value and discharges when the switch is OFF. This causes the voltage across the switch at the drain of the current source to increase, leading to significant leakage, as shown in Fig. 11(b). When the replica is added, V_{DS} stays constant at ~540 mV, and the current settles much faster to the desired value while guaranteeing <200 pA of leakage in the OFF state.

Simulations showed that mismatch between the pulsed current sources ($\sigma = 5\%$), easily achieved through layout and sizing, causes an SQNR variance of 0.3 dB, which is negligible because the mismatch appears after the first integrator. The three $G_{\rm m}$ -cells attached to the PVG FF node add 90 fF of parasitic capacitance, which is compensated by tuning the loop filter coefficients. The input transistors were sized to achieve the target $G_{\rm m}$, and the area was selected to ensure that the flicker noise corner was less than 100 kHz ($f_{\rm ch}/2$).

B. CCO and PFD

The ring-oscillator-based CCO implementation is shown in Fig. 12. The ring is current starved by the NMOS-based $G_{\rm m}$ -cells and implemented as pseudo-differential PMOS crosscoupled stages for low phase noise [20]. Low- $V_{\rm T}$ (LVT) devices guarantee a small ring-oscillator swing, 200–300 mV, over the frequency range. The inverter is sized for symmetric transitions to minimize phase noise and the number of stages selected to achieve the target $K_{\rm CCO}$. As illustrated in Fig. 12, the level shifters following the CCO to allow for rail-torail logic are implemented from [20] and consume negligible power. The PFD is built using a standard NOR-based DFF with custom logic gates implemented using high- $V_{\rm T}$ (HVT) devices to decrease the leakage power leading to a 2-ns reset delay. This delay is sufficient to ensure settling time for the current pulser, even for small $\Delta \varphi$.



Fig. 12. Schematic of the CCO and PFD.

C. Quantizer and DAC

The VCO's phase is quantized using a counter-based quantizer [16], [17]. The VCO edges are asynchronous to the sampling instant; as such, the counter topology must be chosen carefully to avoid sampling the counter output during the transition of multiple internal bits [18]. To this end, the counter is implemented using a gray code that allows only one internal transition during counting and therefore guarantees minimal transition errors [18]. The counter accumulates $\Delta \varphi$, adding the difference to the ADC output. This result is then passed through a segmented DEM algorithm [35], which simplifies the DAC implementation by reducing the number of elements compared to data weighted averaging (DWA) and allows for first-order shaping of the DAC mismatch. The DAC unit elements are custom metal-oxide-metal (MOM) capacitors for more flexibility during the layout of the DAC, with a 3.25-fF unit capacitance for a total DAC capacitance of \sim 250 fF. The capacitor variation was expected to be $\sim 0.25\%$ [37], degrading the ADC's performance by less than 1 dB in simulation.

IV. MEASUREMENT RESULTS

The reported ADC was fabricated in a 65-nm LP-CMOS process and occupies 0.1 mm². An annotated chip micrograph is shown in Fig. 13, where the FF transconductors were laid out near the main $G_{\rm m}$ -cell to minimize the parasitic loading at the input node, maximize matching, and avoid resistive loss. The ADC consumes 4.4 µW when operating from a 0.8-V supply, as shown in Fig. 14(a). The CDAC reference voltage is 1.2 V to maximize the ADC input range. The power consumption is dominated by the first integrator, followed by the on-chip digital blocks such as the counter and DEM algorithm, which would benefit from technology scaling. As shown in Fig. 14(b), the shaped CDAC mismatch (from the DEM) dominates the input-referred noise power. This could be remedied by using DWA, which would increase the tonality but decrease the in-band noise generated by the mismatch shaping by 6 dB, or by improving the CDAC layout and increasing the unit capacitors' area for improved matching. It is estimated that this would lead to a \sim 2-dB improvement in the ADC performance. The active area of the ADC is only 0.026 mm², largely due to the first integrator, DAC, and input capacitors, as shown in Fig. 14(c).



Fig. 13. Annotated chip micrograph.



Fig. 14. (a) Power, (b) noise power, and (c) area distributions.

A. Spectral Characterization

The chip was tested using an Audio Precision APx555B ultra-low distortion signal source applying a $1.8-V_{pp}$ full-scale sinusoidal input at 322 Hz. The input common mode was set to 500 mV, so each differential input varies between 50 and 950 mV for a $1.8-V_{pp}$ differential input. Despite the large voltage across the clock-boosted chopping switches, no reliability issues were observed. Fig. 15(a) shows the output spectrum where the ADC achieves a peak SNDR of 92.1 dB in a 2.5-kHz BW and an SFDR of 123 dB. The 60- and 180-Hz tones are caused by power line interference as this was not tested in a Faraday cage. The characteristic 60-dB/decade noise shaping from a third-order modulator is



Fig. 15. Measured ADC (a) spectrum with DEM, (b) spectrum without DEM, and (c) dynamic range.

apparent, confirming the proper operation of the loop. The spectrum when DEM is deactivated is shown in Fig. 15(b), demonstrating a significant degradation in linearity (>60 dB) without the mismatch shaping algorithm. This also shows that the noise shaping is degraded below 10 kHz due to DEM's first-order mismatch shaping. This degradation was unexpected and indicates that the DAC mismatch is higher than the 0.25% anticipated. The authors believe that a 0.5% mismatch, which would decrease the SQNR to about 95 dB, as illustrated in the noise breakdown, causes a significant loss in performance as the quantization and DAC error shaping contributes to about 40% of the input-referred noise. The flicker noise corner is at \sim 60 Hz due to the CCO, which cannot be chopped. It was sized to have symmetric rise and fall times while maximizing the area. However, the flicker noise still contributes $\sim 15\%$ of the ADC's noise. The DR was characterized by sweeping the input amplitude, achieving a 92.1-dB DR, as shown in Fig. 15(c). The SNDR was then measured with a full-scale input sinusoid from 50 to 2.5 kHz, where <0.5-dB variation was observed [see Fig. 16]. Due to the high number of bits in the internal quantizer, the SNR and DR should have similar values.

The ADC's linearity was measured across the ADC's BW and dominated by the third-order harmonic distortion (HD3). As shown in Fig. 17, the maximum in-band HD3 is 119.6 dBc.



Fig. 16. Measured ADC SNDR across its bandwidth.



Fig. 17. Harmonic distortion (HD2 and HD3) as a function of frequency.



Fig. 18. Measured intermodulation distortion.

Above 833 Hz, the third harmonic lies out of band, whereas the second harmonic (HD2) remains below 121 dBc up to $f_s/2$. The measured intermodulation distortion (IMD) was 114.2 dB with -6-dBFs inputs at 789 and 961 Hz, as shown in Fig. 18, limited by the APx555B, which only guarantees the IMD residual to be <110 dB.

CT- $\Delta\Sigma$ ADCs are also known to exhibit anti-alias filtering behavior, enabling them to filter out-of-band signals and avoid noise folding. This attribute was measured, and the results are shown in Fig. 19 for a -33-dBFS (40 mV_{pp}) input signal from f_s – BW to f_s + BW (BW = 2.5 kHz). The tone folded back in-band was measured, and the rejection in-band was ~42 dB. This is lower than a third-order CIFB structure due to the FF paths. The anti-alias filtering is also reduced by the dead-band switch at the input, which operates at f_s and demodulates part of the signal back in-band before the loop can filter it out [31]. It should be noted that with an OSR of 80, adding a first-order low-pass filter at the input would provide an extra 38 dB of filtering at f_s , bringing the total to 80 dB.

B. Robustness to Variation

Achieving robust performance with a VCO-based ADC is a well-known challenge due to its open-loop nature and the





Fig. 20. Measured ADC (a) PSRR and (b) CMRR.



Fig. 21. Measured ADC SNDR across analog supply voltage.

coefficients being set by $G_{\rm m}$ and $K_{\rm CCO}$ (1), which are notoriously sensitive to process, voltage, and temperature (PVT) variation. This sensitivity can cause the loop coefficients to vary significantly with temperature and process. This was partially addressed in the system's design, where a constant- $G_{\rm m}$ biasing circuit was used to stabilize $G_{\rm m}$, and current-starving the CCO guarantees a supply-independent swing. Simulations show that the loop coefficients vary by $\pm 10\%$ with process and temperature (0–70 °C) and by less than 0.2%/V with supply variation. As shown previously, $f_{\rm CCO}$ variation is also acceptable (provided $f_{\rm CCO} > 2f_{\rm s}$), minimally degrading the SQNR.

The loop coefficients were tuned manually to the correct operating point post-fabrication by controlling the current in the $G_{\rm m}$ -cell and the pulsed current sources. This robustness with supply voltage variation is shown in Fig. 20, where the measured PSRR with a 100-mV_{pp} tone added to $V_{\rm DD}$ and the CMRR with a full-scale common-mode sinusoidal input stay above 80 dB from dc to 5 kHz. The SNDR was also measured as a function of the supply voltage from 0.7 to 1 V, as shown in Fig. 21, where the performance varied by less than 1 dB



Fig. 22. Measured SNDR and SFDR (n = 6 devices).



Fig. 23. Measured SNR (blue) and SFDR (orange) as a function of temperature and simulated SFDR of chopping switch (orange dash).

between 0.75 and 0.95 V, demonstrating the ADC's robustness. The steep degradation at higher supply voltages is due to the CCO level shifters failing and missing edges.

To assess the performance variation of the ADC across different dies, the loop parameters were optimized for a specific device (Device #3), and then, the same control bits were used on the other devices. Fig. 22 shows the measured SNDR and SFDR, where the average SNDR and SFDR were 90.7 and 119.5 dB, respectively. Optimizing the loop parameters separately for each device exhibited a 1-dB improvement in performance mainly due to SQNR improvement and mismatch noise folding reduction. This shows good performance across multiple devices and the loop's reliability across process variation and mismatch.

The ADC's temperature resilience was characterized across the commercial range (0–70 °C) by placing the device in a temperature chamber (Test Equity model 106) without any calibration or retuning of the loop parameters. As shown in Fig. 23, the SNR varies negligibly, by only 1 dB, across the entire temperature range, demonstrating the robustness of the proposed design. The linearity stays above 117 dB for temperatures below 50 °C but degrades significantly at higher temperatures. This degradation with temperature was verified in simulation and found to be caused by leakage of the bootstrapped voltage circuit that drives the input chopping switches. The gate voltage drops below the maximum input voltage, which causes nonlinearity due to leakage through the chopping switches. The simulated chopping switch SFDR (with all other blocks ideal) is overlaid on the measured SFDR,



Fig. 24. Measured output spectra with no input at 0, 20, and 70 °C.



Fig. 25. CT- $\Delta\Sigma$ ADC state-of-the-art landscape.

exhibiting good agreement between simulation and measurement. This degradation could be avoided by increasing the bootstrapping capacitor to ensure a constant voltage, even at higher temperatures. Finally, to demonstrate the correct operation of the loop across temperature, spectra were recorded with shorted inputs at 0, 20, and 70 °C. As shown in Fig. 24, the third-order noise shaping is maintained, and the noise floor stays nearly constant across the temperature range.

C. Comparison to the State-of-the-Art

Table I compares recently published high-performance timeand voltage-domain ADCs. This work is the first third-order VCO-only ADC enabling low supply voltage operation and high DR. The DAC reference voltage was increased to 1.2 V to maximize the input range and allow a large differential swing of 1.8 V_{pp} . When operating the DAC at 0.8 V, the SNDR decreases by 2 dB, and the maximum differential input range decreases to 1.2 Vpp. The SNDR does not decrease by the expected 3.5 dB since the ADC noise is dominated by the CDAC mismatch, not the thermal noise. The reduced swing at the PVG due to the smaller reference voltage also allows for a more aggressive g_m/I_D in the first integrator. Due to the PVG FF technique, extremely high linearity (>119.6 dB) and SNDR (92.1 dB) were achieved while consuming just 4.4 µW. As apparent from the table, the performance of the reported $\Delta\Sigma$ ADC approaches that of voltage-domain $CT-\Delta\Sigma$ modulators and achieves the highest Schreier FoM among time-domain architectures. Fig. 25 plots the Schreier

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	JSSC	VLSI	JSSC	ISSCC	JSSC	JSSC	ISSCC	This Work
	2018 [31]	2021 [2]	2020 [22]	2022 [38]	2019 [20]	2021 [17]	2021 [33]	
Integration domain	Voltage	Voltage	Hybrid	Hybrid	Time	Time	Time	Time
Topology	3 rd -ord.	3 rd -ord.	2^{nd} -ord.	2^{nd} -ord.	1 st -ord.	1 st -ord.	2^{nd} -ord.	3 rd -ord.
Technology [nm]	65	28	65	65	40	65	65	65
Area [mm ²]	0.053	0.12	0.078	0.108	0.025	0.075	0.075	0.1
Supply (A/D) [V]	1.2	0.6	1	0.7	0.8 / 0.6	0.8	1.2 / 0.8	0.8
Power [µW]	4.5	33.6	6.5	5	4.5	1.68	5.8	4.4
DAC type	Capacitive	Resistive	Resistive	Capacitive	Capacitive	Capacitive	Capacitive	Capacitive
Input range [V _{pp}]	1.77	0.8	0.3	0.56	0.1	0.46	0.4	1.8
Sampling freq. [kHz]	400	12,800	1,280	2,560	2,500	64	200	400
BW [kHz]	5	40	10	10	10	0.5	1	2.5
CMRR [dB]	N/A	55	76	88	83	97	89	80-93
SNDR [dB]	93.5	83	80.4	85.1	78.5	94.2	92.3	92.1
DR [dB]	96.5	86.5	81	87.3	79	95.1	92.3	92.1
SFDR [dB]	101.4	94.2	92.2	97.1	91	128	110.3	119.6 (min) – 123 (peak)
FoM _{SNDR} [dB]	184	173.8	172.3	178.1	172	178.9	174.7	179.6

 TABLE I

 Performance Summary and Comparison to the State-of-the-Art

FoM (FoM_{S,SNDR}) of ADCs with BWs below 50 kHz as a function of their Nyquist frequency ($f_{s,nyq}$). The reported ADC significantly advances the state-of-the-art.

V. CONCLUSION

This work demonstrates a feedforwarding technique that enables a highly efficient third-order VCO-only ADC by linearizing the 1st integrator and removing the need for inner feedback DACs. The ADC structure is robust, maintaining performance over a wide temperature and supply voltage range. This PVG FF technique can be generalized to higher order architectures or used with other open-loop integrators such as a G_m -C, which would also benefit from the linearization and improved coefficient scaling offered by the PVG FF technique. This ADC is the first high linearity, single-loop third-order ADC with time-only integrators, and it achieves a state-ofthe-art 179.6-dB FoM among VCO-based ADCs and a 123-dB peak SFDR while operating from a low supply voltage. This work demonstrates that time-based modulators are competitive with standard voltage-domain architectures.

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