A Near-Zero-Power Wake-Up Receiver Achieving −69-dBm Sensitivity

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***Abstract*— This paper presents the design of a wake-up receiver (WuRX) that both improves sensitivity and reduces power over prior art through a multi-faceted design featuring an off-chip impedance transformation network with large passive voltage gain, an active envelope detector with high input impedance to facilitate large passive voltage gain, a low-power precision comparator, and a low-leakage digital baseband correlator. Implemented in a 180-nm silicon on insulator CMOS process using dynamic threshold-voltage MOSFET (DTMOS) devices, the OOK-modulated WuRX operates at 113.5 MHz and achieves a sensitivity of −69 dBm, while consuming just 4.5 nW from a 0.4-V supply.**

***Index Terms*— Low-power wide area network (LPWAN), low-power wireless, near-zero-power, wake-up radios, wake-up receivers (WuRXs).**

I. Introduction

THE high-power consumption of conventional low-power wide area network (LPWAN) receivers employed in applications such as smart meters, environmental sensors, threat monitors, and other Internet of Things (IoT) like applications often dictates overall device battery life. Even though many such applications communicate at low-average throughputs, the power of the radio can be high due to the need for frequent network synchronization [1]. To reduce the power consumption, wake-up receivers (WuRXs), which tradeoff sensitivity and/or data rate for low-power operation, ideally without seriously compromising interference resilience, have been proposed to monitor the RF environment and wake up a high-performance (and higher power) conventional radio upon the reception of a predetermined wake-up packet.

The two most important metrics for WuRXs used in low-average throughput applications are the power consumption and sensitivity, as the power of always-on WuRXs ultimately determines the battery life of low-activity devices, while sensitivity determines the communication distance and, therefore, the deployment cost via the total number of nodes required to achieve a given network coverage. Typically, sensitivity and power consumption tradeoff with one another, making the design of WuRXs that simultaneously achieve both challenging. Interference resilience is also an important metric for WuRXs, since false alarms cause unwanted power dissipation in sensor nodes, while missed detections result in sensor network malfunctions. Unlike conventional mobile receiver design, metrics such as physical size and data rate can often be exploited to improve sensitivity or reduce power, as will be shown shortly.

WuRXs can be loosely classified into two categories based on whether or not a mixer is present. Mixer-based WuRXs tend to utilize a local oscillator (LO), generated via a phase-locked loop (PLL) [2], injection locking from a crystal or high-Q resonator [3], or an uncertain free-running ring oscillator [4], [5] or LC oscillator [6], to mix down incoming RF energy to a known [2], [3] or uncertain [4]–[6] intermediate frequency (IF). Mixing down to an IF allows more efficient amplification than at RF, and thus, such approaches often forgo inclusion of any RF low noise amplifiers (LNAs), at the expense of an increased system noise figure. This approach is advantageous in terms of sensitivity and interference resilience, as it is generally possible to design sharp, yet low power, IF filters to knock out RF and circuit noise, along with interfering blockers. However, LO generation requires significant power, and thus, mixer-based architectures are generally used in applications where μW power levels are acceptable.

On the other hand, direct envelope detection architectures, which forgo LO generation/mixing and instead demodulate directly to baseband, can achieve much lower power than mixer-based designs [7]–[9]. However, since envelope detectors (EDs) demodulate all energy present at their inputs to baseband, such architectures tend to accumulate significant noise and interference, making their sensitivity generally inferior to mixer-based architectures.

This paper presents the design of a WuRX that targets LPWAN applications and, therefore, attempts to achieve both low power and high sensitivity with reasonable interference resilience through a combination of techniques including careful selection of the carrier frequency and data rate, inclusion of a high-Q RF impedance transformer/filter that delivers passive voltage gain as well as interference filtering, a high input impedance and high conversion gain ED, a precise, yet low-power, regenerative comparator, and an optimized digital correlator that provides coding gain while combating false

Manuscript received June 30, 2017; revised January 29, 2018 and February 21, 2018; accepted February 22, 2018. This paper was approved by Guest Editor Kenichi Okada. This work was supported by DARPA under Contract HR0011-15-C-0134. *(Corresponding author: Drew A. Hall.)*

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Digital Object Identifier 10.1109/JSSC.2018.2815658

alarms caused by interferers. This architecture was originally presented in [10]; this paper provides significant additional circuit design details and measurement results. The overall WuRX architecture is presented in Section II, while Section III describes the implemented off-chip transformer and circuits. Section IV presents measurement results, followed by a figure-of-merit (FoM) landscape of state-of-the-art WuRXs in Section V. Finally, Section VI concludes this paper.

II. Wake-Up Receiver Architecture

A. Overview

The architecture of the proposed WuRX is shown in Fig. 1. The primary optimization objective of this design was to minimize power. This motivated the use of a direct ED WuRX architecture operating at a low supply voltage (0.4 V in this work). However, the secondary objective was to achieve sensitivity that approaches that of a mixer-based WuRX architecture, while not significantly compromising tolerance to interferers. This was accomplished through a number of architectural and circuit design techniques described as follows.

B. Direct Envelope Detection RF Front-End Optimizations

Direct ED architectures demodulate all input RF energy to baseband, and thus, any interferers within the input RF bandwidth can inhibit proper reception. In addition, the lack of an LNA together with very low-power demodulating circuits means that the baseband circuit noise often dominates, thereby ultimately limiting the WuRX sensitivity. Fortunately, these two problems, i.e., interference and baseband circuit noise, can be overcome via the following techniques:

1) Minimizing Interference via High-Q Filtering: To reduce the impact of in-band blockers in direct-ED or uncertain-IF mixer-based architectures, a high-Q narrowband filter is needed to minimize RF bandwidth and block interferers. Most prior-art low-power radios accomplish narrowband filtering by utilizing high-Q mechanical resonators, which offer attractive narrow filtering capability at 1–3 GHz [4], [11]. In this design, however, to attain the highest possible Q for sharp filtering, and, as will be seen shortly, to achieve a large impedance transformation ratio from a 50-Ω source as well as wide communication range, a carrier frequency in the 100-MHz range was selected for use near the FM radio band. Therefore, a high-Q filter (and, as will be described shortly, transformer) was designed out of lumped components directly.

2) Minimizing Baseband Circuit Noise via Passive RF Voltage Amplification: EDs are inherently non-linear elements. Unlike linear mixers used for down-conversion, the squaring operation of an ED converts pre-ED noise down to baseband via two mechanisms: self-mixing of noise and noise convolved with the input signal [12]. Since most ultralow-power WuRXs forgo active gain before the ED, sensitivity is typically limited by baseband noise. Therefore, to improve sensitivity without a power penalty, most direct ED WuRX designs strive to achieve as much passive voltage gain in the matching network as possible. This is typically achieved by designing the ED to have a large input impedance, and matching this large impedance to 50 Ω via an impedance transformation network.

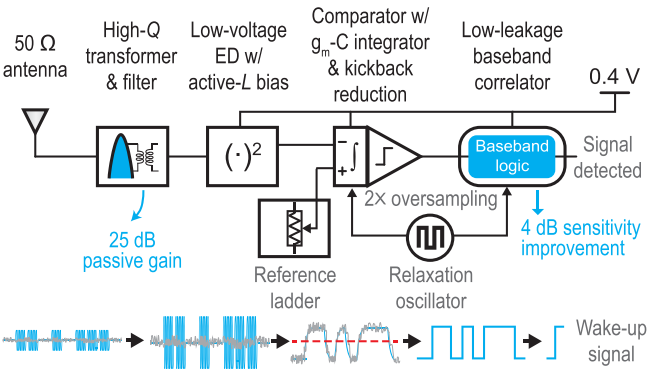

Fig. 1. Overview of the proposed WuRX.

Prior work has shown 5 and 12 dB of passive voltage gain which, when coupled to either a rectifier or an active ED, achieved sensitivities of −45.5 and −41 dBm at 12.5 and 100 kbps at powers of 116 and 98 nW, respectively [7], [8]. Thus, direct ED systems can achieve ultralow-power operation, yet without large RF voltage gain and low-noise baseband circuits, do so at limited sensitivities.

To address the aforementioned issues, the proposed WuRX incorporates an ED with a high input impedance that, combined with a high-Q impedance transformer, facilitates up to 25 dB of passive voltage gain at RF before being demodulated by the ED, thus directly resulting in a 25-dB improvement in sensitivity compared to the exclusion of this transformer. Furthermore, the ED is designed to support high conversion gain to further reduce the impact of baseband circuit noise (i.e., to increase the SNR).

C. Baseband Bandwidth Considerations

There are two primary classes of applications where WuRXs can be useful: 1) high-average throughput applications with asynchronous communication needs where WuRXs are primarily used to eliminate the need for precision watchdog timers that perform network synchronization and 2) low-average throughput applications where the network is largely idle, waiting for an event to occur such as in infrastructure, perimeter, and health alarm monitoring. In high throughput applications, it is important to minimize wake-up detection latency, set in part by the WuRX data rate, so as to not adversely affect the average network throughput. In low throughput applications, wake-up latency (and thus the data rate of the WuRX), is less important, as long latency does not adversely affect the overall throughput needed. Most conventional WuRX designs target the first class of applications; this paper instead focuses on the design of WuRXs used in low-average throughput LPWAN applications. One of the key ideas of a LPWAN is to leverage the reduced data rate (and thus integrated baseband noise) to improve sensitivity and enable wide communication range. For example, LoRaWAN utilizes a 300 bps to 50 kbps data rate, whereas Sigfox is only 100 to 600 bps. Therefore, a 300 bps data rate was selected for this design.

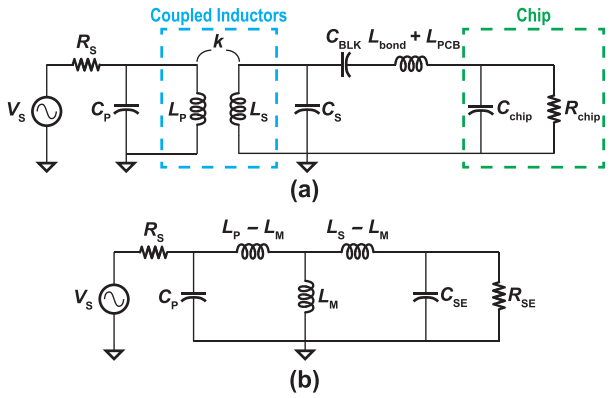

Fig. 2. Schematics of (a) transformer/filter and (b) equivalent circuit model.

D. Digital Baseband Processing

The received RF signal employed in this design is modulated with a custom designed 16-bit sequence. After rectification the demodulated signal is 2× oversampled and digitized by a 1-bit regenerative comparator. The output of the comparator feeds a digital correlator that computes the Hamming distance between the received and stored sequences. When the Hamming distance is below a programmable threshold (H_{th}), a wake-up signal is generated. It will be shown in Section IV that the use of this wake-up sequence provides additional coding gain that improves the sensitivity of the proposed WuRX. Moreover, the correlator prevents false alarms caused by unwanted jammers. An on-chip relaxation oscillator provides the required 600-Hz clock.

III. Circuit Implementation

A. Transformer/Filter

The purposes of the transformer/filter is to impedance transform a 50-Ω source impedance to a much larger value to facilitate passive voltage gain, while also performing high-Q RF filtering. The schematic of the implemented transformer/filter is shown in Fig. 2(a) where R_S is the 50-Ω source impedance. The primary stage resonator is formed by L_P and C_P, while the secondary stage is formed by L_S and C_S, with k denoting the coupling coefficient between L_P and L_S. C_{chip} and R_{chip} are the equivalent input impedance of the chip at the carrier frequency, which connects to the transformer/filter via a large ac-coupling capacitor, C_{BLK}, and a small parasitic inductor from the printed circuit board (PCB) trace and bondwire. Both the primary and secondary stage tanks resonate at the same frequency, $f_{\text{RF}} = 113.5$ MHz. Departing from a traditional two-port RF filter, which has 50 Ω matching at both ports, the proposed transformer/filter not only provides a second-order filter response for interference rejection but also realizes impedance transformation between the two ports to achieve passive voltage gain. To analyze the circuit, an equivalent circuit model is derived as shown in Fig. 2(b). L_M is determined by k and can be written as [13]

$$L_M = k \cdot \sqrt{L_P L_S} = k \cdot L_S \cdot \sqrt{\frac{1}{N}} \tag{1}$$

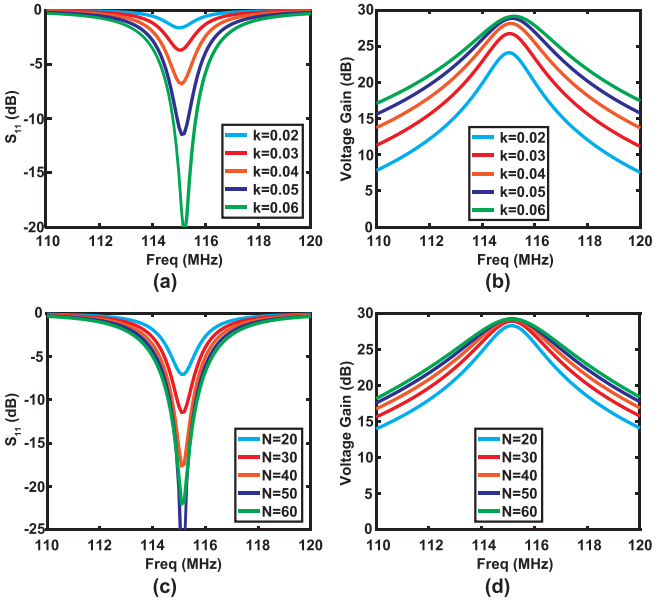

Fig. 3. (a) S_{11} versus k. (b) Voltage gain versus k. (c) S_{11} versus N. (d) Voltage gain versus N.

where N is the turn ratio between L_P and L_S. C_{SE} and R_{SE} are the equivalent capacitor and resistor of the secondary stage, with $C_{\text{SE}} = C_S + C_{\text{chip}}$ and $R_{\text{SE}} = R_{\text{EQ,P}} || R_{\text{chip}}$, respectively, where $R_{\text{EQ,P}}$ is due to the finite quality factor (Q) of L_S. Therefore, the maximum passive voltage gain the transformer/filter can achieve at f_{RF} is

$$\text{Gain}_{\text{max}} = \sqrt{\frac{R_{\text{SE}}}{R_S}} = \sqrt{\frac{R_{\text{EQ,P}} || R_{\text{chip}}}{R_S}}. \tag{2}$$

To get large passive voltage gain, a large $R_{\text{EQ,P}}$ must be achieved by either increasing Q or L_S for a given C_{SE}. Since Q can only be pushed so high using practical inductors, L_S is the only practical tunable parameter. There are two things that limit the achievable value of L_S: 1) the chip input capacitance, C_{chip} and 2) the self-resonant frequency of the inductor. With $C_S = 0$ pF and $C_{\text{chip}} = 1.8$ pF, the maximum L_S is 1.06 μH. Due to the size of the required inductor, it must be off-chip. For commercial inductors with high Q, self-resonance typically occurs when $\omega L \approx 1,400$ Ω. To account for variation in C_{chip} and on-board parasitics, $\omega L = 520$ Ω was chosen. From the datasheet of the selected inductor [14], a Q of 150 can be obtained at 115 MHz, and thus $R_{\text{EQ,P}} < 78$ kΩ.

After determining the value of L_S and C_S, we considered the coupling coefficient k and the turn ratio N, both of which affect the input matching and passive voltage gain. To have a sharp filter response for out-of-band interference rejection, k should be small and Q should be large [15]. Fig. 3(a) and (b) shows calculated S_{11} and voltage gain of the transformer/filter varying k with N fixed to be 30. When k is increased from 0.02 to 0.06, the input matching gets better and the voltage gain increases. However, the filter bandwidth also increases. Fig. 3(c) and (d) shows calculated S_{11} and voltage gain varying N with $k = 0.05$. When N is increased from 20 to 60, the voltage gain does not increase much, but with considerably

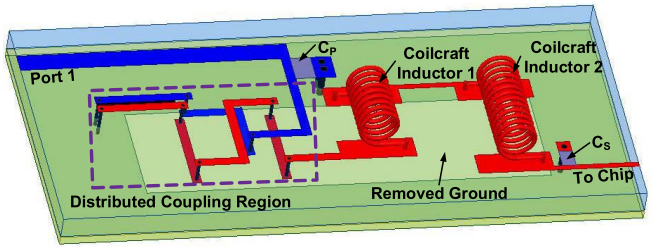

Fig. 4. 3-D model of the transformer/filter.

larger filter bandwidth. Therefore, $k = 0.05$ and $N = 30$ were chosen as a compromise between input matching, voltage gain, and filter bandwidth. Calculations show that S_{11} is better than -10 dB with a passive voltage gain of 28.9 dB and a 3-dB bandwidth of 2.4 MHz.

The key challenge in implementing the proposed transformer/filter is to control the coupling despite the large difference in inductance (24 and 720 nH). Implementing the inductors using only lumped elements would make it very hard to control the coupling through positioning, whereas only distributed inductors would take too much area. As such, we used a combination of lumped inductors (160 and 220 nH from Coilcraft) and a distributed inductor to realize L_S and a distributed inductor to realize L_P, which has three advantages. First, L_S is realized by both distributed and lumped inductors, thus the value can be large. Second, the coupling is realized by the distributed parts of L_P and L_S, and thus, k is determined by the length and gap of the coupling PCB traces. With modern PCB fabrication techniques, this coupling can be controlled precisely, which is crucial since k affects both passive gain and filter bandwidth. Third, the use of both lumped and distributed inductors provides more freedom to design the transformer. For example, the center frequency can be easily tuned by replacing lumped components, which is an advantage compared to mechanical resonators [4], [11].

Fig. 4 shows the 3-D model of the transformer/filter. To reduce the dielectric loss, a Rogers RO4003C substrate was used ($\epsilon_r = 3.55$, thickness of 20 mil, and a loss tangent of 0.0027). From HFSS simulations, we found that at 115 MHz, L_P and L_S are 28 and 756 nH, respectively, and $k = 0.05$. All of the component values are close to the desired values from calculation. The simulated voltage gain was 26.6 dB with a bandwidth of 2.2 MHz.

B. Envelope Detector

To take full advantage of the gain provided by the transformer/filter, the ED must provide a large enough input resistance R_{chip} so as to not to degrade the corresponding $R_{EQ,P}$. Although a passive N-stage RF rectifier [7], [9] is a tempting choice (due to the zero power consumption), it is difficult to achieve high enough R_{chip}. Thus, in this work, an active ED was selected. A transistor biased in the sub-V_t region can not only operate with a low supply voltage and low-power consumption but also provides an exponential voltage–current relationship. Assuming that the transistor is operating in the sub-V_t saturation region (i.e., $V_{DS} > 100$ mV) with

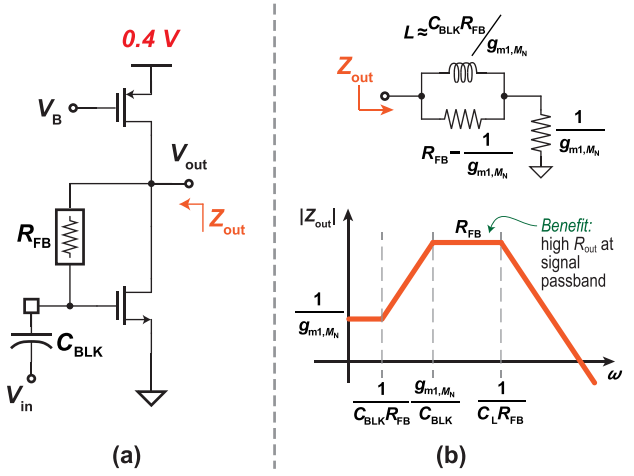

Fig. 5. (a) Schematic of proposed active-L-biased ED. (b) Active-L biasing circuit model and Bode plot of ED output impedance.

negligible drain-induced barrier lowering (DIBL), the current can be written as [16]

$$i_{DS} = \mu C_{ox} \frac{W}{L}(n-1)V_T^2 \, e^{\frac{v_{GS}-V_t}{nV_T}} \tag{3}$$

where μ is the mobility, C_{ox} is the oxide capacitance, W is the transistor width, L is the transistor length, n is the sub-V_t slope factor, V_T is the thermal voltage (k_BT/q), and v_{GS} is the gate-to-source voltage. This exponential relationship results in a second-order non-linearity used for the desired ED functionality. The second order transconductance is given as

$$g_{m2} = \frac{1}{2} \cdot \frac{\partial^2 i_{DS}}{\partial v_{GS}^2} = \frac{I_{DS}}{2(nV_T)^2}. \tag{4}$$

In an silicon on insulator (SOI) process, the floating body can be connected to the gate directly without using deep n-well devices, commonly referred to as the dynamic threshold-voltage MOSFET (DTMOS) configuration [17], to achieve additional second order non-linearity via threshold voltage modulation. The additional transconductance can be derived as

$$g_{mb2} = \frac{1}{2}\frac{\partial^2 i_{DS}}{\partial v_{BS}^2} = (n-1)^2 \cdot g_{m2}. \tag{5}$$

For the process used in sub-V_t, $n \approx 1.4$, meaning that the DTMOS configuration provides an additional 16% transconductance compared to gate input only.

Conventional common source ED biasing schemes use either a diode-connected load or a resistive load. Unfortunately, the diode connected load results in a low output resistance (similar to a source follower ED) and only achieves high conversion gain with large input signals, while a resistive load has limited conversion gain with a 0.4-V supply voltage. Other techniques such as a cascode level shifter provide high output resistance, but require extra voltage headroom [8] not compatible with the employed 0.4-V supply.

To address the aforementioned issues, an active-L self-biased ED was designed [Fig. 5(a)]. The feedback resistor sets the dc voltage for both the gate and drain nodes of the

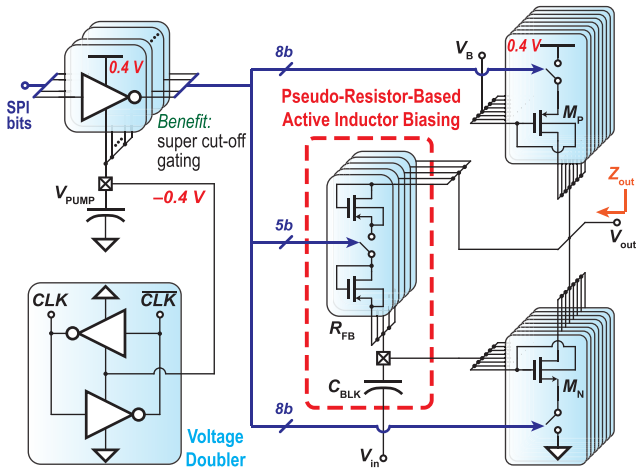

Fig. 6. Full schematic of the proposed low-voltage active-L-biased DTMOS ED with boosted binary-weighted SPI control.

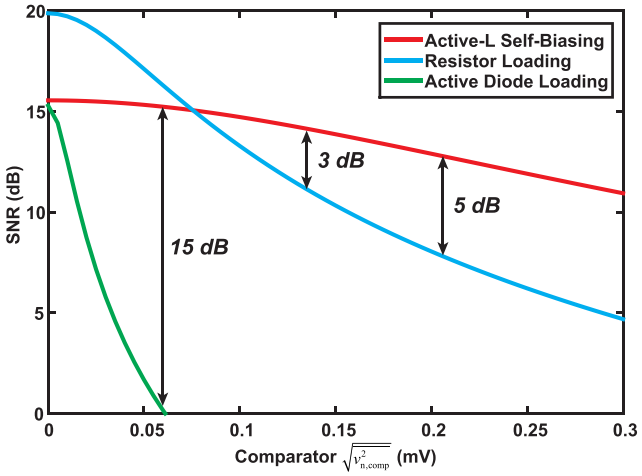

Fig. 7. Simulated ED output SNR versus integrated comparator noise voltage for different biasing schemes.

input transistor and serves as the output impedance. The output impedance can be written as

$$Z_{\text{out}} = \left(\frac{g_{\text{m1}} + sC_{\text{BLK}}}{1 + sC_{\text{BLK}}R_{\text{FB}}} + \frac{1}{r_{\text{o}}} + sC_{\text{L}} \right)^{-1} \tag{6}$$

where g_{m1} is the transconductance of the NMOS, C_{BLK} is the ac-coupling capacitor, R_{FB} is the feedback resistor, r_{o} is the small-signal intrinsic output resistance of the transistor, and C_{L} is the capacitance at the output node. Assuming $r_{\text{o}} \gg 1/g_{\text{m1}}$ and $r_{\text{o}} \gg R_{\text{FB}}$ because of the low current (5 nA in this design, which results in $r_{\text{o}} \approx 1$ GΩ and $1/g_{\text{m1}} \approx 7$ MΩ), $C_{\text{BLK}} \gg C_{\text{L}}$, and $C_{\text{BLK}}/g_{\text{m1}} \gg C_{\text{L}}R_{\text{FB}}$, (6) can be simplified to

$$Z_{\text{out}} \simeq \frac{1}{g_{\text{m1}}} \cdot \frac{1 + sC_{\text{BLK}}R_{\text{FB}}}{\left(1 + s\frac{C_{\text{BLK}}}{g_{\text{m1}}}\right)(1 + sC_{\text{L}}R_{\text{FB}})} \tag{7}$$

which contains two poles and one zero. The equivalent circuit model and Bode plot of Z_{out} are shown in Fig. 5(b). It can be seen that the output impedance is boosted to R_{FB} within the signal passband due to the active-L biasing, which leads to higher conversion gain. Since non-return-to-zero (NRZ) signaling is used, the high pass corner must be low enough to not attenuate the signal power and was set to 20 mHz in this design for <0.01 dB SNR degradation from baseline wander. Therefore, an off-chip C_{BLK} was used as a dc block and incorporated into the bias network.

The full ED schematic is shown in Fig. 6. Due to significant process variation in sub-V_{t} circuits, both M_{N} and M_{P} were designed to have 8-bit binary-weighted tuning capability. To reduce the leakage of unused M_{N} via super-cutoff biasing, and to turn on M_{P} strongly, a voltage doubler [18] was designed to provide −0.4 V, saving up to 3 nA in simulation (in the TT corner). Because of the high required value of the feedback resistor, a MOS-bipolar-pseudoresistor was used instead of a poly resistor to prevent high capacitive loading of the input node at RF, which ultimately limits the achievable inductor value of the second stage of the transformer/filter, and therefore passive voltage gain. For the same reasons as above, and to make the baseband bandwidth tunable, the pseudoresistor was implemented with 5 binary-weighted bits. Since the baseband bandwidth is 300 Hz, all critical transistors were sized to trade-off the contributions of $1/f$ noise while minimizing parasitic capacitance at the output node, the latter of which ultimately limits the achievable R_{FB} to ∼100 MΩ.

The demodulated output signal of the ED is

$$v_{\text{out}} = \text{Conv}_{\text{Gain}} \cdot v_{\text{in}} = \frac{k_{\text{ED}}}{2} \cdot v_{\text{in}}^2 \tag{8}$$

where $\text{Conv}_{\text{Gain}}$ is the conversion gain of the ED, v_{in} is the input signal amplitude, and k_{ED} is the ED scaling factor (in units of $1/V$). Combining (4), (5), and (7), the k_{ED} of the designed ED in the signal passband is given as

$$\begin{aligned} k_{\text{ED}} &= (g_{\text{m2}} + g_{\text{mb2}}) \cdot Z_{\text{out}} \\ &\simeq [1 + (n-1)^2] \cdot \frac{I_{\text{DS}}}{2(nV_{\text{T}})^2} \cdot R_{\text{FB}} \end{aligned} \tag{9}$$

which is only dependent on design parameters.

To compare the two conventional biasing schemes with the proposed active-L biasing scheme, the SNR at the ED output was calculated. Assuming that all three biasing schemes use the same DTMOS configuration as the input stage, the SNR can be written as

$$\text{SNR} = \frac{(g_{\text{m2}} + g_{\text{mb2}})^2 \cdot \frac{v_{\text{in}}^4}{4} \cdot R_{\text{out}}^2}{\overline{i_{\text{n,ED}}^2} \cdot R_{\text{out}}^2 + \overline{v_{\text{n,comp}}^2}} \tag{10}$$

where $\overline{i_{\text{n,ED}}^2}$ is the total integrated noise current of the ED input transistor, R_{out} is the output resistance in the passband, and $\overline{v_{\text{n,comp}}^2}$ is the total input-referred noise of the comparator. It can be shown that if the ED loading and comparator are noiseless, the SNR is independent of R_{out} and all the biasing schemes would have the same SNR. However, if $\overline{v_{\text{n,comp}}^2}$ is significant compared to the ED noise, higher R_{out}, and therefore, higher k_{ED} lead to better SNR. Simulation with an ED current of 5 nA and a 3.2-mV input signal for these three bias schemes is depicted in Fig. 7. When the comparator noise is large, the active-L self-biased scheme achieves the highest SNR.

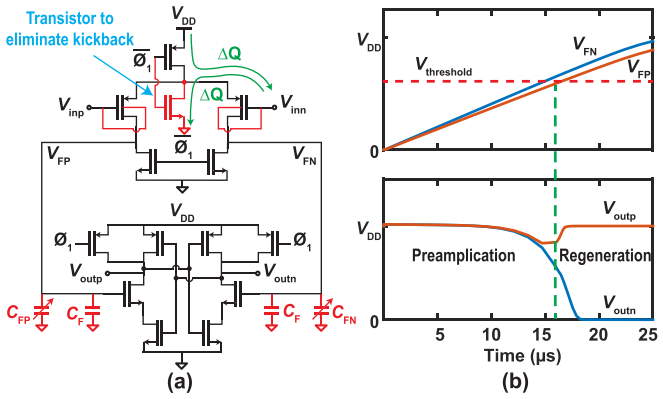

Fig. 8. (a) Schematic of the dynamic two-stage comparator. (b) Simulation showing first and second stage output voltages.

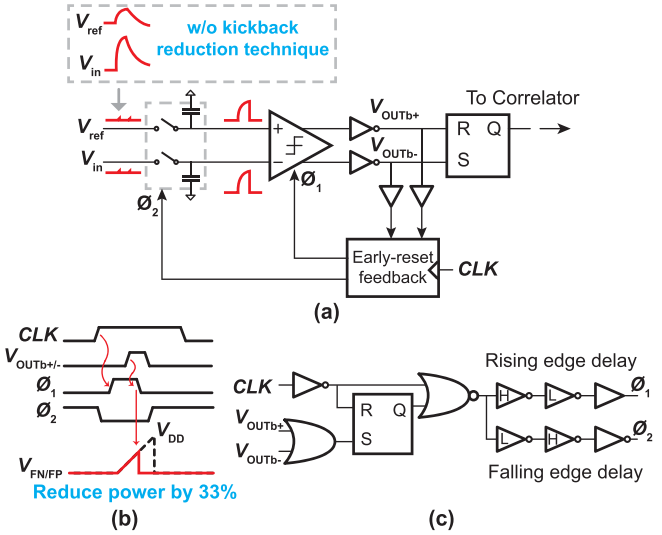

Fig. 9. (a) Schematic of the comparator, S/H stage, and clocking. (b) Timing diagram of the early reset feedback. (c) Schematic of the early reset feedback.

C. Comparator and S/H Stage

The output of the ED is digitized by a comparator, which serves as a 1-bit quantizer. Due to the 2× oversampling, the comparator operates at 600 Hz. The comparator is implemented with a g_mC integrator as a preamplifier followed by a regenerative latch [19]. The operation is as follows: 1) once $\overline{\phi}$ goes low, a current determined by the inputs is integrated on C_F until 2) the voltage crosses the latch threshold voltage, $V_{threshold}$, after which the positive feedback latch regenerates producing complementary rail-to-rail outputs. The two-stage dynamic comparator is then reset by the other phase of the clock and ready for the next cycle.

The preamplifier is typically designed with a moderate integration gain of ∼5 V/V to suppress the latch input-referred noise. Therefore, the preamplifier usually dominates the noise performance of the entire comparator. As can be observed in [19], adding matched capacitance at the preamplifier output prolongs the integration time and limits the preamplifier noise bandwidth, which effectively reduces the comparator noise. In this design, a 480-fF metal-insulator-metal (MIM) capacitor was used and placed in a common centroid layout to ensure good matching. Compared with the same comparator without explicitly loading the preamplifier, the noise power is reduced by 8×, while the power consumption increases by only 5× in simulation because of the $C_F V_{DD}^2$ energy. Since the comparator is operating at a low speed and the dynamic power of the preamplifier is minimal, loading the preamplifier results in a good noise versus power tradeoff. Moreover, as shown in Fig. 8(a), the input pair also uses a DTMOS configuration, which increases the transconductance resulting in a lower input-referred noise at no power cost. Simulation showed that the effective transconductance increased by 51% and the noise power reduced by 66%. With the help of the preamplifier loading and increased transconductance, the simulated comparator noise was suppressed from 505 to 104 μV_{RMS}.

The comparison threshold voltage is tuned with a dual 5-bit binary weighted capacitor DAC (CDAC) in parallel with C_F. By changing the load capacitance, the comparator offset voltage changes accordingly. Assuming the capacitance difference between the two outputs (ΔC_F) is much less than C_F, the comparison threshold voltage can be written as

$$v_{os,DAC} = \frac{\Delta C_F}{C_F} \cdot n \cdot V_T. \tag{11}$$

Thus, the threshold voltage increases linearly with ΔC_F, and is constant after the CDAC is configured. The CDAC uses metal-oxide-metal (MOM) capacitors with a unit capacitance of 3.7 fF ($C_F = 0.65$ pF), corresponding to ∼200-μV resolution. A reference ladder provides a voltage reference to the negative terminal of the comparator. The reference ladder contains 64 diode-connected PMOS transistors in series. A 5-bit MUX selects the output node as the reference voltage, providing a tuning step size of 6.25 mV and a range of 200 mV.

The biggest challenge with this dynamic architecture is the comparator kickback via C_{gs}, C_{bs}, C_{gd}, and C_{bd}. Due to the unbalanced output impedances of the ED (∼100 MΩ||1.7 pF) and the reference ladder (∼2 GΩ||50 pF), the kickback charge introduces unequal voltage perturbations. This voltage difference would lead to a comparison error in subsequent cycles since the time constant at both nodes is much larger than one clock period. To eliminate this error, two techniques were implemented.

1) An additional reset transistor was placed at the source of the input pair, which ensures that V_{gs} always resets to V_{DD}, such that the same amount of charge is injected into the input when ϕ is asserted high and is removed when ϕ is deasserted (Fig. 8). This results in zero net kickback charge into the ED and reference ladder during each cycle, preventing incomplete settling.
2) A S/H stage was added in front of the comparator that provides matched impedances for both inputs and temporarily stores the kickback charge. The sampling capacitor is 1.9 pF, much larger than the parasitic capacitance of the input transistor. Therefore, the only kickback effect is a ∼2-mV common-mode spike at the comparator input, which does not lead to a comparison error. The sampling capacitor and the ED output capacitance limit the baseband bandwidth to 300 Hz.

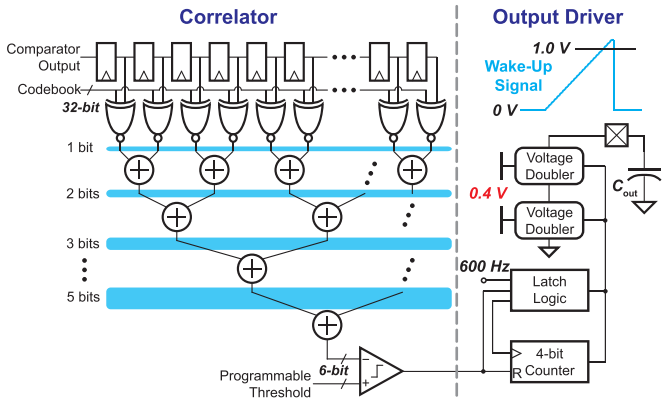

Fig. 10. Digital correlator baseband logic with wake-up signal output driver.

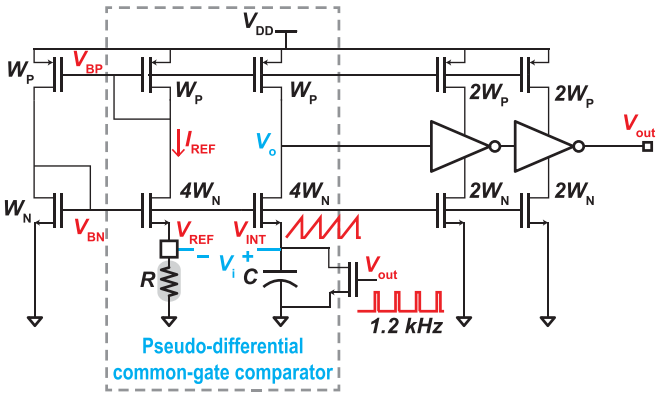

Fig. 12. Schematic of the relaxation oscillator.

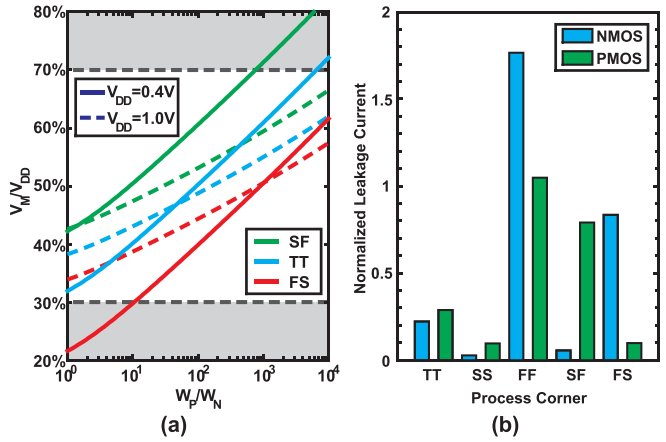

Fig. 11. (a) Simulated switching threshold for an inverter with minimum width and length across different corners and supply voltages. (b) Simulated normalized leakage current of the designed inverter across corners.

An early reset feedback was implemented to generate a two phase non-overlapping clock efficiently and save comparator dynamic power simultaneously. As illustrated in Fig. 9, the comparator resets once the comparator output is latched, such that the dynamic power of the integrator is reduced from $2fC_FV_{DD}^2$ to $2fC_FV_{threshold}^2$. Since a large capacitance C_F is added, the power savings are significant. Simulation shows that 33% of total comparator power is saved when the WuRX RF input power is −69 dBm, or 0.7 mV at the comparator input. The early reset feedback was implemented as shown in Fig. 9(c), where an SR-latch captures the rising edge of either V_{outb+} or V_{outb-} and asserts CLK to "low" to turn off the integration. The non-overlapping phases are generated with two inverter chains: one creates a pos-edge delay and the other creates a neg-edge delay. The pos-edge delay was created by four cascaded inverters, where the first was designed to be a high-skewed inverter followed by a low-skewed inverter with W_P/W_N of 6 and 0.5, respectively. Similarly, the neg-edge delay was created by flipping the order of the skewed inverters. Compared with a conventional two-phase clock generator where cascaded latches are used, this method has lower power consumption with a 0.4-V supply.

D. Digital Baseband

Fig. 10 shows the digital baseband correlation logic that processes the incoming data from the comparator. With the lack of a power hungry PLL for synchronization, the correlator provides an energy efficient way to overcome phase asynchronization by operating at a 2× oversampling rate to sample the incoming bits [20]. An optimal 16-bit code sequence (1110101101100010) was designed such that it has both a large Hamming distance from all of its shifted versions ($D = 9$) and from the all-0 sequence ($D = 9$). A family of codes also exists, but with slightly lower Hamming distances ($D \leq 8$). As the input sequence shifts along the D flip-flop chain, the correlator computes the Hamming distance between the sequence and the programmable 32-bit oversampled code book. Once the value is below a preset threshold, the pattern is declared detected and the correlator generates a wake-up signal. To drive the main receiver with a higher supply voltage, the output driver was designed to generate a >1-V signal with 5 ms duration assuming a 10-pF load. When the correlator sends a wake-up signal to the driver, it resets a 4-bit counter and the signal is latched to leave the cascode voltage doubler enabled until the counter rolls over. The charge pump and counter make the wake-up signal look like a ramp. Also, to use the same 0.4-V supply, the digital baseband operates in the sub-V_t region implemented with a custom designed logic gate library using thick oxide devices. All the gates were designed using only inverters and transmission gates for the highest robustness in subthreshold [21].

From a static performance perspective, digital logic gates operating in the sub-V_t region need extra attention to the transistor sizing to overcome process variation. To see this, the inverting threshold V_M of an inverter with minimum width and length NMOS was simulated across the width of the PMOS at different process corners [Fig. 11(a)], where the solid and dashed lines correspond to a 0.4- and 1.0-V supply voltage, respectively. For an ideal inverter with a negligible transition region, the noise margin is equal to the lower value of either V_M or $V_{DD} - V_M$. It can be seen that the inverter maintains larger than 30% V_{DD} noise margin when operating above-V_t across all corners, while it fails when operating in the sub-V_t region without proper sizing. Another important design

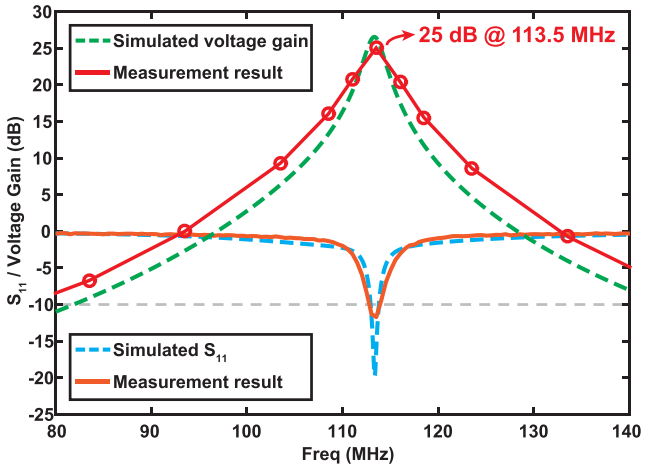

Fig. 13. Simulated and measured transformer S_{11} and voltage gain.

consideration comes from the power dissipation. For a digital circuit, it is well known that the power consumption can be written as

$$P_{\text{tot}} = P_{\text{leak}} + P_{\text{dyn}} = V_{\text{DD}} I_{\text{leak}} + \alpha C_{\text{L}} V_{\text{DD}}^2 f \qquad (12)$$

where I_{leak} is the average leakage current, α is the activity factor, C_{L} is the load capacitor, and f is the clock rate.

In addition to the low clock rate, since ideally the correlator only computes when the signal pattern changes, α is nearly zero, both of which make the leakage power dominant and thus the design target here. To equate the NMOS and PMOS leakages in this process where the PMOS has lower mobility and V_{t} is 90 mV higher than an NMOS in the typical-typical (TT) corner, 5× NMOS devices were stacked. Moreover, the PMOS was re-sized to 1.6× larger width to achieve 30% V_{DD} noise margin even in the worst case fast-slow (FS) corner. Fig. 11(b) shows the leakage current of the designed inverter across corners, which is normalized to the leakage current of a minimum size inverter at TT. The normalized I_{leak} is 0.26 in the TT corner and 1.41 in the fast-fast (FF) corner.

E. Relaxation Oscillator

The system clock for the comparator, digital baseband, and charge pump is generated from a relaxation oscillator. As shown in Fig. 12, the oscillator is composed of a reference generator, where one branch is shared with a pseudo-differential common-gate comparator, an inverter chain, and a reset switch. The reference generator with all four transistors operating in the sub-V_{t} region, generates a reference current I_{REF} and a reference voltage V_{REF} through an off-chip resistor. I_{REF} is used to charge a MIM capacitor that is connected to a common-gate comparator (shown in the dashed box). The comparator output is pulled high after V_{INT} exceeds V_{REF}. Then, the inverter chain is triggered to close the reset switch and reset the integration capacitor. The capacitor is charged and discharged periodically with a period of $\sim RC$. The clock buffer was implemented with current-starved inverters whose delay are determined by I_{REF}, which has better

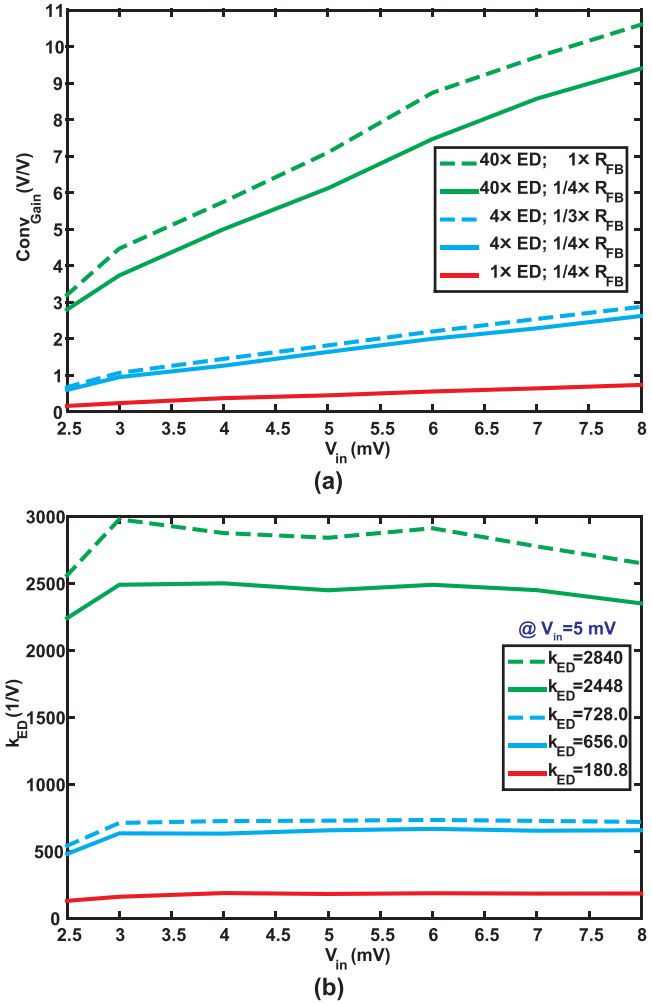

Fig. 14. Measurement results. (a) ED conversion gain. (b) Scaling factor k_{ED}.

energy efficiency than dynamic inverters (CV_{DD}^2). Since the power consumption is largely determined by the static power of the reference generator and comparator, the oscillator power consumption can be minimized by using a large bias resistor. The resistor was chosen to be 30 MΩ and I_{REF} to be ∼0.5 nA. To compensate the variation of the capacitor value and comparator delay, the off-chip resistor is tuned to adjust the oscillation frequency to 1.2 kHz. The oscillator output is divided and buffered to a 600-Hz system clock with 50% duty cycle. The frequency varies from 617 to 585 Hz, when the supply voltage changes from 0.35 to 0.45 V. This corresponds to 5.3% frequency change when the supply changes by 25%. When the temperature changes by 10 °C, the frequency changes by 4.9%. The supply and temperature sensitivity are mainly caused by the comparator and buffer delay. The 2× oversampling scheme and short data sequence (53.3 ms) make the system insensitive to clock mismatch. Based on system-level Monte Carlo simulations where the clock mismatch is modeled as normal distribution with 1.5% standard deviation (i.e., 99.7% samples are within ±4.5% clock mismatch), the sensitivity deviation is less than 0.5 dB.

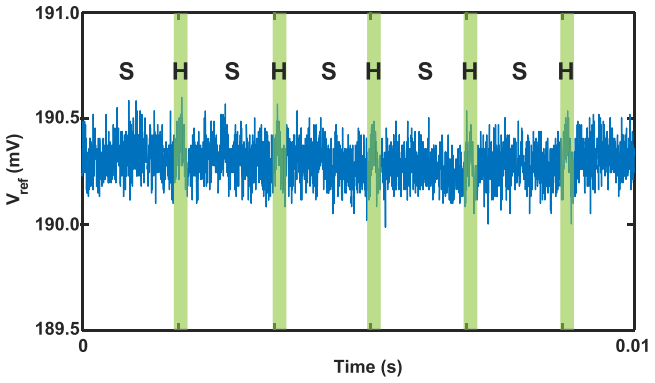

Fig. 15. Measured reference ladder output voltage with sample and hold phases annotated.

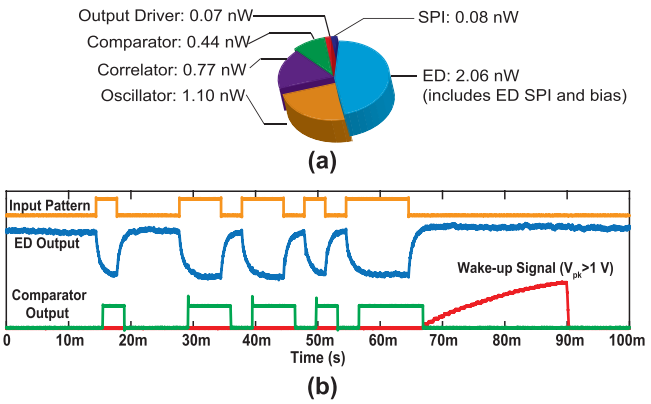

Fig. 16. (a) System power breakdown pie chart. (b) Transient waveforms at each node.

IV. Measurement Results

To characterize the passive voltage gain from the transformer/filter, a conventional two-port measurement such as S_{21} using a vector network analyzer (VNA) is not possible due to the high (i.e., non-50 Ω) output impedance. Instead, we first characterized the ED by connecting a 50-Ω load at the input without the transformer to provide matching and measured the output voltage after applying a known input signal. We then replaced the 50-Ω resistor with the transformer and again measured the output voltage. The transformer gain was then calculated using

$$A_V = \frac{V_{in,1}}{V_{in,2}} \cdot \sqrt{\frac{V_{out-ED,2}}{V_{out-ED,1}}}. \tag{13}$$

Using the above-mentioned procedure, $A_V = 25$ dB was measured, which is in agreement with simulation results (Fig. 13). S_{11} measurements show excellent matching at the signal frequency (113.5 MHz), and is also in agreement with simulations.

The measured conversion gain, $\text{Conv}_{\text{Gain}}$, and scaling factor, k_{ED}, versus $V_{in-ED,1}$ for different ED bias current settings are shown in Fig. 14. While the $\text{Conv}_{\text{Gain}}$ is proportional to $V_{in-ED,1}$ as shown in Fig. 14(a), Fig. 14(b) shows that k_{ED} is independent of $V_{in-ED,1}$, which is expected from (8) and (9). When the ED is configured for 2 nW (i.e., 1× ED) with four parallel feedback units (i.e., 1/4× $R_{FB,unit}$) to achieve a 300-Hz low-pass corner, $k_{ED} = 180.8$ (1/V). Using 1/3× $R_{FB,unit}$ and 4× ED, the ED achieves $k_{ED} = 728$ (1/V), which is ∼ 4× larger than the 1× ED configuration, as expected. At higher powers (e.g., 40× ED), r_o dominates, and thus the improvement in k_{ED} saturates.

The comparator noise was measured by sweeping the input differential voltage and fitting the resulting distribution. Since the comparator noise is mostly white, fitting with a Gaussian distribution allows the noise and offset to be extracted. Nine chips were measured with the input-referred noise varying from 89 to 95 μV_{RMS}, slightly lower than the simulated value at the TT corner, likely due to process variation. The measured offset varied from 0.69 to 1.16 mV, which is easily covered by the 5-bit tuning range of the comparator CDAC.

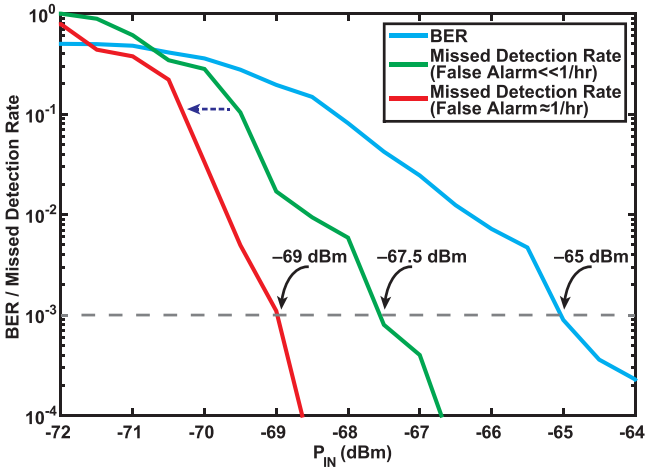

Fig. 17. BER and MDR waterfall curves with a 300-bps data rate.

The performance of the kickback reduction technique was validated by measuring the output voltage of the reference ladder, which connects to one of the comparator inputs, with the transmitted signal at the other input. Since this is a very high impedance node (∼2 GΩ||50 pF), a unity-gain buffer with low input bias current was used to buffer the voltage. The measured data are shown in Fig. 15, where the sample (S) and hold (H) phases are annotated. Only small spikes appear during the H phase that are due to the leakage of the sampling switch since the switch OFF-resistance is not significantly larger than the reference ladder impedance. The spikes always settle before the beginning of the next cycle owing to the zero net charge kickback, and as such do not affect the following comparisons.

Fig. 16(a) shows the measured power breakdown of the WuRX. The total power consumption is 4.5 nW when the ED is set to 2.0 nW. Transient waveforms shown in Fig. 16(b) demonstrate correct detection when the correct code is transmitted.

Fig. 17 shows the waterfall curves for conventional bit error rate (BER) measured at the comparator output, and the wake-up signal missed detection rate (MDR) measured after the digital baseband (BB) logic. The BER was measured

TABLE I
COMPARISON WITH PREVIOUSLY PUBLISHED STATE-OF-THE-ART WURXS

	[4] JSSC'09	[22] ISSCC'10	[3] ISSCC'11	[7] CICC'13	[6] JSSC'16	[9] ISSCC'16		**This Work**
Technology	90 nm	90 nm	130 nm	130 nm	65 nm	65 nm		**180 nm**
Carrier Frequency	2 GHz	915 MHz	402 MHz	403 MHz	2.4 GHz	2.4 GHz		**113.5 MHz**
Modulation	OOK	OOK	FSK	OOK	OOK	OOK		**OOK**
Supply Voltage	0.5 V	1 V	1 V	1.2/0.5 V	0.5 V	1/0.5 V		**0.4 V**
Digital Correlator	No	No	No	31-bit	No	31-bit		**32-bit**[1]
External Components	BAW filter	L for MN + LNA loading	XTAL + LC MN	XTAL + LC MN	BGA SMD L	XTAL + MN		**Transformer/filter**
Oscillator	Ring osc.	No	Inj-locked osc.	XTAL osc.	LC DCO	XTAL osc.		**Relaxation osc.**
Gain Stage(s)	IF[2]	RF/BB[2]	IF[2]	ED[2]	IF/BB[2]	ED[2]	ED/BB[2]	**TF/ED/BB**
Interferer Rejection	BAW filter	LC MN + LNA loading	LC MN + IF filter	LC MN + correlator	LC MN + N-path filters	Digital processor		**Transformer/filter + correlator**
SIR (dB) @ $\lvert\Delta f\rvert$	> -5 @ 10 MHz[3]	N/A	N/A	+3.3 N/A	$-31/-27$ @ 5 MHz[3]	N/A		**-15 @ 5 MHz**[4]
Data Rate	100 kbps	10 kbps	200 kbps	12.5 kbps	10 kbps	8.192 kbps		**0.3 kbps**
Energy/bit	520 pJ	5100 pJ	220 pJ	9.3 pJ	9900 pJ	12.7 pJ	28.8 pJ	**15.0 pJ**
Sensitivity	-72 dBm	-80 dBm	-70 dBm	-45.5 dBm	-97 dBm	-39 dBm	-56.5 dBm	**-69 dBm**[5]
Normalized Sensitivity[6]	-97 dB	-100 dB	-123 dB	-66 dB	-137 dB	-58.6 dB	-76.1 dB	**-81.4 dB**
Power	52 μW	51 μW	44 μW	116 nW	99 μW	104 nW	236 nW	**4.5 nW**

[1] 16-bit code sequence with 2 $\times$ oversampling. [2] The front-end matching network also has modest passive gain.
[3] Measured using CW jammer with signal input power for BER= 10^{-3} + 3 dB.
[4] Measured using CW jammer with signal input power for BER= 10^{-3} + 1 dB.
[5] Defined with less than 10^{-3} missed detection rate.
[6] Calculated by normalizing the sensitivity to data rate using either (16) or (17) depending on demodulation method.

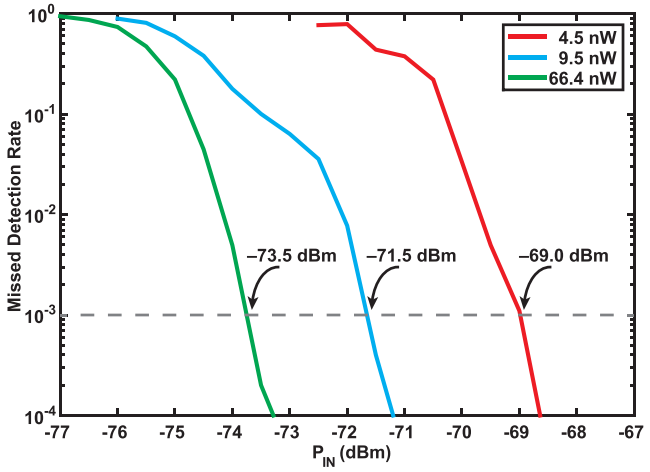

Fig. 18. MDR waterfall curves for different power settings with a 300-bps data rate.

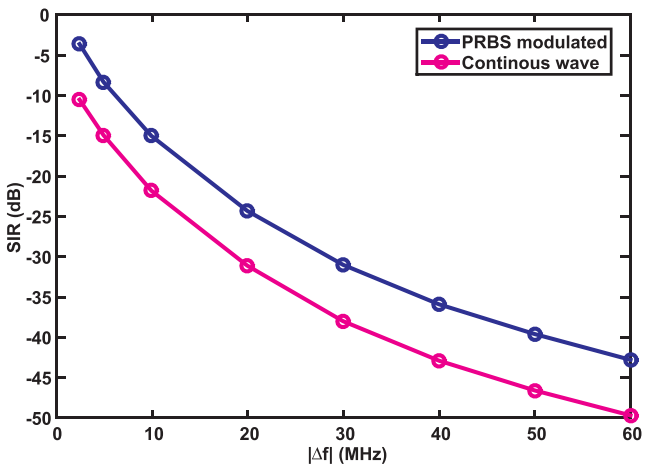

Fig. 19. SIR curve versus interferer frequency offset $|\Delta f|$ to carrier frequency for a worst case 300-bps PRBS-modulated jammer and a CW jammer.

under the assumption of perfect synchronization between clock and input data, while the MDR was measured with random (i.e., not synchronized) transmission. To achieve a BER = 10^{-3}, the input signal power $P_{\text{IN}} = -65$ dBm. With the same comparator and correlator threshold, $P_{\text{IN}} = -67.5$ dBm for MDR = 10^{-3} with a false alarm rate of $\ll$ 1/hr. By adjusting the comparator threshold, $P_{\text{IN}} = -69$ dBm was achieved for MDR = 10^{-3} with a false alarm rate of $\approx$ 1/hr, which is where the sensitivity P_{SEN} is defined, and 4-dB coding gain is shown compared to the BER measurement. MDR measurements were also taken at higher power ED settings (Fig. 18). For the 4$\times$ ED case, $P_{\text{SEN}} = -71.5$ dBm and the power consumption is 9.5 nW. For the 40$\times$ ED case, $P_{\text{SEN}} = -73.5$ dBm and the power consumption is 66.4 nW.

A modulated signal tone along with a pseudorandom binary sequence (PRBS) modulated or continuous wave (CW) jam-

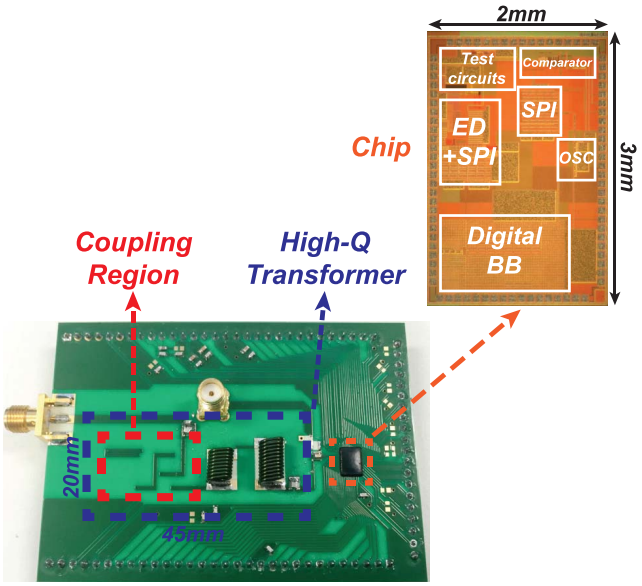

Fig. 20. Top: picture of annotated die micrograph. Bottom: whole WuRX.

mer at frequency offset Δf to the signal center frequency were used to test WuRX performance under interference. The input signal power was set to 1 dB higher than the power where BER $= 10^{-3}$ (i.e., at −64 dBm), and the interferer power at Δf was swept until BER $= 10^{-3}$. The signal-to-interferer ratio (SIR) versus $|\Delta f|$ is depicted in Fig. 19. Because of the high-Q nature of the transformer/filter, for PRBS jammer a SIR < -30 dB was achieved at $|\Delta f| = 30$ MHz. At the chosen FM band, since a narrowband FM signal would look like a CW jammer and only causes a dc tone at the ED output, an additional 7 dB rejection compared to a PRBS jammer was achieved. Moreover, a CW jammer is unlikely to cause a false alarm due to the correlator. Therefore, by designing a longer bit correlator, the code space can be increased, which not only improves interferer resilience further in terms of false alarms, but also enables more WuRXs with different wake-up codes in the sensor network. The die micrograph along with the whole system photograph is shown in Fig. 20.

V. Figure of Merit and Comparison

As discussed in Section I, for WuRXs used in low-average throughput applications, power consumption and sensitivity are the most important metrics, and thus the following FoM is defined:

$$\mathrm{FoM_{LAT}}(dB) = -P_{\mathrm{SEN}} - 10\log\frac{P_{\mathrm{dc}}}{1\ \mathrm{mW}} \tag{14}$$

where P_{SEN} is the sensitivity in dBm and P_{dc} is the power consumption. For high-average throughput applications, data rate is important. Therefore, the following FoM is used:

$$\mathrm{FoM_{HAT}}(dB) = -P_{\mathrm{SEN,norm}} - 10\log\frac{P_{\mathrm{dc}}}{1\ \mathrm{mW}} \tag{15}$$

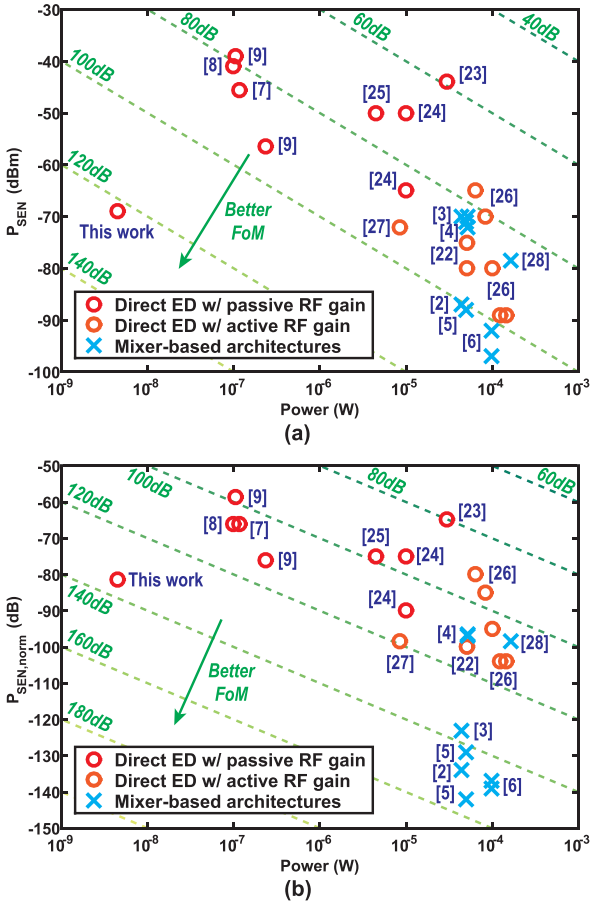

Fig. 21. (a) Sensitivity versus power ($\mathrm{FoM_{LAT}}$). (b) Sensitivity normalized to data rate versus power ($\mathrm{FoM_{HAT}}$).

where $P_{\mathrm{SEN,norm}}$ is the sensitivity normalized to data rate and calculated using one of the following equations:

$$P_{\mathrm{SEN,norm}}(dB) = P_{\mathrm{SEN}} - 5\log BW_{\mathrm{BB}} \tag{16}$$

$$P_{\mathrm{SEN,norm}}(dB) = P_{\mathrm{SEN}} - 10\log BW_{\mathrm{BB}} \tag{17}$$

where $5\log BW_{\mathrm{BB}}$ in (16) is used for designs with a non-linear squaring function for envelope detection [4], [7]–[10], [12], [22]–[28], and $10\log BW_{\mathrm{BB}}$ in (17) is used for designs with a linear operation to demodulate the signal [3], [6] or designs using a non-linear squaring function for envelope detection after high active pre-ED gain with sharp filtering [2], [5] (i.e., where convolution noise dominates [12]). A survey of prior-art WuRXs is shown in Fig. 21 for both FoMs. The low baseband bandwidth and high passive RF gain afforded by the high input impedance ED and FM-band high-Q passives enabled the proposed design to achieve an $\mathrm{FoM_{LAT}} = 122.5$ dB, which is over an order of magnitude higher than prior work. For high-average throughput applications where data rate is important, while this design achieved the best $\mathrm{FoM_{HAT}} = 134.9$ dB among the direct ED architectures, mixer-based architectures achieved comparable, and in some cases better, $\mathrm{FoM_{HAT}}$ at the expense of four decades higher power consumption. Table I summarizes the measurement results of the proposed WuRX and compares the results to the state-of-the-art WuRXs.

VI. Conclusion

In this paper, a 0.4-V 113.5-MHz OOK-modulated WuRX that achieves −69-dBm sensitivity consuming only 4.5 nW in a 0.18-μm SOI CMOS process is presented. The WuRX was designed for emerging event-driven low-average throughput applications to reduce system power. While conventional direct envelope detection architectures can achieve low power at moderate sensitivities, this design breaks the conventional tradeoff to achieve ultralow power with high sensitivity by: 1) reducing the baseband signal bandwidth to 300 Hz; 2) modulating OOK signal with a custom 16-bit code sequence to get 4-dB coding gain; 3) employing an off-chip high-Q transformer/filter with 25-dB passive voltage gain enabled by an ED with high input impedance; 4) achieving higher conversion gain using an active-L-biased ED; 5) digitizing the ED output via a regenerative comparator with kickback elimination; and 6) decoding the received OOK signal using a high-V_t subthreshold digital baseband correlator, operating with 2× oversampling to overcome phase asynchronization, where the clock is generated by a 1.1-nW relaxation oscillator.

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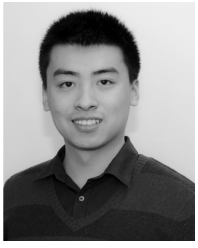

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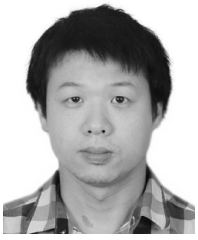

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