A Hybrid Semi-Digital Transimpedance Amplifier With Noise Cancellation Technique for Nanopore-Based DNA Sequencing

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***Abstract*—Over the past two decades, nanopores have been a promising technology for next generation deoxyribonucleic acid (DNA) sequencing. Here, we present a hybrid semi-digital transimpedance amplifier (HSD-TIA) to sense the minute current signatures introduced by single-stranded DNA (ssDNA) translocating through a nanopore, while discharging the baseline current using a semi-digital feedback loop. The amplifier achieves fast settling by adaptively tuning a DC compensation current when a step input is detected. A noise cancellation technique reduces the total input-referred current noise caused by the parasitic input capacitance. Measurement results show the performance of the amplifier with 31.6 MΩ mid-band gain, 950 kHz bandwidth, and 8.5 fA/$\sqrt{\text{Hz}}$ input-referred current noise, a 2× noise reduction due to the noise cancellation technique. The settling response is demonstrated by observing the insertion of a protein nanopore in a lipid bilayer. Using the nanopore, the HSD-TIA was able to measure ssDNA translocation events.**

***Index Terms*—DNA sequencing, nanopore, noise cancellation technique, semi-digital feedback loop, transimpedance amplifier.**

I. Introduction

NANOPORE-BASED DNA sequencing has been under active development since 1995 [1]–[10]. It is a biophysical technique to sequence DNA based on the physical properties of the four types of nucleotides - guanine (G), adenine (A), thymine (T), and cytosine (C) - the building blocks of DNA. A nanopore is a small orifice, usually only a few nanometers in diameter, sandwiched between two fluidic chambers, the *cis* and *trans*, as shown in Fig. 1(a). When the nanopore is immersed in an ionic buffer with a bias voltage V_{b} applied between the two chambers, a baseline current I_{baseline} is generated from the ions that drift through it. As DNA, being negatively charged, translocates through the pore, a current blockade occurs due to the different size and charge distribution of the nucleotides inside of the nanopore. One can, in theory, reconstruct the nucleotide sequence of single-stranded DNA (ss-DNA) by observing the characteristic amplitude changes. Compared to conventional sequencing methods [1], nanopore-based methods are more efficient using only electrical and physical features of DNA without the need for complicated optical detection steps or custom nucleotides.

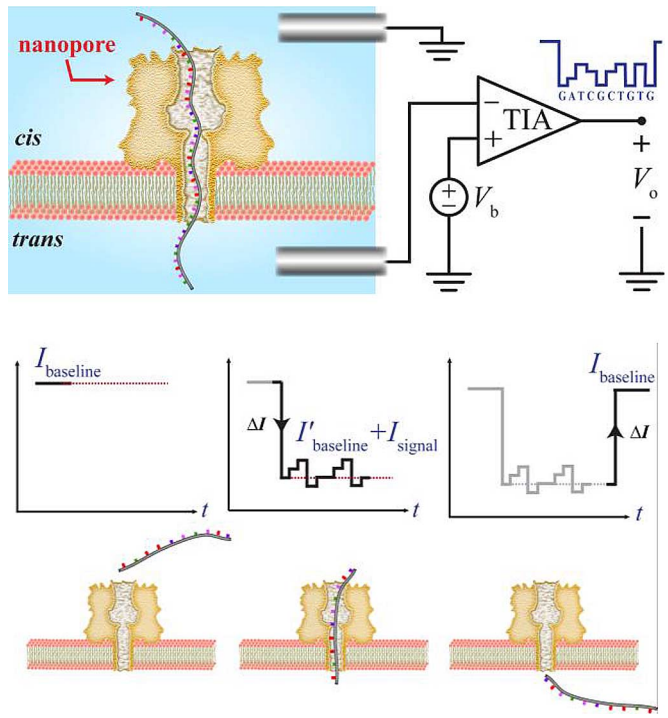

Fig. 1. (a) Illustration of a nanopore-based DNA sequencing platform. (b) The baseline current shift that occurs when a ssDNA translocates.

Two main techniques are used to create nanopores: solid-state fabrication [4]–[6] and biological proteins (porin) [7]–[10]. Solid-state nanopores utilize semiconductor manufacturing techniques, whereas a porin is a natural protein in the shape of a tube inserted in a lipid bilayer. Controlling the spatial and temporal resolution of nanopores is an active area of research, where researchers are investigating methods to control the translocation speed and engineering thin, narrow pores to reduce the interrogation region [5]. Both types of pores require instrumentation to measure the small current differences between nucleotides, often less than 10 pA, in the presence of the baseline ionic current, which can be more than 1 000× larger [5]. Uncontrolled, the speed of ssDNA translocating through a

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nanopore can be faster than one nucleotide per microsecond. Thus, the requirements of the current-sensing circuits for nanopores are quite demanding: high gain (>10 MΩ), high bandwidth (>10 kHz), low noise (<10 $\mathrm{pA_{RMS}}$), and wide dynamic range.

Another more application specific challenge in nanopore-based DNA sequencing is the abrupt change in baseline current that occurs when a protein nanopore inserts or leaves a lipid bilayer [11]. Considering the protein nanopore lifetime, the time period when a pore is inserted into a lipid bilayer, can be as short as several seconds at room temperature [12], it is essential to minimize the settling time of the amplifier. This requirement for low settling time also applies when ss-DNA enters or leaves the pore impeding the flow of ions, reducing the baseline current by 30–90% [5], as shown in Fig. 1(b). This change in I_{baseline} is inversely proportional to the size of the pore. In our setup, using a protein nanopore with a diameter of 1.4 nm, the baseline current is reduced by 83–95% in the presence of ssDNA. Therefore, the step response of the current-sensing circuit must be minimized to prevent missing any current signatures during the settling of the circuit [11].

A transimpedance amplifier (TIA) functions as a current-sensing circuit to convert the current input into a voltage output for further processing and analysis [13], [14]. Resistive and capacitive TIAs are widely used in many commercial instruments, such as the Axopatch 200B [15]. However, these topologies have notable drawbacks in this application. Namely, they either have large input-referred noise and low bandwidth, as is the case for a resistive feedback TIA [13], [14], or must be constantly reset since I_{baseline} can saturate the amplifier in a capacitive feedback TIA [16], [17]. This large I_{baseline} also increases the dynamic range requirement of the TIA [4]. A TIA with a DC feedback loop is one method to achieve low noise and high bandwidth [18], [19] without the need for a reset network; however, the limited bandwidth of the feedback loop requires a long settling time for a step-input current, such as when a pore is inserted into the lipid bilayer [11].

As the bandwidth is increased, the sensitivity of a TIA is limited by the quadratic growth of the total integrated input-referred current noise [13], [14]. Neglecting noise from the feedback resistor, the TIA in Fig. 2 has two noise sources: a current noise i_{n} and a voltage noise e_{n} from the OPAMP. The input-referred current noise density is

$$\overline{i_{\mathrm{n,tot}}^2}(\omega) = \overline{i_{\mathrm{n}}^2} + \overline{e_{\mathrm{n}}^2}\omega^2 C_{\mathrm{in}}^2 \tag{1}$$

where C_{in} is the total capacitance at the input node of the TIA. At low frequencies, since the input-referred current noise density is approximately equal to the current noise i_{n} and the noise from e_{n} can typically be ignored. However, the second term in (1) produced by e_{n} and C_{in} dominates when the bandwidth increases beyond the noise corner frequency f_{c}, which is often only several kilohertz because C_{in} is predominantly caused by the capacitance of the nanopore [4]. Depending on how the pore is realized, it may not be possible to reduce this capacitance.

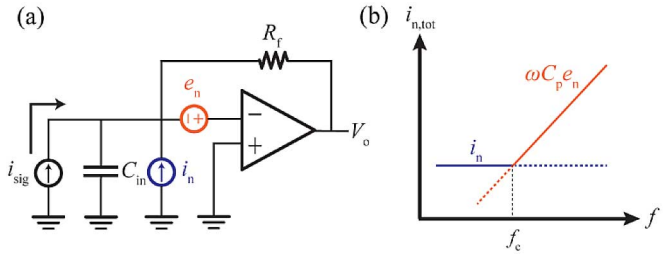

Fig. 2. (a) Conventional resistive feedback TIA with voltage and current noise model. (b) The corresponding power spectrum density (PSD) of the input-referred current noise. The high frequency noise of the TIA is dominated by the input capacitor C_{in} and the voltage noise e_{n}.

Hence, the input-referred current noise must be reduced by either using circuit techniques or actively cooling the system [14] when the bandwidth is greater than 10 kHz.

In this paper, we describe a hybrid semi-digital TIA (HSD-TIA) with high flat-gain bandwidth and very low noise. The HSD-TIA continuously measures the input current without a reset switch by discharging the baseline current through a semi-digital feedback loop. In addition to servoing out the DC and low frequency baseline currents, this loop also adaptively provides a DC compensation current for fast step response. A noise cancellation technique is shown to reduce the input-referred current by partially cancelling the second term of (1).

The rest of this paper is organized as follows. The architecture of the proposed HSD-TIA with the noise cancellation technique is introduced in Section II. In Section III, the semi-digital feedback loop with fast step response is explained. The noise cancellation technique and noise performance of the TIA are analyzed in Section IV. Section V focuses on the implementation of the proposed TIA, and measurement results are presented in Section VI. Using the designed TIA, the biological measurements are shown in Section VII. Finally, conclusions are drawn in Section VIII.

II. Architecture of the HSD-TIA

We describe a HSD-TIA with a noise cancellation technique to obtain low noise, fast settling time, and continuous operation for nanopore-based DNA sequencing as shown in Fig. 3. The HSD-TIA contains three paths: 1) the signal path to amplify the input current at mid-band, 2) the semi-digital feedback loop to discharge the low-frequency components, including the baseline current and flicker noise $(1/f)$, and 3) the feed-forward noise cancellation path to remove the voltage noise from the integrator. The signal path of the TIA consists of a capacitive feedback integrator that is cascaded with a differentiator to obtain high flat-gain bandwidth. The high cutoff bandwidth, f_{H}, is obtained by cancelling a DC pole from the integrator with a DC zero from the differentiator. The mid-band gain is

$$A_{\mathrm{mid}} = R_{\mathrm{f}} \times C_2/C_1 \tag{2}$$

where C_1 is the feedback capacitor in the integrator, and C_2 and R_{f} form the differentiator. The transfer function of the HSD-TIA is shown in Fig. 3(b).

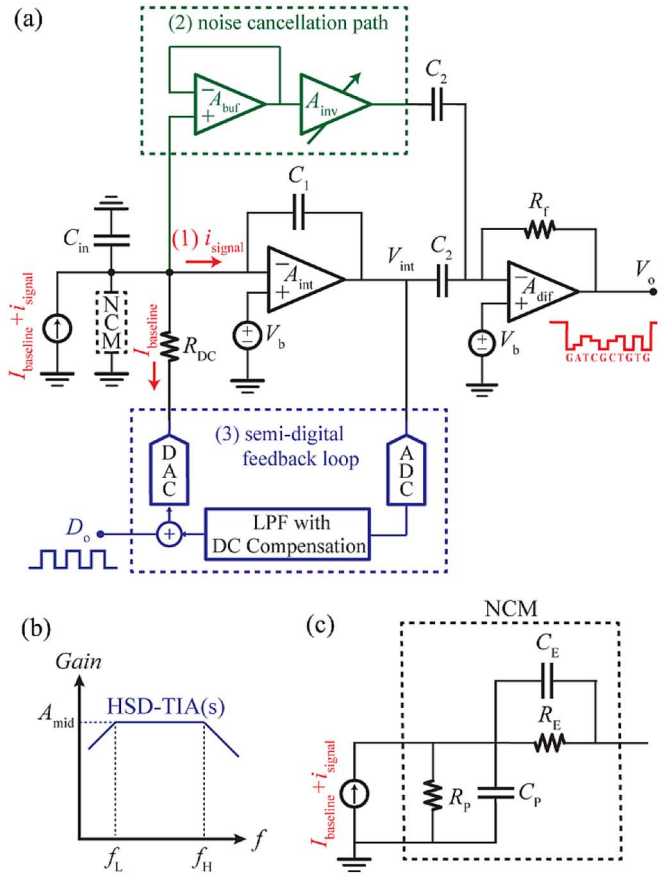

Fig. 3. (a) Architecture of the HSD-TIA with noise cancellation technique. (b) Frequency response of the HSD-TIA with low cutoff frequency f_{L} introduced by the semi-digital feedback loop and high cutoff frequency f_{H}. (c) Equivalent nanopore circuit model. R_{p} and C_{P} are the nanopore resistance and capacitance, and R_{E} and C_{E} model from the Ag/AgCl electrodes.

The semi-digital feedback path is wrapped around the integrator to discharge the low frequency components, particularly the baseline current and $1/f$ noise. The feedback loop introduces poles and zeros to shape the low-frequency response [18], [19]. The lower cutoff frequency f_{L} needs to be as low as a few tens of Hz to prevent loss of signal for nanopores with low DNA translocation speed, such as engineered MspA [8], [9] and motor controlled pores [10]. The frequency of these poles and zeros must be carefully designed to avoid attenuating the signal at mid-band and to maintain stability of the amplifier. Here, the poles and zeros are implemented with a digital low-pass filter (LPF) in the feedback path. Compared to an analog implementation using discrete components with large resistances and capacitances that can have large variation [18], [19], the frequency of the poles and zeros can be precisely controlled in the digital domain.

Another advantage of this approach is the direct accessibility of the digitized low-frequency component, which is filtered out in an analog implementation that contains relevant biological information, such as the size of the nanopore and the number of nanopores inserted in a lipid bilayer. Compared to an analog feedback loop, an additional ADC, DAC, and FPGA are needed to implement the filter. However, the feedback signal may be digitized anyway, so we are merely pushing the ADC inside the feedback loop. Also, the low-frequency nature of this loop does not necessitate high performance data converters.

The settling behavior of the HSD-TIA is determined by the bandwidth of the feedback loop, i.e., the low cutoff frequency, f_{L}. When a step-input current occurs, the baseline current accumulates on the integrator capacitor during the settling of the feedback loop. This step-input current can be as large as 95% of I_{baseline} [5], which can easily saturate the output of the integrator since the feedback loop discharges the accumulated current slower than the integrator saturation rate, resulting in loss of the input signal during settling. We address this by using an adaptive DC compensation current in the feedback loop to improve the settling behavior. A digital circuit in the FPGA detects the occurrence and magnitude of the input step by tracking the integrator output and checking if it exceeds a predefined window. The feedback loop then adaptively produces a DC compensation current by adding a digital code D_{o} with the opposite sign of the step to the output of the filter. This compensation current reduces the difference between the feedback current and baseline current without having to wait for the LPF to settle and prevents saturation of the integrator resulting in a significant reduction of the settling time.

The noise of a high bandwidth TIA is dominated by C_{in} and $\overline{e_{\mathrm{n}}^2}$ at high frequencies (2) where C_{in} is dominated by the capacitance of nanopore [4], [20], the input capacitance of the OPAMP, and cable parasitic capacitances. C_{in} is often 10 pF, even when co-integrating the nanopore and TIA [4]. Thus, there is a fundamental limit to how much C_{in} can be reduced necessitating alternative methods to reduce the noise. Here, we propose a noise cancellation technique to reduce the input-referred current noise by sensing and subtracting the voltage noise e_{n}. This feed-forward noise cancellation path contains a voltage-sensing amplifier and an inverting amplifier with matched gain, such that the noise from the signal and noise cancellation paths add destructively. As shown in Fig. 3, the condition to cancel this voltage noise is

$$e_{\mathrm{n}} \times (C_1 + C_{\mathrm{in}})/C_1 = e_{\mathrm{n}} \times |A_{\mathrm{inv}}| \tag{3}$$

Thus, the voltage noise e_{n} from the integrator is cancelled by summing the inversely duplicated version of the same voltage noise from the noise cancellation path. Note that no input signal is amplified by the noise cancellation path [21], [22] because the input voltage of the HSD-TIA is clamped by the virtual ground. The equivalent nanopore circuit model (NCM) [13], [14], [23], shown in Fig. 3(c), is considered when analyzing the stability and noise performance of the TIA.

In summary, the semi-digital feedback loop performs several functions: 1) it discharges the baseline current preventing saturation of the integrator and allowing continuous operation without the need for the reset network that is common in a capacitive TIA [16], [17], 2) it provides precise control of the low-frequency response and 3) it improves the settling response through an adaptive current. The TIA noise performance is improved by feed-forward cancellation of the integrator voltage noise and the removal of the $1/f$ noise in the feedback loop.

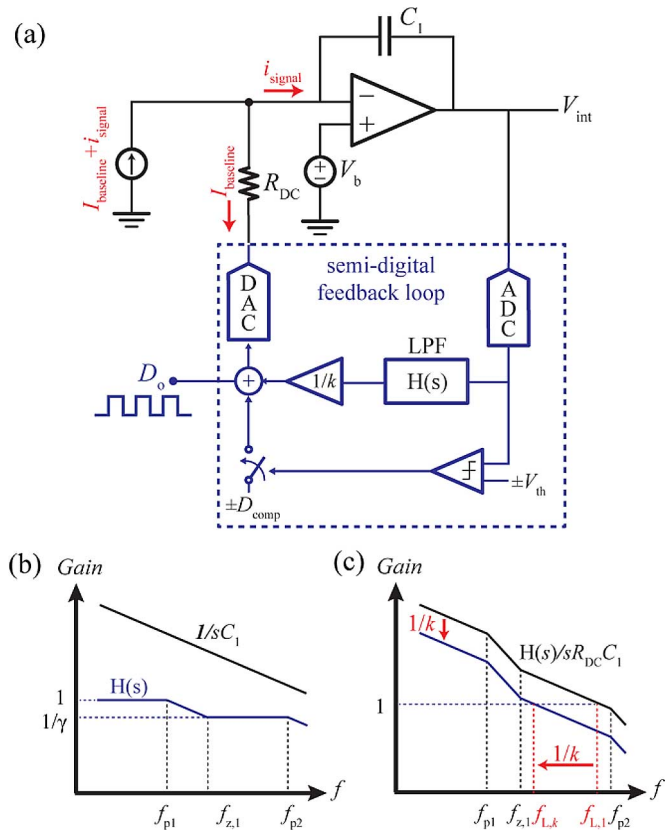

Fig. 4. (a) Concept of the semi-digital feedback loop. (b) Frequency response of integrator and LPF. (c) Frequency response of the loop gain with the tuning factor $1/k$ to adjust the low cutoff frequency f_{L} and the stability of the feedback loop.

Collectively, these relax the requirements of the integrator, particularly the voltage noise level and input capacitance size.

III. Semi-Digital Feedback Loop

The semi-digital feedback loop consists of two main components: a digital filter and a DC compensation block, as shown in Fig. 4(a). The circuits are implemented digitally in order to guarantee the stability of the feedback loop without attenuating the desired signal. The frequency response of the feedback path, shown in Fig. 4(b) and (c), can be controlled efficiently, precisely, and adaptively in the digital domain.

A. Digital Filter

The semi-digital feedback path is composed of an ADC, a LPF, and a DAC. The LPF removes the high frequency signals from the output of the integrator and feeds the resulting signal back to the input of HSD-TIA. Thus, the baseline current is discharged through a resistor R_{DC} by the feedback loop. The ideal loop gain of this feedback path (Fig. 4) can be derived as

$$G(s) = -\frac{H(s)}{sR_{\mathrm{DC}}C_1} \tag{4}$$

where $H(\mathrm{s})$ is the transfer function of the digital LPF. Without loss of generality, $H(\mathrm{s})$ is assumed to have a pole f_{p1}, one or more high frequency poles f_{p2}, a zero f_{z1}, a passband gain of unity, and an attenuation ratio of γ in the stopband. The low cutoff frequency f_{L} of the HSD-TIA can be derived from unity gain frequency of this loop, i.e., $|G(2\pi f_{\mathrm{L}})| = 1$

$$f_{\mathrm{L}} = \frac{1}{2\pi\gamma R_{\mathrm{DC}}C_1}. \tag{5}$$

Considering the stability of a feedback loop, the additional poles introduced by the digital filter reduce the closed loop phase margin [18], [19]. A positive tuning factor k is added in the digital domain to control the frequency response of the feedback loop and set the low cutoff frequency f_{L}. Changing the value of k shifts the magnitude response and the unity gain frequency f_{L} without changing the phase response, thus allowing one to tune the frequency of f_{L} dynamically while guaranteeing the phase margin of the feedback loop. We define $f_{\mathrm{L},k}$ as the unity gain frequency with a tuning factor of $1/k$. When $1/k$ is less than 1, the magnitude response shifts down, and $f_{\mathrm{L}k}$ decreases by k with respect to $f_{\mathrm{L},1}$; that is

$$f_{\mathrm{L},k} = \frac{1}{2\pi k\gamma R_{\mathrm{DC}}C_1}. \tag{6}$$

By carefully choosing k and the -3 dB frequency of the LPF, it is possible to maintain a phase margin of the low-frequency feedback loop greater than 45°. Hence, the stability of the feedback loop is obtained by tuning k even with variation of R_{DC} and C_1. A DC gain larger than unity in $H(\mathrm{s})$ could also be implemented to improve the stability; however, a higher order filter is required resulting in longer settling time.

The LPF is implemented in the digital domain with a sampling frequency of f_{s}. With a fixed f_{s} and f_{L}, one can save power and area in the LPF using a lower order LPF with a large f_{p1} and small $1/k$. However, the static gain error at the output of the integrator depends on the feedback factor. That is

$$\Delta V_{\mathrm{int}} = \Delta I_{\mathrm{baseline}} R_{\mathrm{DC}}/k \tag{7}$$

where ΔV_{int} is the static gain error. The static gain error shifts the output common-mode voltage and limits the output swing of the integrator, so the value of k must be chosen carefully. For example, a 100 pA input-step current with R_{DC} of 1 G Ω and $1/k$ of 0.1 causes a static gain error of 1 V. This large static gain error can saturate the integrator especially with a low power supply voltage. The DC compensation current described later mitigates this problem and allows one to reduce the area and power of this digital LPF by using a lower order filter.

B. DC Compensation Current

A DC compensation current is added to reduce the settling time and prevent the integrator from saturating when a step-input current occurs. In order to implement this, a digital comparator monitors the digitized integrator output. Once the integrator output exceeds a predefined voltage range, a DC compensation code D_{comp} is added to the output of the LPF. The output

voltage of the integrator with the DC compensation current can be written as

$$D_{\mathrm{o,norm}}(t) = D_{\mathrm{comp,norm}} + (1 - D_{\mathrm{comp,norm}})(1 - e^{-t/\tau}) \tag{8}$$

where $D_{\mathrm{o,norm}}$ and $D_{\mathrm{comp,norm}}$ are the respective digital codes of the feedback loop and DC compensation normalized to the amplitude of the step-input current, τ is the closed-loop time constant, and $V(D)$ is the corresponding analog voltage of the digital code D. The feedback loop estimates the size of the step-input current by measuring the static gain error of the feedback loop from (7), and a digital code D_{comp} is calibrated based on this static gain error. The gain error is readily obtained in the digital domain because this gain error appears at the output of the integrator and is digitized by the ADC. The algorithm is as follows: initially, D_{comp} is set to zero; once a step current is detected, the amplitude is measured. Then, a new digital code D_{comp} is updated and used for all later measurements since the size of the step-input current is roughly constant throughout the experiment. Using this technique, the settling time is reduced from 5τ to 2τ, a 60% reduction in settling time with a settling error of 0.7% when D_{comp} is 95% of the step.

The other benefit of the DC compensation current is the reduction in the static gain error due to the tuning factor in (7). When the D_{comp} is used, most of the discharging current is provided by D_{comp} rather than the feedback loop. The loop gain error can be reduced to

$$\Delta V_{\mathrm{int}} = |\Delta I_{\mathrm{baseline}} R_{\mathrm{DC}} - V(D_{\mathrm{comp}})|/k. \tag{9}$$

Hence, the DC compensation current can both decrease the static gain error of the integrator and reduce the settling time.

IV. Noise Cancellation Technique and Noise Analysis

A. Noise Cancellation Technique

The proposed noise cancellation technique requires a low-noise voltage buffer to sense the voltage noise from integrator, and an amplifier to provide the matched gain between the noise cancellation path and the integrator [21], [22], as shown in Fig. 5. Due to the virtual ground at the input of the integrator, the voltage noise of the integrator can be sensed by a unity gain buffer. This sensed voltage noise is then amplified by a tunable inverting amplifier. From (3), the value of R_{c1} and R_{c2} are tuned to obtain the optimized noise cancellation effect with respect to the total input capacitance.

B. Noise Analysis

To analyze the total input-referred current noise density of the HSD-TIA in the signal band, we first neglect the noise cancellation path. The equivalent input noise is given by

$$\overline{i^2_{n,\mathrm{tot}}}(\omega) = \overline{i^2_{n1}} + \overline{e^2_{n1}}\omega^2(C_1 + C_{\mathrm{p}})^2 + \frac{\overline{e^2_{n1}}}{R^2_{\mathrm{DC}}} + \frac{4kT}{R_{\mathrm{DC}}} + \frac{\overline{e^2_{\mathrm{Q}}}}{k^2\gamma^2 R^2_{\mathrm{DC}}}$$

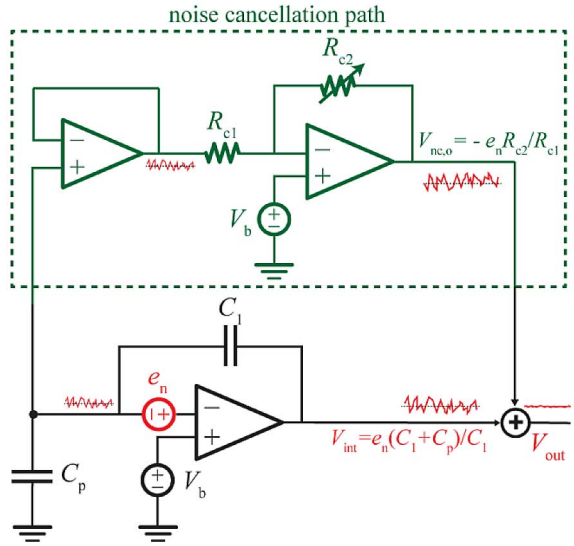

Fig. 5. Schematic of feedforward noise cancellation circuit. The integrator voltage noise is sensed and amplified by the noise cancellation path.

$$+ \left(\frac{C_1}{C_2}\right)^2 \left(\overline{i^2_{n2}} + \overline{e^2_{n2}}\omega^2 C_2^2 + \frac{\overline{e^2_{n2}}}{R^2_{\mathrm{f}}} + \frac{4kT}{R_{\mathrm{f}}}\right) \tag{10}$$

where $\overline{i^2_{n1}}$,$\overline{e^2_{n1}}$, $\overline{i^2_{n2}}$, and $\overline{e^2_{n2}}$, are the current and voltage noises of the OPAMPs in the integrator and differentiator, respectively; C_{in} is the total capacitance at the input of the HSD-TIA, including the input node of integrator, the connection between the TIA, and the capacitance of the lipid bilayer; and $\overline{e^2_Q}$ is the noise from the digital circuits, including the quantization error of the ADC and digital LPF. For simplicity, the integrated digital noise $\overline{e^2_{Q,\mathrm{rms}}}$, is taken to be only the ADC quantization noise, $V^2_{\mathrm{LSB}}/12$ over the bandwidth of the feedback loop which is attenuated by the tuning factor k. The ratio of $\mathrm{C_2/C_1}$, which forms part of the gain of the TIA, is much greater than unity by design, so the input-referred noise of the TIA is approximately

$$\overline{i^2_{n,\mathrm{tot}}}(\omega) \simeq \overline{i^2_{n1}} + \overline{e^2_{n1}}\omega^2 (C_1 + C_{\mathrm{in}})^2 + \frac{4kT}{R_{\mathrm{DC}}} + \frac{\overline{e^2_{\mathrm{Q}}}}{k^2\gamma^2 R^2_{\mathrm{DC}}} + \left(\frac{C_1}{C_2}\right)^2 \frac{4kT}{R_f}. \tag{11}$$

Note that the input-referred current noise of the TIA, like the resistive feedback TIA, is dominated by the second term in (11) at frequencies higher than f_{c}.

Next, we analyze the input-referred current noise with the noise cancellation technique using similar steps

$$\begin{aligned}\overline{i^2_{n,\mathrm{tot}}}(\omega) \simeq{}& \left(\overline{i^2_{n1}} + \overline{i^2_{nc1}}\right) + \alpha^2\overline{e^2_{n1}}\omega^2(C_1 + C'_{\mathrm{in}})^2 \\ &+ \left(\overline{i^2_{nc2}} \cdot R^2_{c1}||R^2_{c2} + 4kTR_{\mathrm{c1}}\frac{R^2_{\mathrm{c2}}}{R^2_{\mathrm{c1}}} + 4kTR_{\mathrm{c2}}\right)\omega^2 C_1^2 \\ &+ \overline{e^2_{nc1}}\omega^2 (C_1 + C_{\mathrm{in}})^2 + \frac{4kT}{R_{\mathrm{DC}}} + \frac{\overline{e^2_{\mathrm{Q}}}}{k^2\gamma^2 R^2_{\mathrm{DC}}} \\ &+ \left(\frac{C_1}{C_2}\right)^2 \frac{4kT}{R_f}.\end{aligned} \tag{12}$$

where $\overline{i_{\rm nc1}^2}$,$\overline{e_{\rm nc1}^2}$, $\overline{i_{\rm nc2}^2}$, and $\overline{e_{\rm nc2}^2}$ are the current and voltage noises of the OPAMPs in the voltage buffer and the inverting amplifier and $C_{\rm in}^{'}$ is the total input capacitance at the input of the HSD-TIA after adding the noise cancellation path. We define α as the residual noise factor after the noise cancellation

$$\alpha = \left| 1 - \frac{(R_{\rm c2}/R_{\rm c1})}{(C_{\rm i}+C_{\rm in}^{'})/C_{\rm i}} \right|. \tag{13}$$

The noise at frequencies higher than $f_{\rm c}$ is reduced significantly, by a factor of α, with the trade-off of slightly increased noise at low frequencies due to the additional term $\overline{i_{\rm nc1}^2}$. The noise from the inverting amplifier can be neglected because $R_{\rm c1}$, $R_{\rm c2}$, and $\overline{e_{\rm nc2}^2}$ can be designed with smaller values compared to $\overline{e_{\rm n1}^2}$, since no signal is processed in the noise cancellation path. Thus, the TIA input-referred current noise can be approximated as

$$\begin{aligned}\overline{i_{n,\rm tot}^2}(\omega) \simeq & \left(\overline{i_{n1}^2}+\overline{i_{nc1}^2}\right)+\alpha^2\overline{e_{n1}^2}\omega^2(C_1+C_{\rm in}^{'})^2 \\ & + \overline{e_{\rm nc1}^2}\omega^2(C_1+C_{\rm in}^{'})^2+\frac{4kT}{R_{\rm DC}}+\frac{\overline{e_{\rm Q}^2}}{k^2\gamma^2R_{\rm DC}^2}+\left(\frac{C_1}{C_2}\right)^2\frac{4kT}{R_f}.\end{aligned} \tag{14}$$

From (14), the performance of the noise cancellation is limited: by 1) the residual noise factor α and 2) the voltage noise $\overline{e_{nc1}^2}$ from the buffer. The residual noise factor is optimized by tuning the gain of the inverting amplifier to match the signal path. The unity gain buffer can be designed or chosen with lower voltage noise $\overline{e_{\rm nc1}^2}$ than $\overline{e_{\rm n1}^2}$ because the requirement of this buffer is relaxed with a feedback factor of unity, which is much larger than the integrator. Hence, the total integrated noise of the HSD-TIA with the noise cancellation in (14) is reduced compared to (11).

V. Implementation

We verified the proposed HSD-TIA with the noise cancellation technique using discrete components on a PCB (Fig. 6). This design has a mid-band gain of 31.6 MΩ and a flat-gain bandwidth of 950 kHz. The component values for the design are listed in Table I. A 5 V LDO is used to provide a stable power supply voltage, and a low-noise reference voltage generator for the common mode and bias voltage are also implemented on the PCB. A 6th order Bessel LPF with a gain of 10 dB is cascaded with the HSD-TIA as an anti-aliasing filter. The gain of the HSD-TIA was designed based on (2). The differentiator is implemented as a band-pass filter to set the high cutoff frequency $f_{\rm H}$ and improve the stability of the TIA. $f_{\rm H}$ can be easily adjusted for different types of nanopores by simply tuning the feedback capacitor in the band-pass filter without an increase in the input-referred noise or decrease in the gain. Currently, $f_{\rm H}$ is limited by the parasitic capacitance on the PCB in the feedback path of the differentiator rather than by the OPAMPs when the bandwidth is increased.

In order to obtain low noise and low leakage current, the integrator OPAMP requires a voltage noise less than 10 nV/$\sqrt{\rm Hz}$, a current noise less than 10 fA/$\sqrt{\rm Hz}$, and an input capacitance of only a few pF. A MOS-input OPAMP with low input bias current is used for the integrator. The total input bias current of the HSD-TIA is designed to be less than 10 pA to minimize signal leakage. The requirements of low voltage noise and low input capacitance are relaxed because of the noise cancellation path. The noise requirement of the differentiator OPAMP is reduced also because of the gain from the integrator.

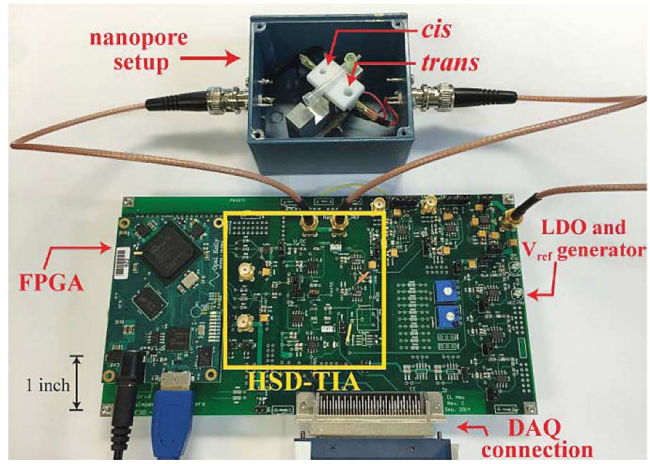

Fig. 6. Photograph of nanopore and TIA.

TABLE I
List of Discrete Components and Values

Active Device		Part Name	Passive Component	Part Name
OPAMP	$A_{\rm int}$	AD8033	$R_{\rm DC}$	1 GΩ
	$A_{\rm dif}$	AD8065	$R_{\rm f}$	200 kΩ
	$A_{\rm buf}$	LTC6240	C_1	2.2 pF
	$A_{\rm inv}$	LTC6200	C_2	110 pF
ADC		AD7276	FPGA	Opal Kelly XEM6300
DAC		AD5320		

The semi-digital feedback loop was realized with a 12-bit ADC, FPGA, 12-bit DAC, and a resistor $R_{\rm DC}$. The FPGA implemented the LPF, DC compensation logic, and all control logic. The LPF was designed based on the values of $f_{\rm L}$ and k in (6), (8) and (9). The LPF is implemented as an equal-ripple finite impulse response (FIR) filter with a -3 dB frequency of 100 Hz and a gain factor $1/k$ of 0.1 which results in an $f_{\rm L}$ of 26 Hz. The -3 dB frequency could be lower with a larger value of k, but the area/power overhead is increased due to a higher order filter. $R_{\rm DC}$ was chosen according to the discharging current capability and the current noise $4k{\rm T}/R_{\rm DC}$. Furthermore, $R_{\rm DC}$ should be on the same order of magnitude as the resistance of nanopore channel, so the baseline current caused by the bias voltage $V_{\rm b}$ can be discharged by $R_{\rm DC}$. Here, an $R_{\rm DC}$ of 1 GΩ provides a maximum baseline discharging capability of 2 nA with $V_{\rm o,peak}$ of 2 V and a low input-referred noise based on (14).

The noise requirements of the noise cancellation path are higher than the signal path to reduce the total noise of the TIA. The OPAMP in the unity-gain buffer has the same requirements as the integrator, except with a lower input capacitance and

lower voltage noise. However, the feedback factor of this OPAMP is unity, which is much larger than the feedback factor of the integrator, so the open-loop bandwidth requirement of the buffer is reduced. We chose an OPAMP with a voltage noise $\overline{e_{\mathrm{nc1}}^2}$ lower than $\overline{e_{\mathrm{n1}}^2}$. Next, the voltage noise requirement of inverting amplifier should also be lower than the integrator to minimize the noise overhead. We used a BJT-input OPAMP with lower voltage noise because the input bias current is provided by the buffer. The voltage noise from the resistors in the inverting amplifier are also optimized, thus minimizing the noise contribution from the noise cancellation path. The differentiator in the signal path is used to subtract the amplified signal V_{int} from the sensed noise $V_{\mathrm{nc,o}}$, as shown in Fig. 5. We use OPAMPs with closed-loop bandwidth higher than 1 MHz in the noise cancellation path to prevent phase mismatch between the signal path and noise cancellation path at high frequency. The offset voltage from OPAMPs in the noise cancellation is removed by the differentiator. Due to limited selection of commercially available OPAMPS, it may be possible to find a single OPAMP that outperforms the proposed solution in the noise cancellation path. However, a CMOS implementation allows the designer greater flexibility in the amplifier design and benefits from the decoupling of the requirements from the noise cancellation path.

VI. Circuit Performance

We characterized the performance of the designed HSD-TIA with the NCM at the input. The TIA operates with a single supply voltage of 5 V and a common-mode voltage of 2 V. All measurements were analyzed using a National Instruments data acquisition system (DAQ) with 16-bit resolution.

A. Frequency Response

The frequency response was measured by sweeping the frequency of a sinusoidal input current connected to the NCM. The measurement results in Fig. 7 show the frequency response of the design. The measured flat-band gain is 31.6 MΩ over a 26 Hz–950 kHz bandwidth. The measurement results correspond well with the theoretical analysis.

B. Noise Performance

The measured noise power spectral density is shown in Fig. 8 with zero input current applied. First, we measured the input-referred current noise without the noise cancellation path; i.e., disconnecting both the input of the unity gain buffer and the output of the inverting amplifier from the integrator. The TIA had a measured spot noise of 8.5 fA/$\sqrt{\mathrm{Hz}}$ at 1 kHz. The corner frequency f_{c} was 1.5 kHz, and the noise increased at higher frequencies due to the parasitic capacitor C_{p} and the voltage noise of the integrator. The total integrated input-referred current noise was 6.9 $\mathrm{pA_{rms}}$ for a bandwidth of 10 kHz without the noise cancellation technique.

Next, we tested the noise of the TIA with the noise cancellation path. The corner frequency $f_{\mathrm{c,NC}}$ of the TIA was 3 kHz, which is 2× higher compared to the original TIA without the noise cancellation. The total integrated input-referred current noise of the designed TIA was 3.4 $\mathrm{pA_{rms}}$ and 13.5 $\mathrm{pA_{rms}}$ for a bandwidth of 10 kHz and 100 kHz, which is a 2× improvement, with the noise cancellation technique. We also calculated the total integrated input-referred current noise of 1.8 $\mathrm{nA_{rms}}$ for a bandwidth of 950 kHz by extrapolating the noise power spectrum. The proposed design shows a ∼ 2.2× reduction in the input-referred current noise compared to the Axopatch 200B [4], [15], and this could be further reduced to 2.9 $\mathrm{pA_{RMS}}$ with the same active cooling system at −15° C . Note that the noise at low frequency is caused by an output offset voltage of 10 μV, which has a negligible contribution on the integrated input-referred current noise over the designed bandwidth.

Table II lists this work and recent works on TIAs for nanopores. One key feature of our design is the higher dynamic range afforded by discharging baseline current and the addition of a noise cancellation technique. The bandwidth of the described design and the total integrated input-referred noise is

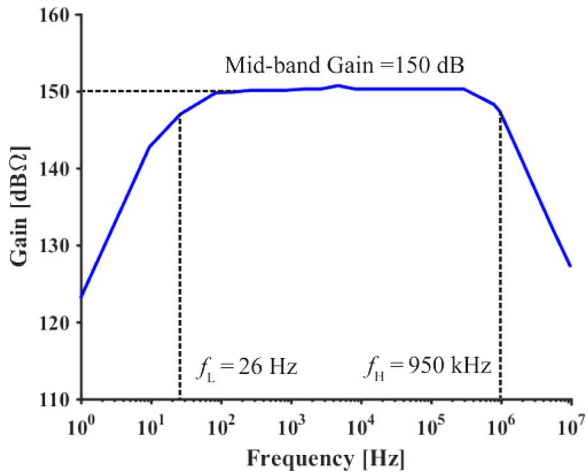

Fig. 7. Frequency response of reported HSD-TIA.

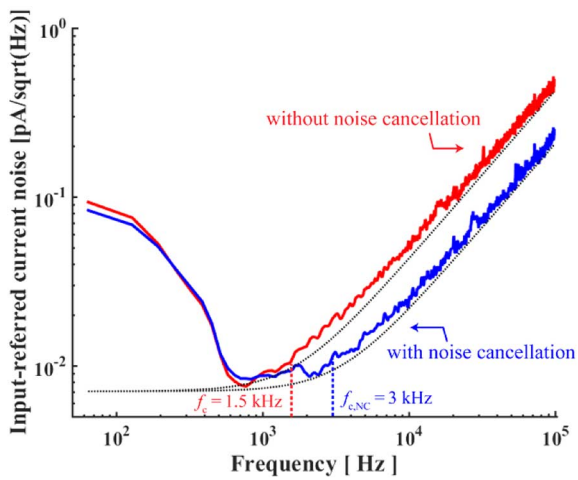

Fig. 8. Measured input-referred noise spectrum of reported HSD-TIA with and without noise cancellation circuit. The dotted lines are theoretical noise spectrums with and without noise cancellation path calculated from (14) and (11) respectively.

TABLE II
PERFORMANCE COMPARISON

SPEC	[4]	[18]	[19]	[23]	This Work
Gain (MΩ)	100	20	20	250	31.6
Bandwidth (kHz)	1,000	1,400	4,000	10	950
Input-Referred Noise (fA/√Hz)	10	8	3	42.1	8.5
Settling Time (s)	N/A	> 10	N/A	N/A	0.04
Supply (V)	± 1.5	± 10	+ 1.5	± 1.5	+5
Power (mW)	45	640	N/A	0.52	65*
Implementation	CMOS	Discrete IC	CMOS	CMOS	Discrete IC

* The power consumption of FPGA is not included.

currently limited by the parasitic capacitance on the PCB, and could be further improved with CMOS integration.

VII. Biological Measurement Results

We verified the performance of the reported TIA by measuring nanopore insertions into a lipid bilayer. We used wild type α-Hemolysin (α-HL), a natural protein, to form the nanopore in a lipid bilayer composed of 1,2-dipalmitoyl-sn-glycero-3-phosphocholine (DPhPC) from Avanti.

A. Creating Lipid Bilayer

The lipid bilayer was formed using the painting method [7] with a clean pipette tip on 25 μm diameter PEEK tubing in a buffer consisting of 0.3 M KCl and 10 mM HEPES. Ag/AgCl electrodes were used to bias the *cis* and *trans* chambers and to sense the current. The bias voltage was set to 180 mV, which was determined by the salt concentration of the buffer. The entire setup was placed inside of a Farady cage to minimize environmental interference, such as 60 Hz power line noise.

To verify the formation of the lipid bilayer rather than just a clogged tube, a saw-tooth waveform is typically applied at the *cis* chamber with a conventional resistive feedback TIA [24]. The principle of this test method is that the impedance of the lipid bilayer is mainly capacitive, with a unit area capacitance C_{u} of $\sim 1-2$ μF/mm^2 [20]. The output waveform will be a square wave when the TIA works as an R-C differentiator with the capacitance of the lipid bilayer at the input of the designed TIA. However, in our design the low-frequency component of the saw-tooth waveform is discharged by the feedback path.

Instead of a saw-tooth waveform, we verify the existence of a bilayer by applying a single-tone sinusoidal wave to the lipid bilayer. The output voltage of the HSD-TIA with a capacitor at the input is equal to

$$V_{\mathrm{o}}(s) = \frac{C_1}{C_u \cdot A_{\mathrm{bilayer}}} s R_{\mathrm{f}} C_2 \tag{15}$$

where A_{bilayer} is the area of a lipid bilayer. We apply a sine wave with a frequency of 10 kHz and peak-to-peak amplitude of 10 mV to guarantee the stability of the lipid bilayer, i.e., the lipid bilayer will not break with the 10 mV voltage variation across these two chambers. The output waveform of the HSD-TIA is shown in Fig. 9. The peak-to-peak output voltage of the HSD-TIA is 45 mV, which equates to a capacitor of 3.2 pF in series with the input of the designed TIA. This capacitance corresponds well with the theoretical value.

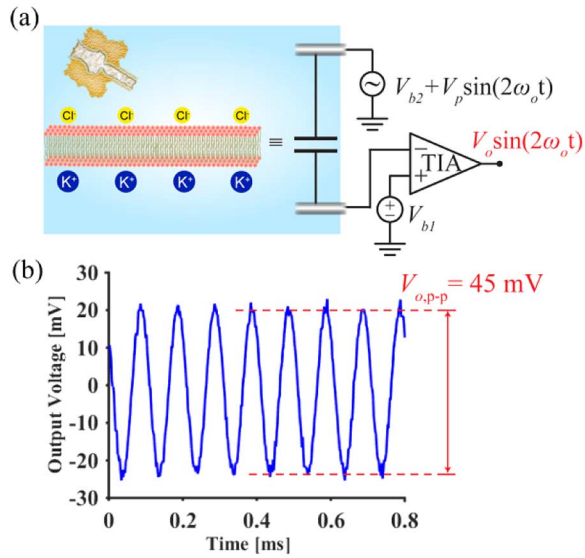

Fig. 9. (a) Equivalent test circuit with the HSD-TIA for verifying the existance of a lipid bilayer. (b) Measured output waveform of the HSDTIA with a single-tone sine-wave input.

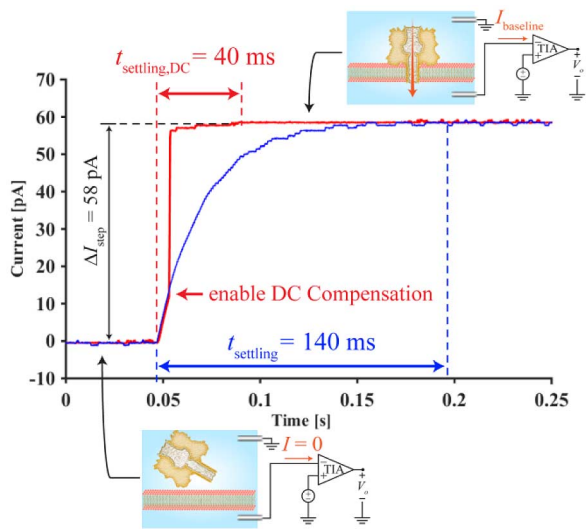

Fig. 10. Comparison of the step responses of the reported TIA with and without the DC compensation current when a protein nanopore is inserted into the lipid bilayer.

B. Measurement of Nanopore Insertion

We verified the fast step response by measuring the settling time of the feedback loop when a nanopore is inserted into a lipid bilayer. A nanopore, α-HL, was prepared in the same buffer with a surfactant and added to the *cis* chamber. Initially, no current channel forms when only the lipid bilayer exists, so the feedback current, I_{baseline}, in the feedback path was zero. An ion channel formed when α-HL spontaneously was inserted into the lipid bilayer. A baseline current step, $\Delta I_{\mathrm{baseine}}$, of 58 pA was measured when a single nanopore was inserted into the lipid bilayer. Fig. 10 shows the settling of the feedback current over time. The settling time of the designed HSD-TIA was 140

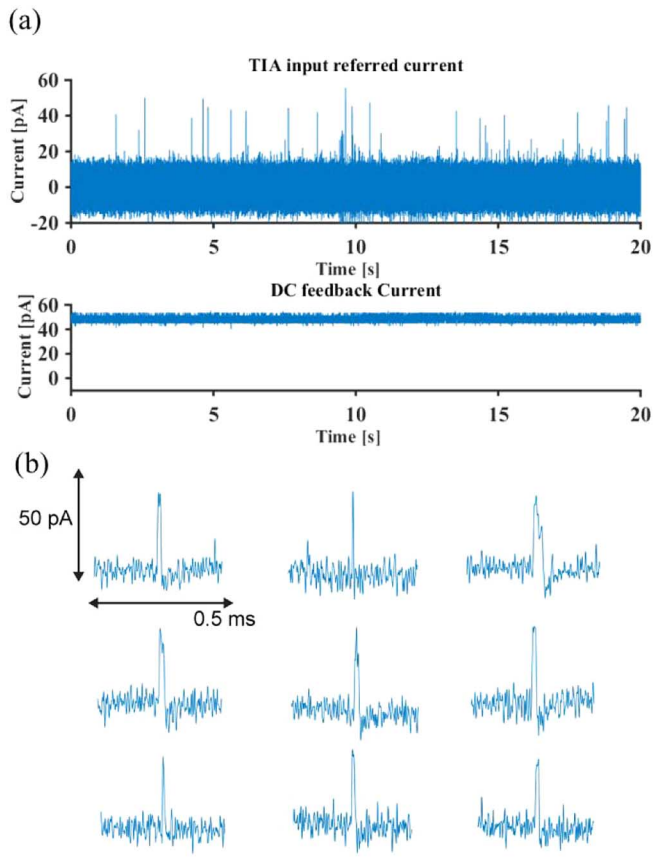

Fig. 11. (a) Measurement of 200 base ssDNA translocation events in the signal path and DC feedback path. (b) Zoomed in view of spikes with an average translocation time of 0.1 msec and amplitude of 30–50 pA.

milliseconds without the DC compensation current. After the calibration of DC compensation code D_{comp}, the settling time was reduced to 40 ms, a $3.5\times$ improvement. Furthermore, the integrator did not saturate during the settling period because of this DC compensation current. In contrast, the settling time of an analog feedback TIA [18] was longer than several seconds and the output was saturated with the same step-input current [11].

C. Measurement of DNA Translocation

We observed ssDNA (200 nucleotides) translocation events by adding 0.1 nM of ssDNA to the *cis* chamber after a nanopore was inserted into the lipid bilayer. The baseline current was $\sim$50 pA measured by the low frequency code D_{o} with a bias voltage of 150 mV. The output of the HSD-TIA captured the current changes caused by the translocation of ssDNA while the baseline current remained unchanged. As shown in the Fig. 11, the ssDNA caused a current change of 30–50 pA with an average translocation time of 0.1 ms. The amplitude and translocation time of the measured data agree well with the results in [2], [3], and demonstrate the feasibility of the proposed HSD-TIA for nanopore-based DNA sequencing.

VIII. Conclusion

In this paper we identified the key requirements for nanopore-based DNA sequencing approaches. We reported a hybrid semi-digital TIA with a noise cancellation technique to achieve the necessary high flat-gain, high-bandwidth, low input-referred noise, and fast step response. The baseline current from ionic diffusion is discharged through a semi-digital feedback loop that improves the dynamic range. The sensitivity of the TIA was increased with the reduction of the input-referred current noise using a noise cancellation technique. Fast settling was obtained with a DC compensation current in this feedback loop. ssDNA translocation data demonstrate the feasibility of the HSD-TIA for the nanopore-based DNA sequencing. In the future, we will investigate increasing the bandwidth and decreasing the high frequency noise by implementing the proposed concept in a CMOS process and co-integrating the amplifier with the nanopore.

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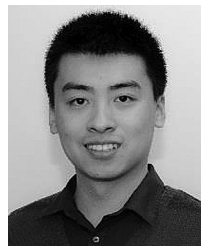

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