A Dynamically Reconfigurable ECG Analog Front-End With a $2.5 \times$ Data-Dependent Power Reduction

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Abstract—This paper presents a reconfigurable electrocardiogram (ECG) analog front-end (AFE) exploiting bio-signals' inherent low activity and quasi-periodicity to reduce power consumption. This is realized by an agile, on-the-fly dynamic noise-power trade-off performed over specific cardiac cycle regions guided by a least mean squares (LMS)-based adaptive predictor leading to ~2.5× data-dependent power savings. Implemented in 65 nm CMOS, the AFE has tunable performance exhibiting an inputreferred noise ranging from 2.38 – 3.64 $\mu V_{\rm rms}$ while consuming 307 – 769 nW from a 0.8 V supply. A comprehensive system performance verification was performed using ECG records from standard databases to establish the feasibility of the proposed predictor-based approach for power savings without compromising the system's anomaly detection capability or ability to extract pristine ECG features.

Index Terms—Activity-based power, ECG, reconfigurable AFE.

I. INTRODUCTION

D EMAND for portable health and wellness products has dramatically increased as individuals have become more engaged and proactive in their healthcare. For example, many of today's smartphones and wearables (*e.g.*, smartwatches, rings, and patches) incorporate health-centric sensors that have tremendous potential for early detection and real-time monitoring of health disorders in the comfort of one's daily routine. However, the small form factor and need for continuous biosignal acquisition, like the electrocardiogram (ECG), imposes stringent power budgets. Energy-efficient designs are hence critical for long-lasting operation.

From a low-power perspective, an analog front-end (AFE) comprising a low-noise amplifier and an analog-to-digital converter (ADC) followed by local feature extraction (*e.g.*, using either analog [1] or digital [2] circuitry) to reduce/remove the

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Fig. 1. (a) Proposed digitally-assisted adaptive bio-signal acquisition system architecture. (b) Example of a reconfiguration strategy for an ECG signal.

power-hungry RF transmission is widely accepted as the stateof-the-art architecture for ECG acquisition today. However, the AFE power consumption is fixed at design time and primarily driven by the noise requirement in such a system. The power of such AFEs can vary from the μ W range for diagnostic quality ECG recording [3] to a few nW for low-accuracy sensors [4], [41], thus exhibiting a power/accuracy trade-off. The inclusion of tunable parameters (*e.g.*, gain/bandwidth in the amplifier [5]– [7] and sampling rate/resolution in the ADC [8], [9]) partially address this trade-off; however, these systems cannot dynamically trade power consumption for performance, as is demonstrated in this work.

Notably, many bio-signals, including ECG, exhibit lowactivity and quasi-periodicity properties that provide a unique opportunity to tackle the power/accuracy trade-off by alternate means. This is facilitated by the signal path shown in Fig. 1(a), wherein the AFE is dynamically reconfigured through feedback from a digital signal processor (DSP). A new technique to reduce the AFE power in a data-dependent fashion is demonstrated by digitally assisting this reconfigurable AFE on the fly and thereby adaptively adjusting the signal fidelity, as illustrated in Fig. 1(b). As in most systems, the amplifier is the most power consumptive block and is guided by an adaptive filter based on a least mean squares (LMS) algorithm for dynamic reconfiguration. This work extends the work initially presented in [10].

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The rest of the paper is organized as follows: Section II reviews prior work and motivates the proposed technique. Section III provides an overview of the system architecture. Section IV describes the AFE circuit implementation followed by the DSP in Section V. Finally, measurement results are presented in Section VI, and Section VII concludes this work.

II. LIMITATIONS OF PRIOR WORK AND MOTIVATION

The concept of leveraging inherent signal properties is not new and has been incorporated in several prior works [11]–[20]. Notably, data-dependent power reduction has emerged as a popular approach in recent successive approximation register (SAR) ADCs by bypassing conversion cycles within predefined windows [11], [12], using the previous conversion result as the starting point for subsequent conversions [13], [14], resolving only the difference between consecutive samples [15], using an ECG-specific tracking algorithm [49], and other similar techniques [49–53]. Specifically, [12]–[14] demonstrated $1.5 \times$, $2.7\times$, and $2.6\times$ reductions in the ADC power, respectively, for digitizing an ECG signal. However, as elaborated upon later, the ADC has a negligible contribution to an ECG AFE's power. RF transmission has also benefited from this concept using derivative-based adaptive sampling [5], level-crossing sampling [16], adaptive resolution digitization [17], and sparsity-based data-compression algorithms [18], [65]. However, a local DSP is preferred over continuous RF transmission to realize lower power systems as some signal processing (e.g., feature extraction) is less costly to perform locally than to transmit raw data. For example, a recent low-power MedRadio transmitter consumes 67 μ W for continuous RF transmission [46], significantly higher power than needed for feature extraction [2], [34].

A survey of recent state-of-the-art ECG AFEs indicates that the noise-limited amplifier's power consumption is generally $10 \times$ larger than the low-resolution, low-speed SAR ADC [1]– [2]. For example, the ECG AFE presented in [1] dissipates only 67 nW in the ADC but 559 nW in the amplifier. This results from advances in technology scaling that have dramatically improved the Figure-of-Merit (FoM) for SAR ADCs [22]. However, minor/no technology improvements have been made in the fundamental noise efficiency of amplifiers typically limited by the transconductance efficiency of transistors biased in subthreshold [23]. As such, for amplifier power reductions, the noise specification, from $\sim 1 \ \mu V_{\rm rms}$ as in earlier work [5], has been significantly relaxed to levels such as 26 $\mu V_{\rm rms}$ in recent work [4] while compromising the signal quality and limiting the applications. Operational transconductance amplifier (OTA)-stacking is a technique to improve noise efficiency [40]-[41] and can be readily integrated with the concept presented here for further benefit.

In this work, we employ the concept of relaxing the noise as in recent low accuracy sensors [2], [4], but only during select regions over an entire cardiac cycle such that the features of interest are always acquired with high fidelity and thereby do not sacrifice the feature extraction capabilities of the system. This forms the underlying motivation behind this work enabling data-dependent savings, specifically focusing on the amplifier.



Fig. 2. Limitations of prior work with data-dependent power savings and emphasis of this work.

A distinguishable feature of this work, as highlighted in Fig. 2, is to emphasize the amplifier contrary to prior works focusing on the ADC or the transmitter to utilize the data-dependent power reduction concept in a meaningful fashion and achieve substantial power savings. A recent photoplethysmogram (PPG) sensor used a similar concept by turning on the power-hungry light-emitting diode (LEDs) only over a window near the expected peak [47]. However, if the peak lies outside the window determined by a moving average filter, it is missed, and a recovery phase is needed. The data is still acquired in this work but with lower accuracy, and the upcoming window is automatically adjusted using an LMS adaptive filter.

Apart from the nW-level AFEs, recent years have seen development in several other aspects of bio-potential signal acquisition as well [54–63]. These works have focused on ultra-high input impedance [55], high linearity [54], robustness to interferences [56], area efficiency [61], and direct digitization [62]. In many of these works, the input stage noise has a substantial influence over the power. It may be possible to integrate the data-dependent power reduction technique presented here in these designs.

III. PROPOSED ADAPTIVE ACQUISITION

The proposed digitally-assisted system is shown in Fig. 1(a). The AFE has multiple digitally controllable knobs, notably the amplifier noise, which can be dynamically reconfigured to trade the signal fidelity with the power consumption adaptively. Other tunable parameters include the amplifier gain and the ADC sampling rate/resolution to aid in efficient signal acquisition. Dynamic time warping (DTW) is used to extract bio-signal features in the DSP. The DSP also contains the adaptive acquisition strategy for the system.

As shown in Fig. 1(b), an ECG signal is characterized by the P-Q-R-S-T peaks detected in real-time by the DTW algorithm. Also, evident is that the distinctive ECG features (*e.g.*, the QRS complex) occur only over a small fraction of the period (less than 15%) and repeat continuously in a well-defined, predictable fashion. This low activity and quasi-periodicity create an opportunity for data-dependent savings like the one illustrated in the example in Fig. 1(b). The feature extraction accuracy remains consistent in the proposed acquisition strategy wherein only specific regions of interest around the peaks are captured with high fidelity compared to the conventional case when the entire signal is captured with high fidelity. An LMS-based adaptive



Fig. 3. Reconfigurable chopper stabilized biopotential amplifier.

linear predictor directs the dynamic noise-power reconfiguration. With only one prediction per heartbeat needed, this extra filter operates at a very slow rate (*i.e.* for a typical heart rate of 72 beats/min, the filter updates at \sim 1 Hz), thereby imposing a negligible power overhead, making the power savings using the proposed technique feasible.

The proposed technique enables power savings for longterm ECG recording applications/studies where capturing slow cardiac feature variability is important. Specifically, the slow variability in peak position and magnitude (*i.e.* the PR interval, QRS width, ST segment, etc.) are essential for diagnosing, classifying, and predicting various heart diseases [31], characterizing sleep stages [66], monitoring correlations or anomalies in patients with other diseases such diabetes [67], or those taking medication [68], etc. With the quasi-periodicity being maintained for such applications, the recording can be performed adaptively. Extreme cardiac irregularities, such as rapid changes in the heart rate, can still be reliably detected since the signal is always acquired, allowing the adaptive acquisition to be instantly disabled and operate the AFE in its highest fidelity mode if needed. As a result, no compromise in the real-time anomaly detection capability is made, whereas, for slow cardiac variability classification applications, one can benefit from the data-dependent power saving technique proposed here.

IV. RECONFIGURABLE ANALOG FRONT-END CIRCUIT

The front-end biopotential sensing circuit is realized using a chopper-stabilized amplifier with a noise-power trade-off. The



Fig. 4. OTA topologies: (a) Conventional single-tail and (b) Dual-tail complementary input.

digitization is performed using a rate and resolution reconfigurable SAR ADC. The implementation of these reconfigurable analog circuits is discussed below.

A. Noise-Tunable Chopper Amplifier

A capacitively-coupled chopper amplifier architecture similar to those presented in [22]–[24] is employed and shown in Fig. 3. The use of chopper-stabilization mitigates the otherwise dominant flicker noise in the low-frequency regime also occupied by ECG signals. The large dc offset resulting from electrode polarization is rejected by a dc servo-loop using an off-chip capacitor, C_{int} , that integrates the residual offset, cancels it at the amplifier input, and sets the high-pass corner frequency. Impedance boosting from a positive feedback loop ensures that the switched capacitor resistance caused by the chopper modulator does not degrade the amplifier's input impedance and is implemented from [26]. This avoids signal attenuation at the input and improves resilience to electrode mismatch. The amplifier has an array of switchable feedback capacitors, $C_{\rm fb}$, that control the closed-loop gain, $A_{\rm v} = C_{\rm i} / C_{\rm fb}$. The impedance boosting capacitors, $C_{\rm ib}$, are tuned in tandem with the feedback capacitors and equal in size to $C_{\rm fb}$, while the input capacitor, $C_{\rm i}$, is fixed to ensure that the amplifier input impedance remains constant regardless of the gain setting.

The first stage OTA current is tunable (100-675 nA) to enable fine-grain control over the amplifier noise-power trade-off. It is implemented with a dual-tail complementary input pair rather than the more conventional single-tail version (Fig. 4). The main benefit is that this allows a wide current-tuning range because the output common-mode (CM) voltage of the single-tail differential pair is determined by the tail current and the sizes of transistors $M_{\rm a3,4}$ whereas the output CM voltage of the dual-tail topology is independent of the tail current when both the top and the bottom tails are switched simultaneously. For low-supply voltage operation, it is important to have the output CM voltage fixed to maximize signal swing, avoid unwanted distortion while switching current modes, and minimize the complexity of the common-mode feedback (CMFB) circuitry. The complementary input pair also has a lower input-referred noise due to the $2\times$ transconductance by reusing the current and thus has better power efficiency.



Fig. 5. Noise tunable dual-tail complementary input OTA with CMFB.

The agile mode switching forces additional requirements on the CMFB. A simple CMFB with resistors $R_{\rm cmfb}$ forming a resistive divider, as shown in Fig. 4(b), is not suitable since the OTA's open-loop gain, $A_{\rm v,ol}$, changes with its bias current resulting in an unwanted non-linearity during reconfiguration by presenting slightly different closed-loop gains over different segments of the acquired signal. For $A_{\rm v,ol}$ to remain relatively constant over a wide range of the bias currents, $R_{\rm cmfb}$ must be sufficiently larger than $R_{\rm o}$, namely

$$A_{\rm v,ol} = G_{\rm m} \left(R_{\rm o} || R_{\rm cmfb} \right) \approx G_{\rm m} R_{\rm o} = \left(\frac{2I_{\rm D}}{\eta V_{\rm T}} \right) \left(\frac{1}{\lambda I_{\rm D}} \right)$$
(1)

where $G_{\rm m}$ and $R_{\rm o}$ are the OTA's transconductance and output impedance, respectively, η , $V_{\rm T}$, and λ are device parameters, namely the sub-threshold coefficient, thermal voltage, and channel length modulation coefficient, respectively, and $I_{\rm D}$ is the drain current. In practice, this is hard to achieve, requiring an alternative that presents only a capacitive load.

The OTA implementation is shown in Fig. 5. Multiple NMOS and PMOS tail current source cells that can be switched simultaneously enable the current tunability. For the CMFB, each PMOS tail cell utilizes additional transistors $M_{t1,2}$ in deep triode acting as linear resistors. The desired CM voltage, $V_{\rm CM}$, is applied to the triode transistors $M_{t1,2,c}$ by a replica bias circuit with devices analogous to those in a unit tail source. The effective resistance equality with $M_{t1,2}$ and $M_{t1,2,c}$ having equal source-drain voltages and carrying the same current forces the output CM voltage to be $V_{\rm CM}$. Additional details on this CMFB technique can be found in [48]. The performance of this triode CMFB at achieving a constant $A_{\rm v,ol}$ (as compared to a resistive-divider based CMFB with a 100 M Ω $R_{\rm cmfb}$) is shown in the simulation result in Fig. 5. This CMFB relies on matching between the triode and the PMOS tail devices, which is ensured by sizing. From a Monte-Carlo simulation (n = 100), the output CM voltage deviation remains within ± 4 mV, which is acceptable given this first stage OTA output has a low signal swing. G Ω -valued pseudo resistors for $R_{\rm cmfb}$ is an alternative approach; however, the associated CM bandwidth is low, which is unsuitable for agile switching. The OTA's bias current is set



Fig. 6. SAR ADC: (a) circuit architecture and (b) dynamic comparator.

via the NMOS gate voltage, $V_{\rm bn}$, generated using a conventional constant- $g_{\rm m}$ reference circuit. The OTA bandwith, which would otherwise vary across the current modes, is kept constant by designing the front-end amplifier to be wideband and using an anti-aliasing filter to band limit the signal.

B. SAR ADC

The reconfigurable SAR ADC is shown in Fig. 6(a). The input is sampled onto the top plate of a binary-weighted capacitor array, with 15 fF unit capacitors using bootstrapped switches [27]. The successive reference generation employs the switching scheme presented in [28], where for the first conversion, the signal is sampled with the MSB capacitor preset to $V_{\rm ref}$. The following conversion proceeds by either resetting the MSB or keeping it preset depending on the comparator decision and switching the MSB-1 capacitor to a preset state. The process is repeated for subsequent cycles in a monotonic fashion. This switching technique ensures a constant DAC CM voltage, reducing the comparator's signal-dependent offset while realizing an energy-efficient conversion. The comparator is implemented with a two-stage architecture with a dynamic pre-amplifier followed by a regenerative latch, as shown in Fig. 6(b) [29]. The resolution reconfiguration functionality (5- to 9-bits) with efficient power-scaling is incorporated using tri-state switches on the capacitors' bottom plate. Each resolution decrement is realized by floating the MSB capacitor(s) and starting the bit-cycling operation from the next largest capacitor. In this fashion, the energy drawn from the references scales with the resolution.

C. Adaptive AFE Operation

The DSP interacts with the analog circuitry through a scan chain into which the desired mode-programming control/config bits are sent in serially. The amplifier chopping, the dynamic



Fig. 7. Timing diagram of the reconfigurable AFE.

reconfiguration, and the ADC sampling operation are all performed synchronously, as shown in Fig. 7. As in [30], to realize chopper spike filtering, the sampling instant always arrives just before the onset of the next chopping phase or at the very end of the current chopping phase, thereby allowing maximum time for the transient spikes occurring due to the finite bandwidth to settle. The dynamic OTA reconfiguration is also performed right after an ADC sampling event to allow maximal settling time for any abrupt transients during the mode switching. With a 1 kSps sampling rate, any mode switching perturbation has 1 ms to settle. The amplifier mode reconfigurations are considerably instantaneous, as indicated by simulations during the design phase and confirmed by measurement results presented later.

An important aspect related to the dynamic reconfiguration is that any abrupt transients that occur while switching the CM current are mostly CM as well, appearing at the first stage's output, which the low CM gain of the second stage rejects. The output CM voltage of the overall amplifier is the same as that of the second stage, set by its CMFB, and is independent of the first stage's mode switching. With mismatch, part of these CM artifacts appear in differential-mode, with a substantial lowfrequency component as they repeat quasi-periodically every cardiac cycle and henceforth are chopped and filtered out.

The amplifier and the ADC were connected via an off-chip programmable gain amplifier to scale the analog signal to the ADC's full-scale and an active anti-aliasing filter to band limit the signal and attenuate the chopper ripple while also providing flexibility in testing. An on-chip realization of these would require very little power since the front-end amplifier gain attenuates its noise. The SAR ADC driver implemented in [2] consumed only 0.3 nW with a similar 10 fF unit capacitor. A simple RC filter for anti-aliasing with no power overhead can also be used, as in [35]. Residual out-of-band artifacts (e.g., baseline-wander, ripple, etc.) are further removed by digital filtering in the DSP back-end, a common practice before postprocessing, such as in [4]. The filtering requirement could have been relaxed by using a ripple rejection loop but was omitted here to focus on noise-power reconfigurability such that additional wide bandwidth loops do not impact this key feature. The AFE is designed such that OTA1 with its CMFB consumes 80-540 nW, OTA2 consumes 40 nW, the dc servo loop consumes 25 nW, the digital circuitry (SPI/config register) for mode programming



Fig. 8. (a) DTW-based ECG feature extraction (b) algorithm overview.

consumes 100 nW (due to leakage that would be absent if the DSP was integrated on-chip), and the SAR ADC consumes 30 nW.

V. DSP BACK-END

A. ECG Feature Extraction

Real-time detection and classification of ECG features, characterized by P-Q-R-S-T peaks, is of great importance in cardiac activity monitoring. Several algorithms based on discrete wavelet transform (DWT) [36], dynamic time warping (DTW) [43–44], [64], windowing and adaptive thresholding [45], etc., have been developed to detect these features. A DTW technique that finds an optimal matching pattern between two time-domain sequences was adopted in this work. As illustrated in Fig. 8(a), the DTW algorithm finds an alignment between a selected template consisting of a single cardiac cycle and the signal acquired in real-time. Thus, each data point in the template and the distinctive features get monotonically mapped to a corresponding point or feature in the cardiac cycle acquired in real-time, thereby detecting each feature's time-instants. Notably, the DTW technique (and, in general, many feature extraction algorithms) is susceptible to noise so that the detection accuracy of a specific feature depends mainly upon the transient noise corrupting the surrounding area of the acquired waveform.

The DTW algorithm is briefly described below for completeness. Consider two time-domain sequences, $X = \{x_1, \ldots, x_N\}$ and $Y = \{y_1, \ldots, y_M\}$, and a cost function, c(x, y), that compares the different features in X and Y such that c(x, y) is small (low cost) if x and y are similar and large if dissimilar. A warping path, $p = \{p_1, \ldots, p_L\}$, is defined as an alignment or a monotonic mapping with each $p_i = (n, m)$ relating an element of X with index n to one in Y with index m. The goal is to find an optimal warping path with the minimal overall cost, also known as the DTW distance, DTW[X, Y]. This is achieved by computing an accumulated optimal cost matrix D using a dynamic



Fig. 9. Adaptive linear predictor (a) functionality and (b) performance.

programming approach. Each element of this matrix D is defined as D(n,m) = DTW[X(1:n), Y(1:m)], the DTW distance of the partial prefix sequences X(1:n) and Y(1:m)(where a partial sequence X(1:n) consists of only the first *n* elements of *X* (*i.e.* $X(1:n) = \{x_1, ..., x_n\}$). Further, using the fact that a warping path involves a monotonic mapping, one can obtain the relation D(n,m) = $min\{D(n-1,m-1), D(n-1,m), D(n,m-1)\} + c(x_n, y_m).$ The computation of D is performed using the above relation and the boundary conditions $D(n,0) = D(0,m) = -\infty$ and D(0,0) = 0. Finally, once D is available, the desired optimal warping path is determined by traversing backward from the end element $p_{\rm L} = (N, M)$ using $p_{\rm L-1} =$ $arg\{ min\{D(n-1,m-1), D(n-1,m), D(n,m-1)\}\}.$ To summarize, as shown in Fig. 8(b), the DTW involves the computation of a 2D matrix and a path along it, which corresponds to the desired mapping.

B. Dynamic Reconfiguration Algorithm

To leverage the quasi-periodicity of ECG signals, a prediction of an upcoming region/peak of interest is required. A well-established signal processing technique, the LMS-based adaptive linear predictive filter, was used. The filter uses the past and current P-Q-R-S-T peaks detected by the DTW algorithm to predict the upcoming features' arrival time. The AFE reconfiguration strategy and LMS filter are independent of the feature extraction algorithm used.

The functionality of this filter is described here with the help of an R-peak prediction application. As shown in Fig. 9(a), the R-R peak interval separation as detected by DTW is provided as an input x[n] to the adaptive filter implemented as follows:

$$y[n] = w_1[n] x[n-1] + w_2[n] x[n-2]$$

$$+ \cdots + w_N[n] x[n-N] \tag{2}$$

$$e[n] = y[n] - x[n] \tag{3}$$

$$w_i[n+1] = w_i[n] + x[n-i]e[n]\mu$$
(4)

where w_i are the filter coefficients that are adapted such that the error e[n] between the predicted R-R intervals y[n] and the ones detected x[n] is minimized based on an LMS algorithm with adaptation parameter μ . The performance of such an adaptive filter for dynamic reconfiguration was previously presented and studied for heart-rate variability (HRV) in [32].

A 5 tap adaptive filter is implemented and found to be sufficiently accurate in predicting features in quasi-periodic ECG signals that generally exhibit a steady or slow feature variability with time. Fig. 9(b) shows this prediction ability and accuracy evaluated using ECG signals with artificially added random HRV. The prediction error plotted is defined as $\sigma_{\Delta R}/\mu_R$, where $\sigma_{\Delta R}$ is the standard deviation in the differences between predicted and detected R-R intervals and μ_R is the average of detected R-R intervals. This error is typically <5% for HRV of 10 beats/minute. To put this in perspective, the HRV of healthy people during steady work-out (measured by dynamometry) is around 3 beats/minute [33]. The filter functionality could be extended to predict ECG features other than the R-peak in the same fashion. The digital adaptation algorithm also has additional benefits. Namely, even in the presence of interference and other uncorrelated ECG artifacts, the feature (e.g., the QRS region) is predicted, contrary to detecting the interference's activity as is expected to be the case with some existing derivative-based approaches [5].

C. DSP Power Overhead

The DSP back-end was implemented off-chip in an FPGA for the evaluation of various predictors and flexibility purposes. The feature extractor is an inevitable component in any ECG sensing system, and hence its power need not be considered. However, to put things into perspective, the reported power consumption of existing state-of-the-art on-chip DSP is around 450 nW for comprehensive ECG feature-extraction in [34] and around 45 nW for only R-peak detection in [2]. The estimated power for the DTW is 620 nW from simulations of a synthesized design. This is comparable to the AFE power, which is generally a few hundreds of nW [1]. On the other hand, the predictor is an additional component in the system but introduces only a negligible power overhead if integrated on-chip. One prediction is needed per heartbeat $\sim 60/72$ seconds, implying that the predictor's digital circuit operates at a rate around 1 Hz. Furthermore, during regular operation with consistent cardiac activity, the adaptive filter coefficients converge to realize a moving average filter such that the circuit activity is often quite low. This slow operation and low activity translate to a very low dynamic power consumption. From simulations of a synthesized design in the 65 nm CMOS process, the power consumption of this adaptive predictor is less than 10 nW.

VI. MEASUREMENT AND EXPERIMENTAL RESULTS

Measurements from the chip fabricated in a 65 nm CMOS process, occupying 2 mm² with pads (Fig. 10) and operated from a 0.8 V supply are presented. The test setup to evaluate the



Fig. 10. Chip micrograph with layout snapshot.



Fig. 11. Test set-up for characterizing the ECG acquisition system.



Fig. 12. Measured input-referred noise PSD in the 35-dB gain mode.

proposed adaptive ECG acquisition system is shown in Fig. 11 and is similar to standard setups used to characterize physiological sensing front-ends, such as in [35]. Experimental results using anomalous ECG records from established databases are presented to validate the system's functionality.

A. Chopper Amplifier

The chopper amplifier can be precisely programmed to achieve several gain and noise modes. The gain is programmable from 22 to 43 dB, and the measured bandwidth is 250 Hz across all modes as set by the anti-aliasing filter. Notably, fine-grain control of the amplifier's input-referred white noise floor from $125 - 195 \text{ nV}/\sqrt{\text{Hz}}$ is achieved by trading power in 12 discrete uniform steps from 272 – 734 nW, as shown in Fig. 12. The chopping frequency was 4 kHz (more than twice the measured 1/f corner of 1.15 kHz) and mitigated the otherwise dominant flicker noise. Table I lists the amplifier's input-referred total integrated noise (35-dB gain mode). The noise power doesn't scale linearly with the current here since there are residual noise sources such as the dc-servo, input biasing resistors, second stage, etc. The amplifier also achieves good dc offset rejection to account for electrode polarization. Applying a dc offset at the input, it was measured that offsets less than $\pm 100 \text{ mV}$ can be tolerated without saturating the amplifier. The measured

TABLE I Measured Amplifier Power vs. Input-Referred Noise

Power (nW)	Noise (µV _{rms})	Noise PSD @ 100 Hz (nV/ $\sqrt{\text{Hz}}$)
272	3.64	195.2
378	3.23	170.8
434	3.01	157.8
620	2.87	134.6
734	2.38	125.2



Fig. 13. Measured amplifier common-mode rejection ratio (CMRR).

 TABLE II

 MEASURED ADC RESOLUTION AND POWER FOR DIFFERENT MODES

Mode	ENOB	SFDR (dB)	Power (nW)
9-bit	8.75	67.1	34.6
8-bit	7.87	62.8	21.9
7-bit	6.91	61.0	13.4
6-bit	5.93	60.1	9.8
5-bit	4.93	59.4	9.1

amplifier input impedance at 50 Hz improved from 6.5 to 105 M Ω by enabling the impedance boosting loop. A CMRR greater than 82 dB across all modes was measured, as shown in Fig. 13. The measured amplifier's total harmonic distortion (THD) for an 11 mV_{pp} input is ~1.3% (-38 dB) across all the power modes, confirming that the fixed power second stage limits the distortion.

B. SAR ADC

The resolution reconfigurable ADC with a 1 kSps sampling rate consumes 35 nW in the 9-bit mode and 9 nW in the 5-bit mode, thereby offering a power scalable resolution reconfiguration as listed in Table II. In the 9-bit mode, the SAR ADC exhibits an ENOB of 8.75 bits, a DNL of +0.43/-0.8 LSBs, INL of +0.58/-0.47 LSBs, and an SFDR of 67.1 dB measured at 1 kSps. The ADC's linearity in its highest resolution mode, shown in Fig. 14, remains consistent up to 10 kSps. The linearity versus resolution decrement (Table II) degrades slightly, owing to the leakage and parasitics associated with tri-stating, but this does not impact the eventual ENOB.



Fig. 14. ADC spectra in 9-bit mode ($f_s = 1$ kSps, $f_{in} = 93$ Hz, and N = 16384).



Fig. 15. Measured ECG signal and instantaneous power while employing various dynamic reconfiguration strategies to selectively capture specific regions of interest with higher accuracy.

C. Adaptive ECG Acquisition

The dynamic noise reconfiguration functionality of the AFE provides opportunities for several adaptive acquisition strategies to save power depending upon the desired application. The most fundamental among the possible strategies is to capture only the QRS-complex with high fidelity selectively. In Fig. 15, an ECG signal transient and instantaneous power consumption are shown corresponding to such a QRS-only adaptive acquisition implementation. This acquisition strategy is beneficial in arrhythmia detection/classification applications, usually the focus of low-power sensors. The measured ECG transient also shows a discerning compromise with the signal quality in the non-QRS low-power regime. The measured instantaneous power indicates agile mode switching leading to $2.5 \times$ data-dependent power savings toggling between 272 and 734 nW for an average of 310 nW.



Fig. 16. Predictor performance with HRV (MIT-db record 203).

If the application only requires heart-rate/R-peak detection, the adaptive acquisition does not need to be done, and the AFE can continuously be operated in the low power mode. However, for QRS characterization, since the signal amplitude at the QRS wave's onsets and ends are weak, low noise levels around the features are essential [36]. Capturing the entire QRS rather than just the R-peak is helpful for arrhythmia classification, where the distinctive QRS-complex's periodicity, width, variability in amplitude, etc., provide crucial diagnostic information [37].

Furthermore, with the ability to predict each of the P-Q-R-S-T peaks individually, the concept could be extended to realize a wide variety of data-dependent acquisition strategies. To illustrate these, shown in Fig. 15, are the measured instantaneous power plots corresponding to the implementation of a couple of such strategies. These examples indicate that further diagnostic functionality can be added by capturing the P and T waves with high-fidelity while trading-off with data-dependent power savings (463 nW average power) or a further lower power, yet precise, arrhythmia classification can be performed by capturing alternate QRS regions with high fidelity instead of each consecutive one (295 nW average power).

D. Predictor Performance

The proposed system's functionality was evaluated extensively using ECG records from standard databases like the MIT-BIH Arrhythmia database (MIT-db) [38] and the QT-database (QT-db) [39]. The discrete-time samples of these records are upsampled, interpolated, and filtered to realize clean analog inputs for the AFE and are sent out via a high-speed digitalto-analog converter (DAC). These datasets are further scaled to 1 mV $_{\rm pp}$ using the input side attenuator (Fig. 11) to have the same signal power for consistency of comparison. The filter's ability to accurately track the quasi-periodic ECG with its typical slow variability and quickly adapt (after suffering from false prediction due to an abrupt variability, such as arrhythmias) is clear from the example in Fig. 16, wherein the predictor performance is evaluated using a transient ECG waveform (record 203 from MIT-db) exhibiting slight HRV. Additional illustrative examples for the predictor performance are shown in Fig. 17. The instantaneous magnitude of errors in R-peak predictions $\in_{\Delta R}$ (detected R-peak position – predicted R-peak position) normalized by the average R-R interval $T_{\Delta R}$ are plotted. In Fig. 17(a), a region of extreme irregular HRV is accompanied by equally large prediction errors. But these errors reduce quickly as the HRV subsides. On the other hand, Fig. 17(b) shows a



Fig. 17. Instantaneous R-peak prediction errors over (a) MIT-db record 203 and (b) QT-db record 116.

Record	# beats	# P	# Q	# R	# S	# T
M-101	1897	1801	1808	1809	1805	1811
		94.9%	95.3%	95.3%	95.1%	95.4%
M-103	2077	2029	2024	2023	2023	2025
		97.7%	97.5%	97.4%	97.4%	97.5%
M-215	3326	3234	3238	3236	3236	3231
		97.2%	97.4%	97.2%	97.2%	97.1%
Q-116	2876	2870	2869	2869	2869	2868
		99.8%	99.8%	99.8%	99.8%	99.8%
Q-307	1968	1963	1965	1965	1965	1966
		99.7%	99.8%	99.8%	99.8%	99.9%
Q-231	3890	3877	3882	3885	3879	3867
		99.6%	99.8%	99.9%	99.7%	99.4%

TABLE III ECG PEAK PREDICTIONS

M-xxx and Q-xx indicates ECG data from MIT-db and QT-db, respectively # F denotes the number of correct predictions of the feature/peak F

case where the quasi-periodicity always holds and thus has low prediction errors.

Although the predictor cannot track extreme irregular cardiac activity (*i.e.* when the quasi-periodicity property doesn't hold), no compromise with the system's anomaly detection performance is made. This is because the case of persistent large prediction errors is itself an anomaly indicator that can be used to take appropriate countermeasures or stop the adaptive acquisition and capture these events with high accuracy. In other words, the predictor has a secondary functionality of acting as a simple yet efficient, real-time anomaly detector while assisting the AFE power savings over prolonged durations of slow HRV.

The prediction of each ECG characteristic peak is further quantified in terms of the statistical results in Table III. The number and percentage of correct predictions for each P-Q-R-S-T peak are listed. A prediction is considered correct if the prediction error is <5% of the average cardiac cycle, which ensures that the detected peak falls well within the window for adaptive acquisition. Overall, the percentage of missed predictions was $\sim5\%$ for records from the MIT-db that have moderate HRV and <0.3% for records from the QT-db that have a fairly regular



Fig. 18. DTW feature extraction performance (a) transient waveforms and (b) ECG peak detection errors for QRS only reconfiguration.

TABLE IV ECG PEAK DETECTION ERRORS

	Q-116	Q-307	Q-231			
	$\sigma_{\Delta t} \mid \sigma_{\Delta t} / T_{avg}$	$\sigma_{\Delta t} \mid \sigma_{\Delta t} / T_{avg}$	$\sigma_{\Delta t} \mid \sigma_{\Delta t} / T_{avg}$			
	(ms) (%)	(ms) (%)	(ms) (%)			
	P-peak					
A	1.34 0.16	2.01 0.24	2.19 0.27			
В	13.91 2.47	14.78 2.53	12.98 2.25			
Q-peak						
Α	1.47 0.20	1.33 0.16	1.91 0.26			
В	10.11 2.12	10.89 2.15	13.00 2.81			
R-peak						
A	0.89 0.12	1.05 0.14	1.41 0.20			
В	2.33 0.41	2.89 0.45	4.71 0.96			
	S-peak					
Α	1.77 0.24	1.81 0.26	1.19 0.18			
В	16.11 3.01	17.63 3.15	13.00 2.81			
	T-peak					
Α	1.14 0.12	1.01 0.10	1.99 0.25			
В	11.75 2.13	12.24 2.26	10.22 1.85			

Case A: All P-Q-R-S-T acquired adaptively Case B: Always in low power mode

Q-xx indicates ECG data from QT-db

HR with low HRV, thus clearly establishing the feasibility of employing the proposed LMS-based predictor to save power for long-term ECG monitoring where the quasi-periodicity property of ECG is expected to hold over lengthy durations.

E. Feature Extraction Performance

A key benefit of the proposed work is that since the feature extraction algorithms operate on transient waveforms to detect features occurring over only a small fraction of the period, selectively acquiring pristine data over limited regions of the cycle suffices for the signal analysis while still maintaining high detection accuracy for the features of interest. This aspect of

	[1]	[4]	[2]	[21]	[5]	[42]	[54]	This work
Application	ECG	ECG	ECG	ECG	ECG	ECG	ExG	ECG
Technology node	180 nm	65 nm	65 nm	180 nm	180 nm	180 nm	180 nm	65 nm
Supply (V)	1.3	0.6	0.6	0.6	1.8	1.2	1.8	0.8
				Amplifier				
Power (nW)	559 ⁺	1	16.8	831 ⁺	600 ⁺	504	2,300 +	734 ¹ , 272 ²
Gain (dB)	20-31	32	51 - 96	35 - 70	40 - 60	66 - 74	42 - 50	22-43
BW (Hz)	130	370	250	156	170	1000	150	250
THD (%)	1 (110 mV _p in)	_	2.8	1 (8 mV _{pp} in)	-	-	0.01 (12 mV _{pp} in)	$\begin{array}{c} 1.3^1, \ 1.3^2 \\ (11 \ mV_{pp} \ in) \end{array}$
Input-refferred noise (µV _{rms})	4.9	26	6.52	3.44	1.1	4.6	0.733	2.38 ¹ , 3.64 ²
NEF [*]	10.8	2.1	2.64	12.5	7.91	3.7	2.3	5.3 , 5.0 , 2.9 ⁺
				ADC	-		-	
Power (nW) @ 1 kSps	67	1.1	1.8 (500 Sps)	19	4,400 (2 kSps)	_	(2.5 kSps)	41.6
ENOB	8.96	9.2	7.14	8.01	10.6	_	>9.23	8.75
INL (LSBs)	-	0.87	1.8	0.55	0.3	-	-	0.58
DNL (LSBs)	-	0.96	1	0.48	0.5	-	_	0.80
Feature Extractor / DSP								
Technique	Analog QRS band power	_	FDM algo. on-chip DSP	_	Analog QRS band power	Analog QRS band power	_	DTW algo. off-chip DSP
Features detected	R-peak	_	R-peak	_	R-peak	R-peak	_	P,Q,R,S,T peaks
Power (nW)	100+	_	45	_	212	92	-	630
System								
AFE power (nW)	626	3	18.6	850	14,000	-	5,300	307 - 769
$P_{\rm Amp}/P_{\rm ADC}$	8.34	0.91	9.33	43.74	2.41	-	_	6.53 - 17.64

TABLE V Performance Summary and Comparison to State-of-the-Art Bio-AFEs

¹At highest power mode with 35 dB gain. ²At lowest power mode with 35 dB gain.

*Digital SPI power is excluded for reported NEF.

+Effective NEF computed using the avg. current with adaptive acquisition and noise at highest power mode.

⁺Estimated.

preserving the feature detection accuracies and simultaneously enabling the data-dependent savings are highlighted here.

Fig. 18 shows a single cardiac cycle snapshot with annotated detected peaks for a known ECG record from a standard database played at the AFE's input. The detection accuracy is further quantified in terms of the relative error $\sigma_{\Delta t}/T_{avg}$ where Δt is the difference in detected peak-position with data acquired adaptively relative to that acquired in high accuracy mode and T_{avg} is the average separation between consecutive detected peaks over the entire data. Such peak detection errors corresponding to a QRS-only reconfiguration strategy are listed in Fig. 18(b). It can be seen that with data acquired adaptively, detection errors are $5 \times$ lower for the QRS peaks than those for P and T peaks (which are corrupted with greater noise), highlighting the selective detection accuracy. These data demonstrate that no compromise is made with the detection accuracy of the features of interest while slightly sacrificing the detection accuracy outside that region to save power. Additionally, it was found that high-noise levels as in [4] added artificially (also shown in Fig. 18) to the same known ECG result in false detections (>5% errors), thereby justifying the targeted noise-levels. Further, the predictive adaptation that depends upon this accurately detected QRS-complex also remains unaffected with dynamic reconfiguration.

Table IV shows a comprehensive quantification of the feature extractions by comparing the performance of the individual P-Q-R-S-T peak detections with an adaptive, selective high-fidelity acquisition of each peak (Case A) compared to those

with signal acquisition always performed in low-power/lowfidelity mode (Case B). The minor errors in Case A affirm the detection accuracy preservation benefits. It may be noted that the detection accuracies reported are dependent on the feature extraction algorithm used. An improved algorithm could relax the noise requirements and lower the power. Additionally, an aggressive noise power reconfiguration could also better leverage the reconfiguration technique for greater power savings. However, irrespective of the exact noise trade-off and the detection accuracies corresponding to this implementation, the efficacy of the proposed technique holds since, in general, the ECG feature extraction is known to be sensitive to noise with improving the noise tolerance being an important objective of several prior detection algorithms [36], [43]. Apart from noise, the signal fidelity across different power modes may exhibit slight dependence on other amplifier characteristics such as settling of chopping artifacts, slewing, etc. and are also captured in the reported detection accuracies.

F. Comparison to State-of-the-Art ECG AFEs

A performance summary of the designed reconfigurable AFE, along with a comparison to state-of-the-art works, is presented in Table V. The amplifier standalone achieves a noise efficiency factor (NEF) of \sim 5. The data-dependent power savings are quantified in terms of an effective NEF computed using the average current with adaptive acquisition and noise at the highest power mode, which corresponds to the accuracy of the features of interest. The effective NEF is improved to 2.9. While this effective NEF is inferior to the best reported NEF using an OTA-stacking technique in [41], this work's key novelty was to demonstrate an alternate technique to address the noise-power trade-off. The proposed work can also be integrated with OTA-stacking for further improvements using the data-dependent power reduction technique. The table also indicates $P_{\rm Amp}/P_{\rm ADC}$, the ratio between the amplifier and the ADC power for such existing work, justifying the focus on the data-dependent amplifier power reduction. Finally, to summarize, compared to prior ECG recording systems, all the characteristic P-Q-R-S-T peaks can be detected with accuracies corresponding to <2.4 μ V_{rms} noise using a dynamically reconfigurable AFE consuming state-of-the-art low average power for such diagnostic quality noise levels.

VII. CONCLUSION

This paper reported a reconfigurable AFE design that achieves data-dependent power savings by dynamically switching modes in an agile fashion to trade power with performance. The amplifier noise was determined to be the dominant power demanding design aspect and made a tunable knob in the design. A DTW algorithm and an LMS linear predictive adaptive filter were incorporated to perform the cardiac feature extraction and guide the data-dependent adaptation. The AFE was operated to selectively capture various ECG features like the QRS complex P-wave and T-wave with higher precision. A $2.5 \times$ power reduction was achievable by employing an agile, dynamic ORS-only reconfiguration of the AFE. Comprehensive system performance characterizations were performed using ECG records from standard databases to establish the feasibility of using the LMS predictor on the ECG's quasi-periodicity and demonstrate data-dependent savings without compromising the eventual feature extraction accuracy.

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REFERENCES

- L. Yan *et al.*, "24.4 A 680nA fully integrated implantable ECG-acquisition IC with analog feature extraction," in *Proc. IEEE Int. Solid-State Circuits Conf. Dig. Tech. Papers*, 2014, pp. 418–419.
- [2] D. Jeon et al., "24.3 An implantable 64nW ECG-monitoring mixed-signal SoC for arrhythmia diagnosis," in Proc. IEEE Int. Solid-State Circuits Conf. Dig. Tech. Papers, 2014, pp. 416–417.
- [3] A. Kalb, Y. Sharma, and J. Virtanen, "Interference-immune diagnostic quality ECG recording for patient monitoring applications," in *Proc. IEEE Int. Custom Integr. Circuits Conf.*, 2017, pp. 1–4.
- [4] P. Harpe, H. Gao, R. van Dommele, E. Cantatore, and A. van Roermund, "21.2 A 3nW signal-acquisition IC integrating an amplifier with 2.1 NEF and a 1.5fJ/conv-step aDC," in *Proc. IEEE Int. Solid- State Circuits Conf.*, 2015, pp. 1–3.
- [5] R. F. Yazicioglu, S. Kim, T. Torfs, H. Kim, and C. Van Hoof, "A 30 μW analog signal processor ASIC for portable biopotential signal monitoring," *IEEE J. Solid-State Circuits*, vol. 46, no. 1, pp. 209–223, Jan. 2011.

- [6] X. Zou, X. Xu, L. Yao, and Y. Lian, "A 1-V 450-nW fully integrated programmable biomedical sensor interface chip," *IEEE J. Solid-State Circuits*, vol. 44, no. 4, pp. 1067–1077, Apr. 2009.
- [7] T. Yang, J. Lu, M. S. Jahan, K. Griffin, J. Langford, and J. Holleman, "A configurable 5.9 µW analog front-end for biosignal acquisition," in *Proc. IEEE Custom Integr. Circuits Conf.*, 2015, pp. 1–4.
- [8] M. Yip and A. P. Chandrakasan, "A resolution-reconfigurable 5to-10-Bit 0.4-to-1 v power scalable SAR ADC for sensor applications," *IEEE J. Solid-State Circuits*, vol. 48, no. 6, pp. 1453–1464, Jun. 2013.
- [9] S. Fateh, P. Schonle, L. Bettini, G. Rovere, L. Benini, and Q. Huang, "A reconfigurable 5-to-14 bit SAR ADC for battery-powered medical instrumentation," *IEEE Trans. Circuits Syst. Regular Papers*, vol. 62, no. 11, pp. 2685–2694, Nov. 2015.
- [10] S. Mondal, C. L. Hsu, R. Jafari, and D. Hall, "A dynamically reconfigurable ECG analog front-end with a 2.5× data-dependent power reduction," in *Proc. IEEE Int. IEEE Custom Integr. Circuits Conf.*, 2017, pp. 1–4.
- [11] G.-Y. Huang, S.-J. Chang, C.-C. Liu, and Y.-Z. Lin, "A 1-μW 10-bit 200kS/s SAR ADC with a bypass window for biomedical applications," *IEEE J. Solid-State Circuits*, vol. 47, no. 11, pp. 2783–2795, Nov. 2012.
- [12] T. Wang, H. Li, Z. Ma, Y. Huang, and S. Peng, "A bypass-switching SAR ADC with a dynamic proximity comparator for biomedical applications," *IEEE J. Solid-State Circuits*, vol. 53, no. 6, pp. 1743–1754, Jun. 2018.
- [13] F. M. Yaul and A. P. Chandrakasan, "11.3 A 10b 0.6nW SAR ADC with data-dependent energy savings using LSB-first successive approximation," in *Proc. IEEE Int. Solid-State Circuits Conf. Dig. Tech. Papers*, 2014, pp. 198–199.
- [14] S. Jeong *et al.*, "A 120nW 8b Sub-ranging SAR ADC with signaldependent charge recycling for biomedical applications," *Proc. Symp. VLSI Circuits*, vol. 2015, pp. C60–C61, Jun. 2015.
- [15] Y. Song, Z. Xue, Y. Xie, S. Fan, and L. Geng, "A 0.6-V 10-bit 200-kS/s fully differential SAR ADC with incremental converting algorithm for energy efficient applications," *IEEE Trans. Circuits Syst. Regular Papers*, vol. 63, no. 4, pp. 449–458, Apr. 2016.
- [16] Y. Li, A. L. Mansano, Y. Yuan, D. Zhao, and W. A. Serdijn, "An ECG recording front-end with continuous-time level-crossing sampling," *IEEE Trans. Biomed. Circuits Syst.*, vol. 8, no. 5, pp. 626–635, Oct. 2014.
- [17] M. Trakimas and S. R. Sonkusale, "An adaptive resolution asynchronous ADC architecture for data compression in energy constrained sensing applications," *IEEE Trans. Circuits Syst. Regular Papers*, vol. 58, no. 5, pp. 921–934, May 2011.
- [18] A. M. R. Dixon, E. G. Allstot, D. Gangopadhyay, and D. J. Allstot, "Compressed sensing system considerations for ECG and EMG wireless biosensors," *IEEE Trans. Biomed. Circuits Syst.*, vol. 6, no. 2, pp. 156–166, Apr. 2012.
- [19] F. Tang et al., "A low power and fast tracking Light-to-Frequency converter with adaptive power scaling for blood spo2 sensing," *IEEE Trans. Biomed. Circuits Syst.*, vol. 13, no. 1, pp. 26–37, Feb. 2019.
- [20] T. Marisa *et al.*, "Pseudo asynchronous level crossing ADC for ECG signal acquisition," *IEEE Trans. Biomed. Circuits Syst.*, vol. 11, no. 2, pp. 267–278, Apr. 2017.
- [21] M. Yip, J. L. Bohorquez, and A. P. Chandrakasan, "A 0.6V 2.9µW mixed-signal front-end for ECG monitoring," in *Proc. Symp. VLSI Circuits*, Honolulu, HI, USA, 2012, pp. 66–67.
- [22] B. Murmann, "ADC Performance Survey 1997-2021." Accessed: Mar. 10, 2021. [Online]. Available: https://web.stanford.edu/~murmann/ adcsurvey.html
- [23] R. R. Harrison and C. Charles, "A low-power low-noise CMOS amplifier for neural recording applications," *IEEE J. Solid-State Circuits*, vol. 38, no. 6, pp. 958–965, Jun. 2003.
- [24] T. Denison, K. Consoer, W. Santa, A.-T. Avestruz, J. Cooley, and A. Kelly, "A 2 uW 100 nV/rtHz chopper-stabilized instrumentation amplifier for chronic measurement of neural field potentials," *IEEE J. Solid-State Circuits*, vol. 42, no. 12, pp. 2934–2945, Dec. 2007.
- [25] N. Verma, A. Shoeb, J. Bohorquez, J. Dawson, J. Guttag, and A. P. Chandrakasan, "A micro-power EEG acquisition SoC with integrated feature extraction processor for a chronic seizure detection system," *IEEE J. Solid-State Circuits*, vol. 45, no. 4, pp. 804–816, Apr. 2010.
- [26] Q. Fan, F. Sebastiano, J. H. Huijsing, and K. A. A. Makinwa, "A 1.8 µW 60 nV/√Hz capacitively-coupled chopper instrumentation amplifier in 65 nm CMOS for wireless sensor nodes," *IEEE J. Solid-State Circuits*, vol. 46, no. 7, pp. 1534–1543, Jul. 2011.
- [27] M. Dessouky and A. Kaiser, "Input switch configuration suitable for railto-rail operation of switched op amp circuits," *Electron. Lett.*, vol. 35, no. 1, pp. 8–10, Jan. 1999.

- [28] D. Zhang, A. Bhide, and A. Alvandpour, "A 53-nW 9.1-ENOB 1-kS/s SAR ADC in 0.13- m CMOS for medical implant devices," *IEEE J. Solid-State Circuits*, vol. 47, no. 7, pp. 1585–1593, Jul. 2012.
- [29] M. van Elzakker, E. van Tuijl, P. Geraedts, D. Schinkel, E. Klumperink, and B. Nauta, "A 1.9 μW 4.4fJ/Conversion-step 10b 1MS/s charge-redistribution ADC," in *Proc. Solid-State Circuits Conf.*, 2008, pp. 244–610.
- [30] R. F. Yazicioglu, P. Merken, R. Puers, and C. Van Hoof, "A 60 μW 60 nV/Hz readout front-end for portable biopotential acquisition systems," *IEEE J. Solid-State Circuits*, vol. 42, no. 5, pp. 1100–1110, May 2007.
- [31] D. Mann, D. Zipes, P. Libby, and R. Bonow, *Braunwald's Heart Disease: A Textbook of Cardiovascular Medicine*, 2-Volume Set, 10th ed. Amsterdam, Netherlands: Elsevier, 2014.
- [32] C. Zong, S. Mondal, D. A. Hall, and R. Jafari, "Digitally assisted analog Front-end power management strategy via dynamic reconfigurability for robust heart rate monitoring," *SIGBED Rev.*, vol. 12, no. 3, pp. 36–39, Aug. 2015.
- [33] M. Moser *et al.*, "Heart rate variability as a prognostic tool in cardiology. A contribution to the problem from a theoretical point of view," *Circulation*, vol. 90, no. 2, pp. 1078–1082, Aug. 1994.
- [34] X. Liu et al., "A 457 nW near-threshold cognitive multi-functional ECG processor for long-term cardiac monitoring," *IEEE J. Solid-State Circuits*, vol. 49, no. 11, pp. 2422–2434, Nov. 2014.
- [35] H. Chandrakumar and D. Marković, "An 80-mVpp linear-input range, 1.6-GΩ input impedance, low-power chopper amplifier for closed-loop neural recording that is tolerant to 650-mVpp common-mode interference," *IEEE J. Solid-State Circuits*, vol. 52, no. 11, pp. 2811–2828, Nov. 2017.
- [36] J. P. Martinez, R. Almeida, S. Olmos, A. P. Rocha, and P. Laguna, "A wavelet-based ECG delineator: Evaluation on standard databases," *IEEE Trans. Biomed. Eng.*, vol. 51, no. 4, pp. 570–581, Apr. 2004.
- [37] B. U. Kohler, C. Hennig, and R. Orglmeister, "The principles of software QRS detection," *IEEE Eng. Med. Biol. Mag.*, vol. 21, no. 1, pp. 42–57, Jan. 2002.
- [38] G. B. Moody and R. G. Mark, "The impact of the MIT-BIH arrhythmia database," *IEEE Eng. Med. Biol. Mag.*, vol. 20, no. 3, pp. 45–50, 2001.
- [39] A. L. Goldberger *et al.*, "PhysioBank, physiotoolkit, and physionet components of a new research resource for complex physiologic signals," *Circulation*, vol. 101, no. 23, pp. e215–e220, Jun. 2000.
- [40] S. Mondal and D. A. Hall, "An ECG chopper amplifier achieving 0.92 NEF and 0.85 PEF with AC-coupled inverter-stacking for noise efficiency enhancement," in *Proc. IEEE Int. Symp. Circuits Syst.*, Baltimore, MD, USA, 2017, pp. 1–4.
- [41] S. Mondal and D. A. Hall, "A 13.9 nA ECG amplifier achieving 0.86/0.99 NEF/PEF using AC-coupled OTA-Stacking," *IEEE J. Solid-State Circuits*, vol. 55, no. 2, pp. 414–425, Feb. 2020.
- [42] S. Bose, B. Shen, and M. L. Johnston, "26.5 A 20μW heartbeat detection System-on-Chip powered by human body heat for self-sustaining wearable healthcare," in *Proc. IEEE Int. Solid- State Circuits Conf.*, San Francisco, CA, USA, 2020, pp. 408–410.
- [43] H. J. L. M. Vullings, M. H. G. Verhaegen, and H. B. Verbruggen, "Automated ECG segmentation with dynamic time warping," in *Proc.* 20th Annu. Int. Conf. IEEE Eng. Med. Biol. Soc., 1998, pp. 163–166, vol. 1.
- [44] N. Kale, J. Lee, R. Lotfian, and R. Jafari, "Impact of sensor misplacement on dynamic time warping based human activity recognition using wearable computers," in *Proc. Conf. Wireless Health*, New York, NY, USA, 2012, Art. no. 7.
- [45] J. Pan and W. J. Tompkins, "A real-time QRS detection algorithm," *IEEE Trans. Biomed. Eng.*, vol. BME-32, no. 3, pp. 230–236, Mar. 1985.
- [46] S. Mondal and D. A. Hall, "A 67-μW ultra-low power PVT-Robust medradio transmitter," in *Proc. IEEE Radio Freq. Integr. Circuits Symp.*, 2020, pp. 327–330.
- [47] J. Lee, D. Jang, S. Park, and S. Cho, "A low-power photoplethysmogrambased heart rate sensor using heartbeat locked loop," *IEEE Trans. Biomed. Circuits Syst.*, vol. 12, no. 6, pp. 1220–1229, Dec. 2018.
- [48] B. Razavi, Design of Analog CMOS Integrated Circuits. New York, NY, USA: McGraw-Hill, 2001.
- [49] Z. Zhang, Q. Yu, J. Li, X. -Z. Wang, and N. Ning, "A 12-Bit dynamic tracking algorithm-based SAR ADC with real-time QRS detection," *IEEE Trans. Circuits Syst. I: Regular Papers*, vol. 67, no. 9, pp. 2923–2933, Sep. 2020.
- [50] S. Yim, Y. Park, H. Yang, and S. Kim, "Power efficient SAR ADC adaptive to input activity for ECG monitoring applications," in *Proc. IEEE Int. Symp. Circuits Syst.*, 2017, pp. 1–4.

- [51] M. Tohidi, J. K. Madsen, and F. Moradi, "Low-Power high-inputimpedance EEG signal acquisition SoC with fully integrated IA and signal-specific ADC for wearable applications," *IEEE Trans. Biomed. Circuits Syst.*, vol. 13, no. 6, pp. 1437–1450, Dec. 2019.
- [52] A. Das, S. Rout, A. Urso, and W. A. Serdijn, "Activity dependent multichannel ADC architecture using level crossing quantisation for atrial electrogram recording," in *Proc. IEEE Biomed. Circuits Syst. Conf.*, 2019, pp. 1–4.
- [53] Y. Hou *et al.*, "A 61-nW level-crossing ADC with adaptive sampling for biomedical applications," *IEEE Trans. Circuits Syst. II: Exp. Briefs*, vol. 66, no. 1, pp. 56–60, Jan. 2019.
- [54] Y.-P. Hsu, Z. Liu, and M. M. Hella, "A 12.3-μW 0.72-mm² fully integrated front-end IC for arterial pulse waveform and ExG recording," *IEEE J. Solid-State Circuits*, vol. 55, no. 10, pp. 2756–2770, Oct. 2020.
- [55] M. Chen *et al.*, "A 400 $g\omega$ input-impedance active electrode for noncontact capacitively coupled ECG acquisition with large linear-input-range and high CM-Interference-Tolerance," *IEEE Trans. Biomed. Circuits Syst.*, vol. 13, no. 2, pp. 376–386, Apr. 2019.
- [56] C. Ratametha, S. Tepwimonpetkun, and W. Wattanapanitch, "A 2.64-μW 71-dB SNDR discrete-time signal-folding amplifier for reducing ADC's resolution requirement in wearable ECG acquisition systems," *IEEE Trans. Biomed. Circuits Syst.*, vol. 14, no. 1, pp. 48–64, Feb. 2020.
 [57] Y. Zhao, Z. Shang, and Y. Lian, "A 2.55 NEF 76 dB CMRR DC-coupled
- [57] Y. Zhao, Z. Shang, and Y. Lian, "A 2.55 NEF 76 dB CMRR DC-coupled fully differential difference amplifier based analog front end for wearable biomedical sensors," *IEEE Trans. Biomed. Circuits Syst.*, vol. 13, no. 5, pp. 918–926, Oct. 2019.
- [58] Y. Hsu, Z. Liu, and M. M. Hella, "A 1.8 –65 dB THD ECG acquisition front-end IC using a bandpass instrumentation amplifier with Class-AB output configuration," *IEEE Trans. Circuits Syst. II: Exp. Briefs*, vol. 65, no. 12, pp. 1859–1863, Dec. 2018.
- [59] W. Bai, Z. Zhu, Y. Li, and L. Liu, "A 64.8 2.2 DC–AC configurable CMOS front-end IC for wearable ECG monitoring," *IEEE Sensors J.*, vol. 18, no. 8, pp. 3400–3409, Apr. 2018.
- [60] J. Yoo et al., "An 8-Channel scalable EEG acquisition SoC with patientspecific seizure classification and recording processor," *IEEE J. Solid-State Circuits*, vol. 48, no. 1, pp. 214–228, Jan. 2013.
- [61] L. B. Leene and T. G. Constandinou, "A 0.006 mm2 1.2 μW Analogto-Time converter for asynchronous bio-sensors," *IEEE J. Solid-State Circuits*, vol. 53, no. 9, pp. 2604–2613, Sep. 2018.
- [62] C. Pochet, J. Huang, P. P. Mercier, and D. A. Hall, "28.4 A 400mVpp 92.3 dB-SNDR 1kHz-BW 2nd-Order VCO-based exg-to-digital front-end using a multiphase gated-inverted ring-oscillator quantizer," in *Proc. IEEE Int. Solid- State Circuits Conf.*, 2021, pp. 392–394.
- [63] C. J. Deepu, X. Zhang, W. Liew, D. L. T. Wong, and Y. Lian, "An ECG-on-Chip with 535 nW/Channel integrated lossless data compressor for wireless sensors," *IEEE J. Solid-State Circuits*, vol. 49, no. 11, pp. 2435–2448, Nov. 2014.
- [64] Q. Zhang, D. Zhou, and X. Zeng, "A novel framework for motion-tolerant instantaneous heart rate estimation by phase-domain multiview dynamic time warping," *IEEE Trans. Biomed. Eng.*, vol. 64, no. 11, pp. 2562–2574, Nov. 2017.
- [65] C. J. Deepu, C. Heng, and Y. Lian, "A hybrid data compression scheme for power reduction in wireless sensors for IoT," *IEEE Trans. Biomed. Circuits Syst.*, vol. 11, no. 2, pp. 245–254, Apr. 2017.
- [66] P. Fonseca, X. Long, M. Radha, R. Haakma, R. M. Aarts, and J. Rolink, "Sleep stage classification with ECG and respiratory effort," *Physiol. Meas.*, vol. 36, no. 10, pp. 2027–2040, Oct. 2015.
- [67] S. Stern and S. Sclarowsky, "The ECG in diabetes mellitus," *Circulation*, vol. 120, no. 16, pp. 1633–1636, Oct. 2009.
- [68] P. J. Goodnick, J. Jerry, and F. Parra, "Psychotropic drugs and the ECG: Focus on the QTc interval," *Expert Opin. Pharmacother.*, vol. 3, no. 5, pp. 479–498, May 2002.



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