A Current-Measurement Front-End with 160dB Dynamic Range and 7ppm INL

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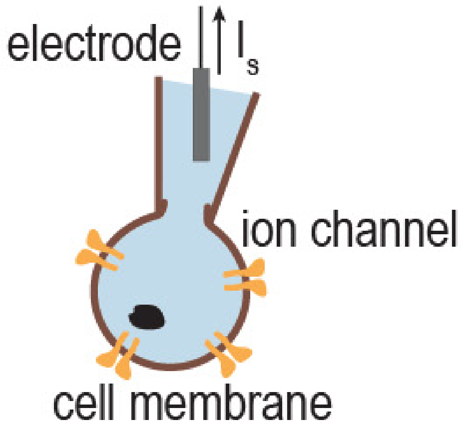
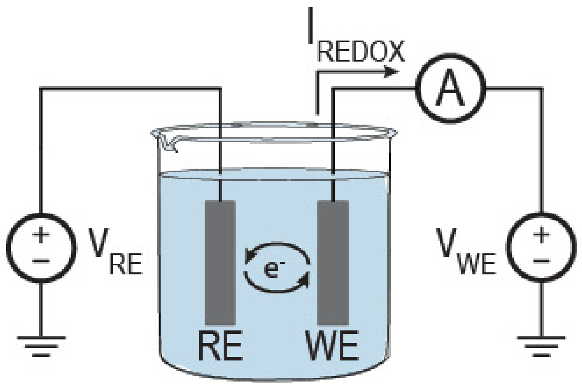
Motivation: Current Input Biosensors

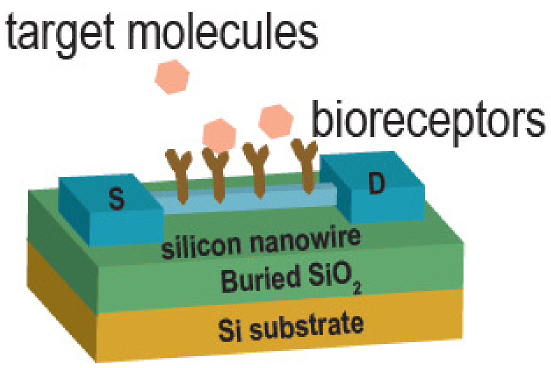
Patch Clamp



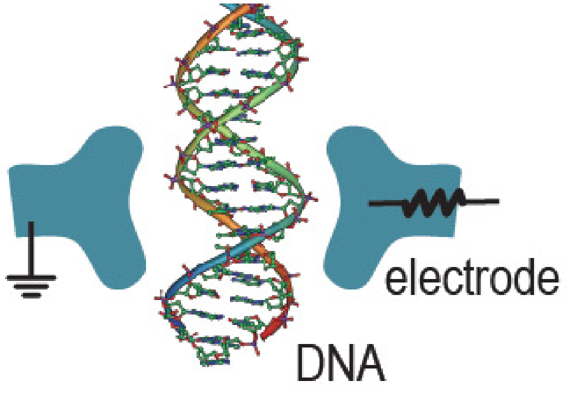
Electrochemical



Nanotube

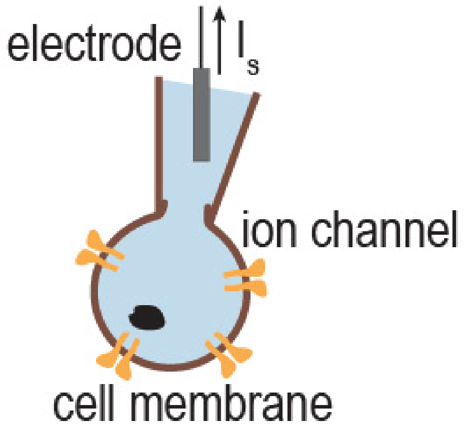


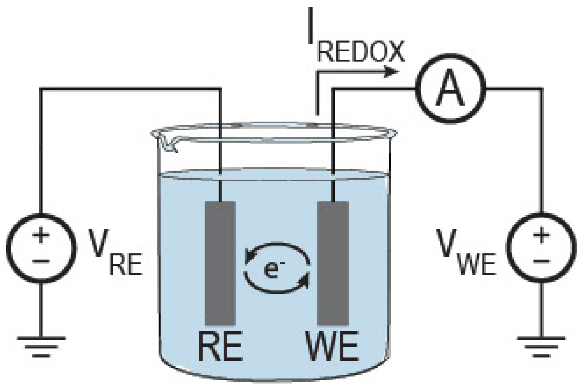
Nanopore

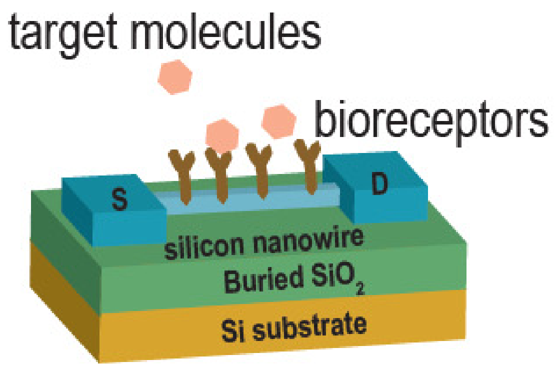


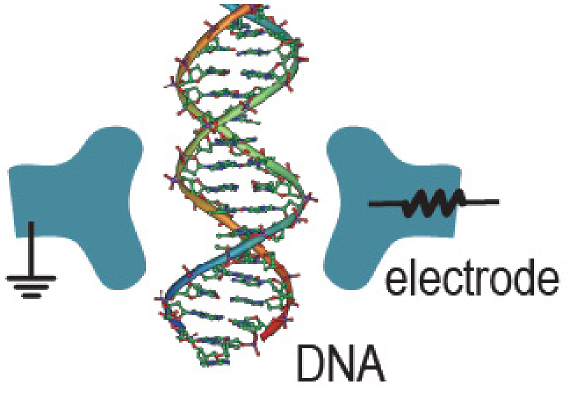
Motivation: Current Input Biosensors

Patch Clamp	Electrochemical	Nanotube	Nanopore



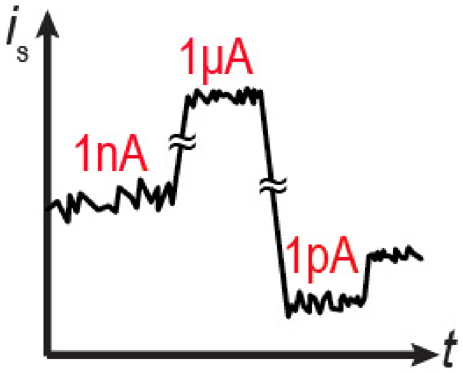






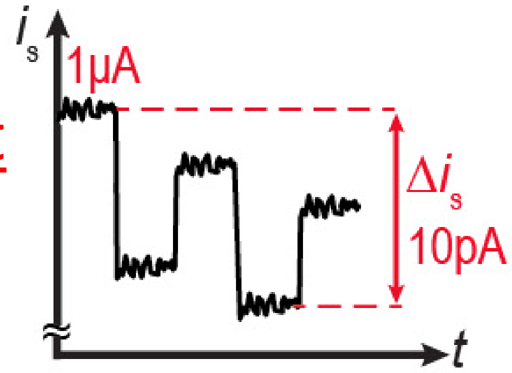
Large signal range

I_s = 1 pA – 1 μA



Small signal with large offset

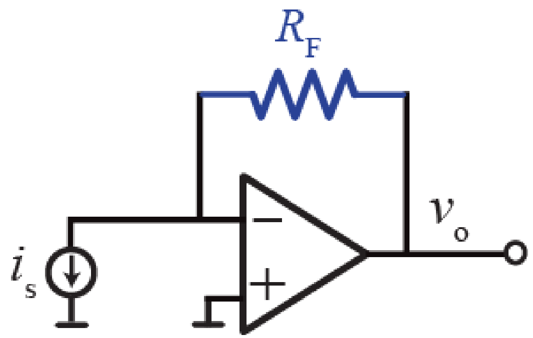
ΔI_s = 1 pA – 1 nA
with I_s = 1 nA – 1 μA



A front-end with >120dB DR and >60dB linearity is required.

Conventional Current-Input AFE

R-TIA



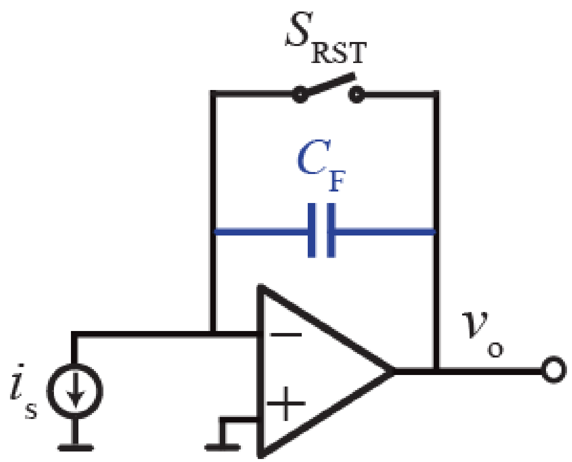
X High noise:

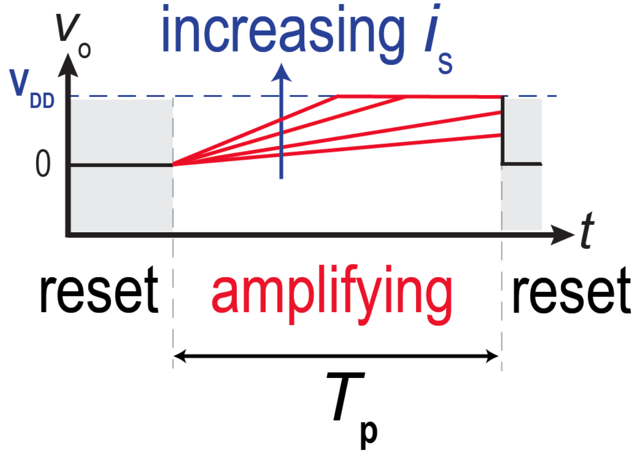
$$i_n^2 = BW \cdot 4k_BT/R_F$$

X Low DR:

$$i_{s,max} = V_{DD}/R_F$$

C-TIA





O Low noise

X Periodic reset

X Low DR:

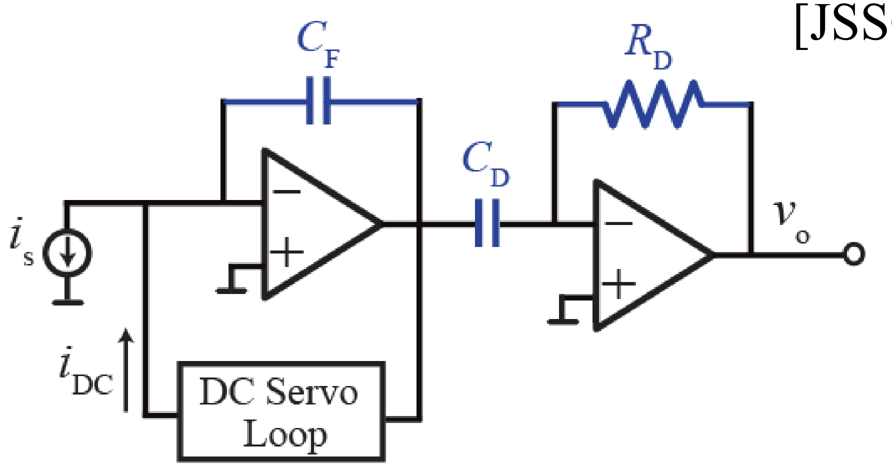
$$i_{s,max} = C_FV_{DD}/T_P$$

DR is limited by circuit noise and supply voltage.

Current-Input AFE Using C-TIA

C-TIA with DC servo loop

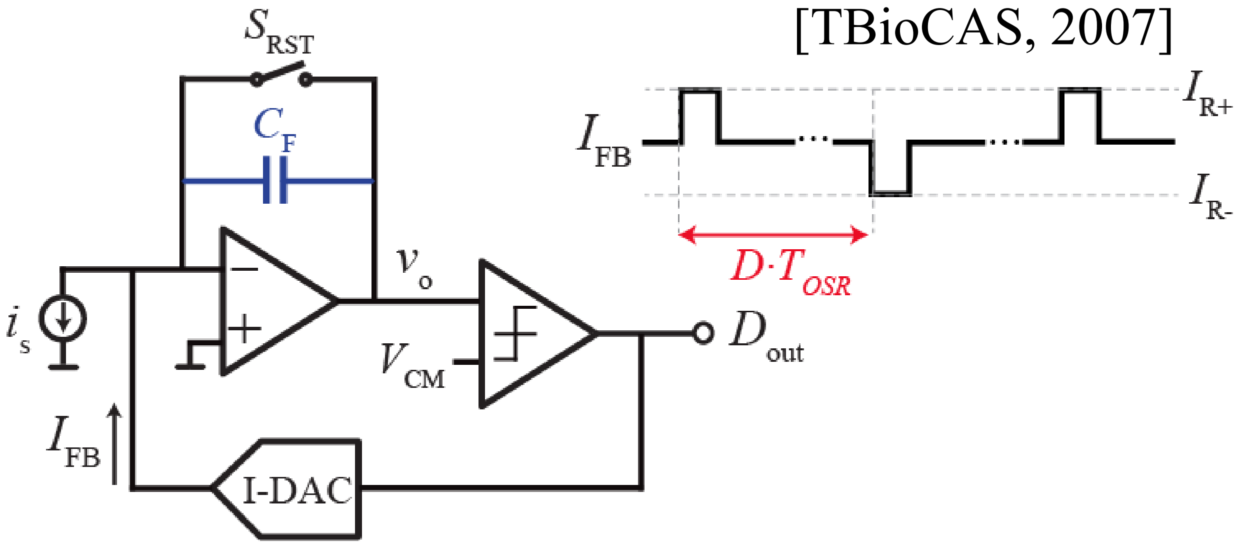
[JSSC, 2009]



- O Low noise
- O Continuous-time
- Δ Improved DR

ΔΣ w/ pulse modulation

[TBioCAS, 2007]



- O Low noise
- O High DR
- O Inherent digitization
- Δ Good linearity with slow f_s

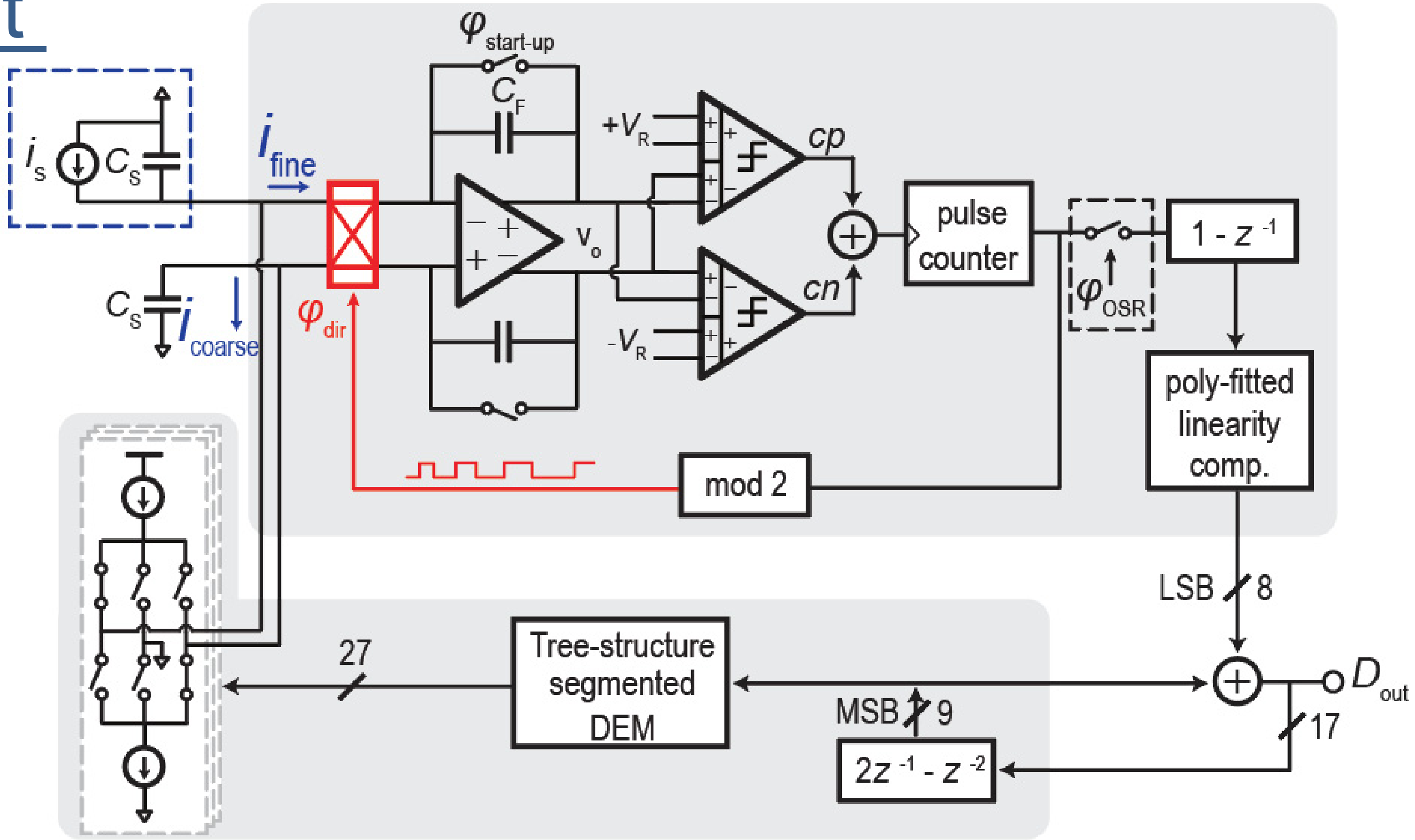
Challenge: Achieving >120dB DR and >60dB linearity

System Overview

Hourglass ADC

Input Current

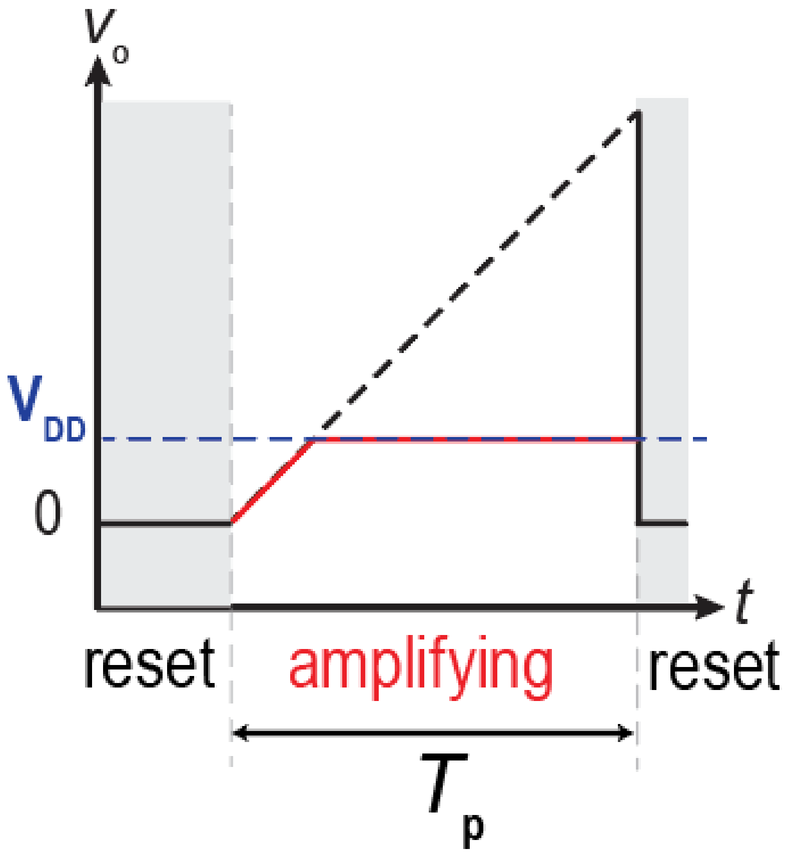
<1pA to 10μA



Predictive DAC

C-TIA with Improved DR

Conventional C-TIA

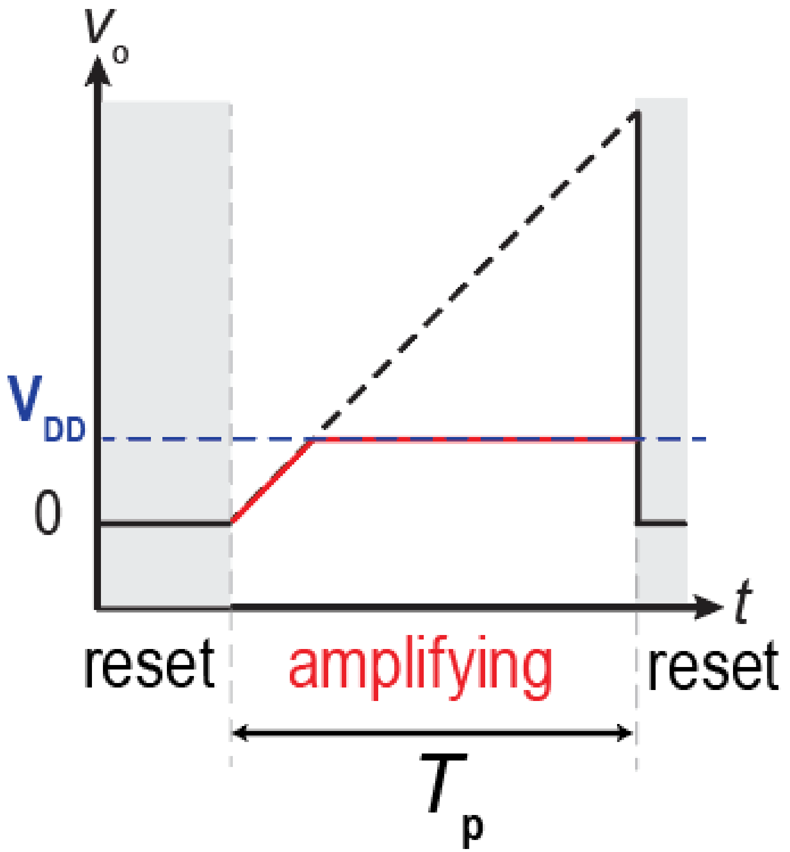


C_F saturates when $i_{sig} > C_F V_{DD}/T_p$

→ limited DR

C-TIA with Improved DR

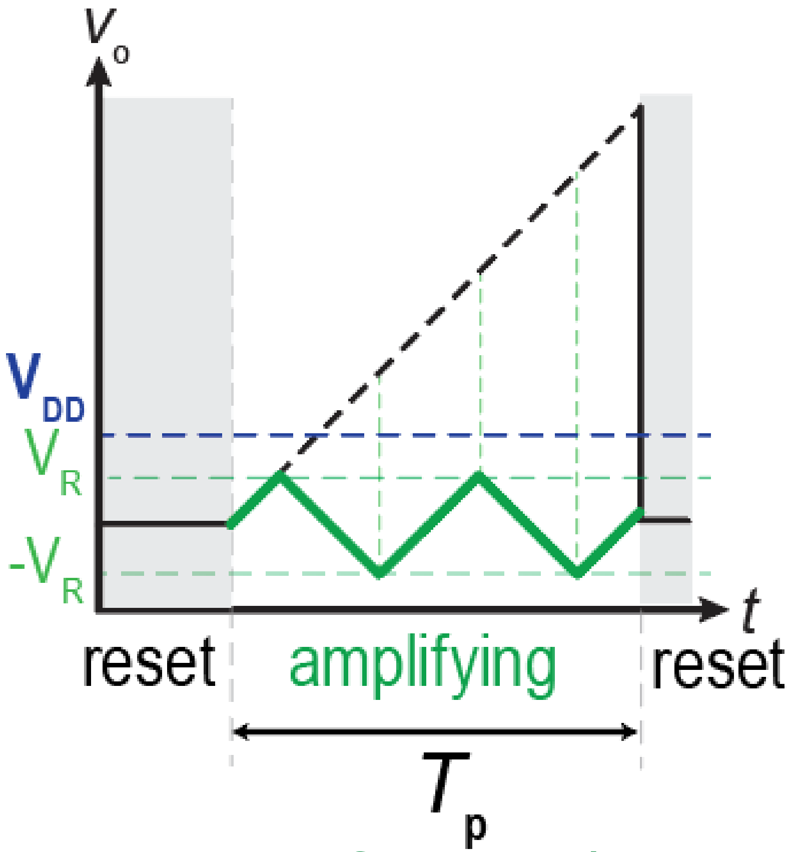
Conventional C-TIA



C_F saturates when $i_{sig} > C_F V_{DD}/T_p$

→ limited DR

C-TIA w/ Hourglass Switch

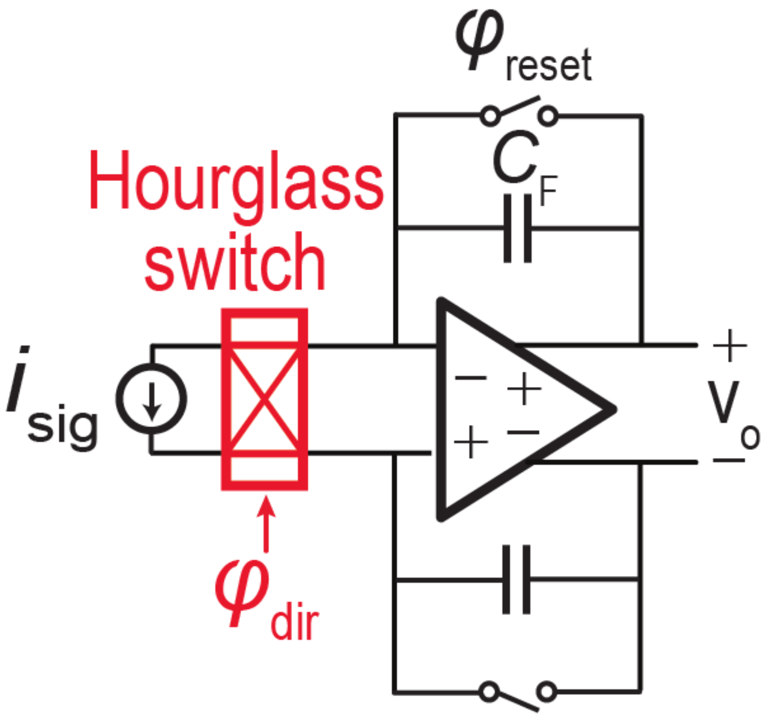


Keep amplifying w/o saturation

→ increased DR

C-TIA with Hourglass Switch

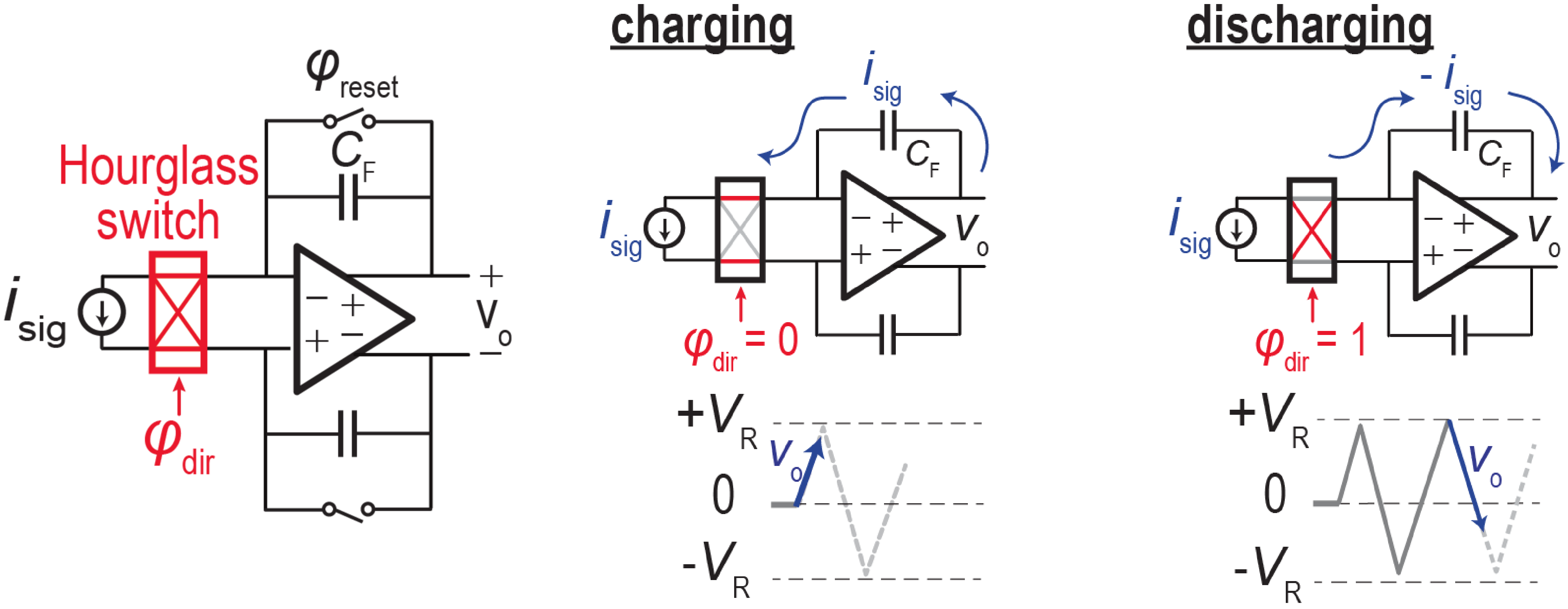
Goal: Increase DR, keep amplifying w/o saturation



C-TIA with Hourglass Switch

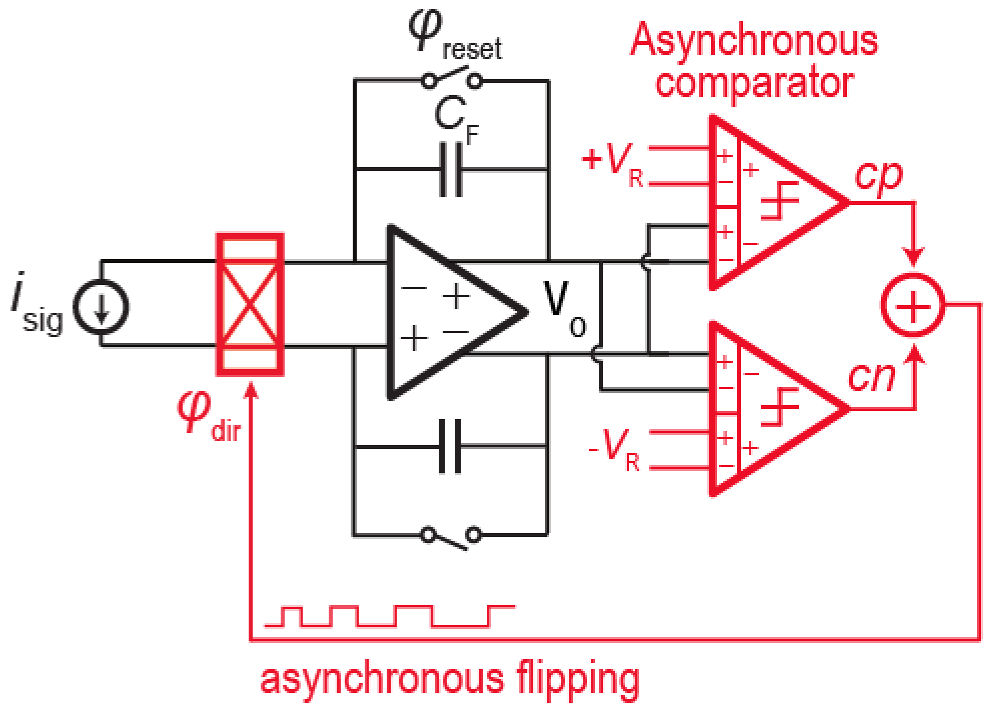
Goal: Increase DR, keep amplifying w/o saturation

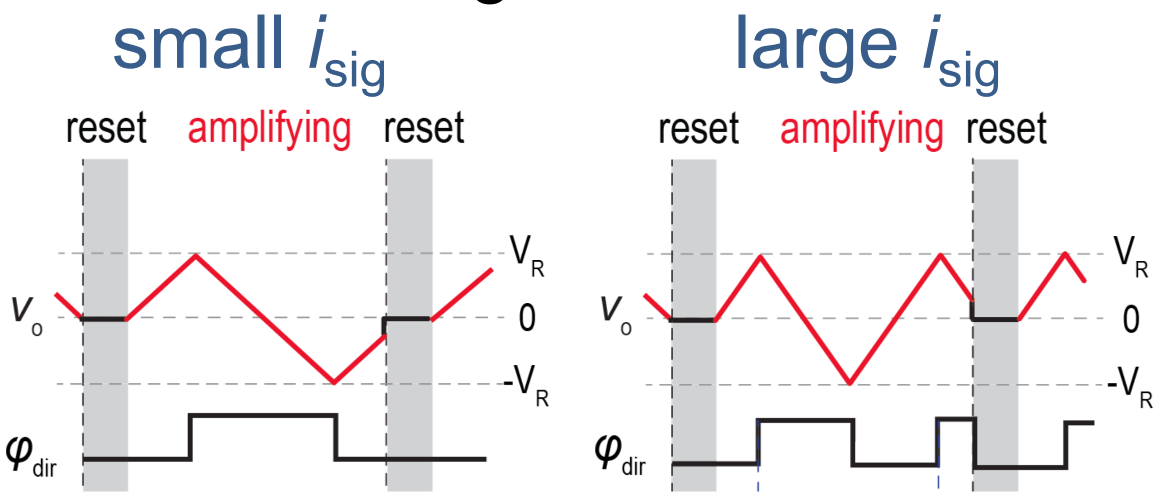
Method: Flipping the input polarity asynchronously



C-TIA with Hourglass Switch

- Two continuous-time comparators controls the hourglass switch



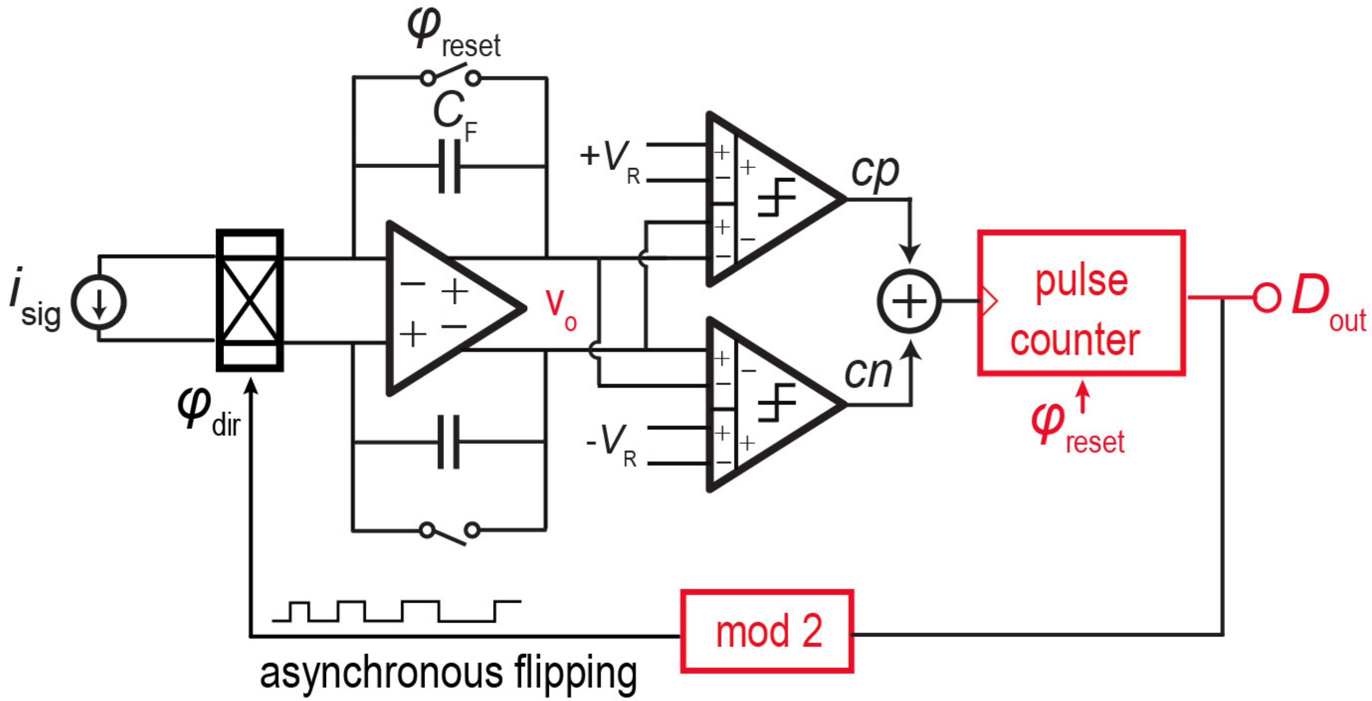


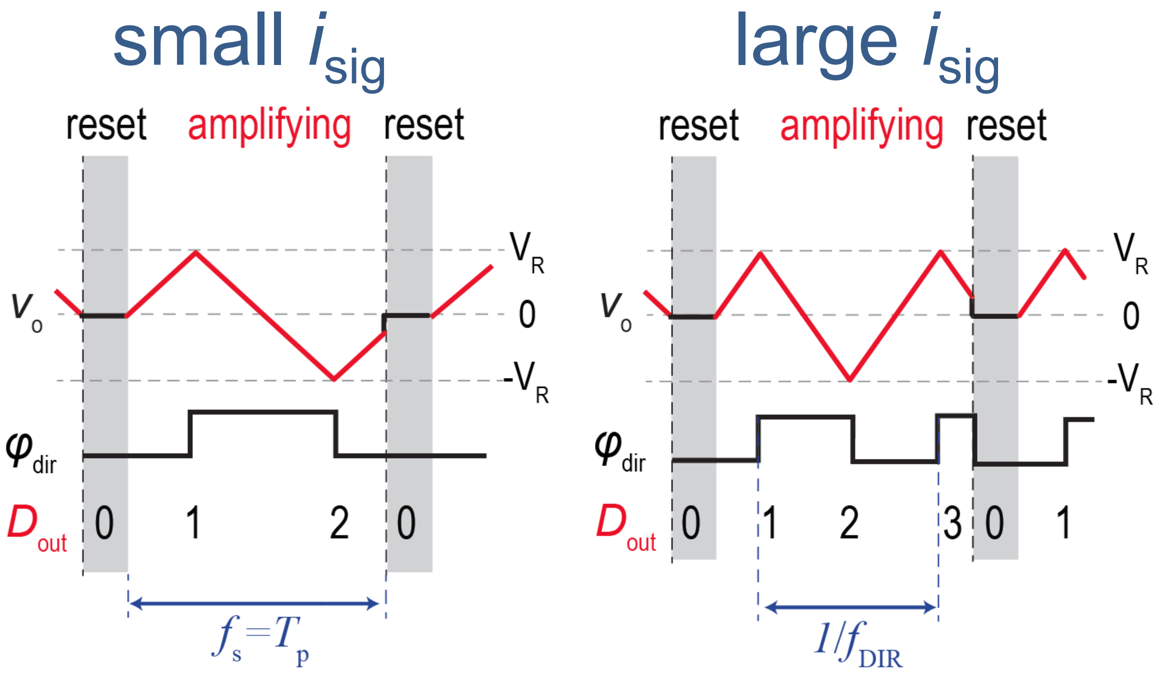
- C-TIA: low input-referred current noise
- Asynchronous Hourglass switching: $i_{sig} >> C_F V_{DD}/T_p$

The DR of a C-TIA is improved with an asynchronous Hourglass switch.

Hourglass ADC

- The comparators work as a 1-bit quantizer

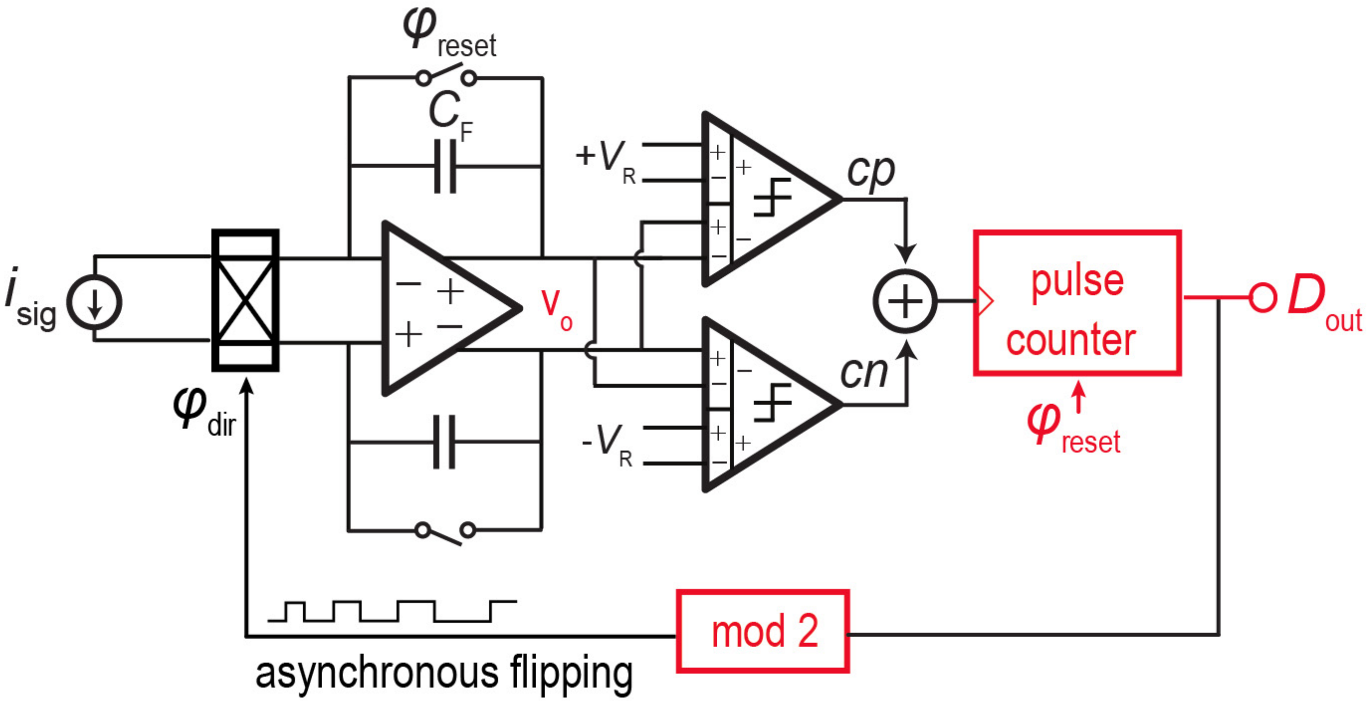


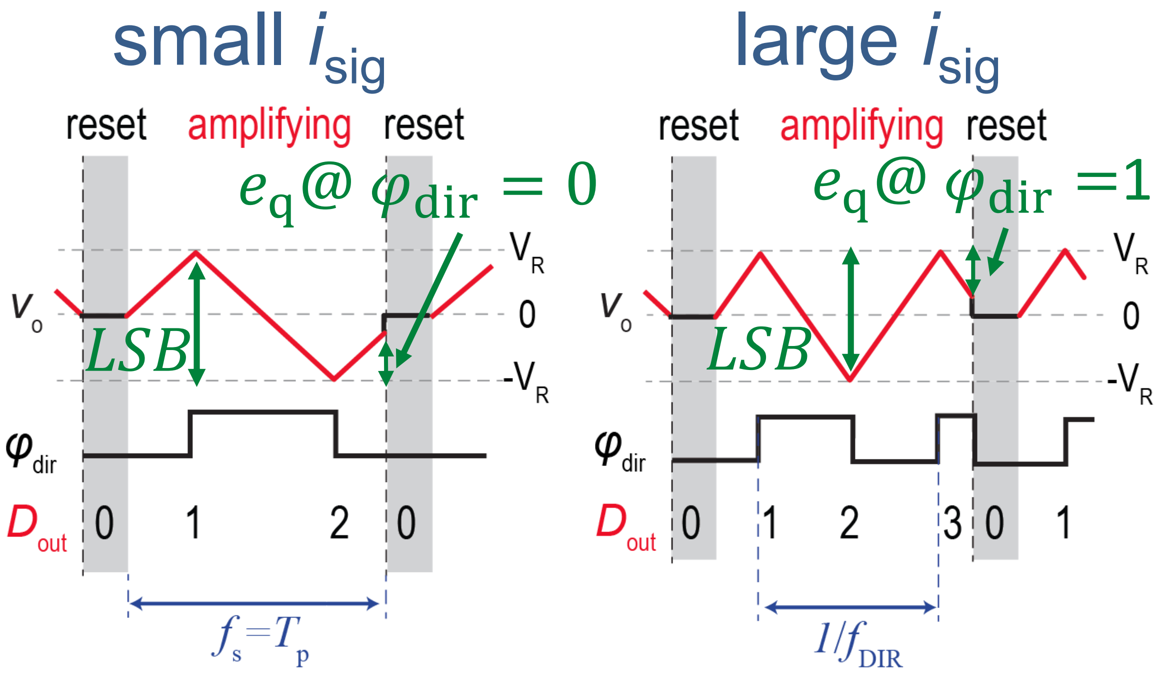


$$v_{\mathrm{o,unfolded}} \equiv \frac{i_{\mathrm{sig}} T_{\mathrm{p}}}{C_{\mathrm{F}}} = (2D_{\mathrm{out}} - 1)\, V_{\mathrm{R}} + e_{\mathrm{q}}$$

Hourglass ADC

- The comparators work as a 1-bit quantizer





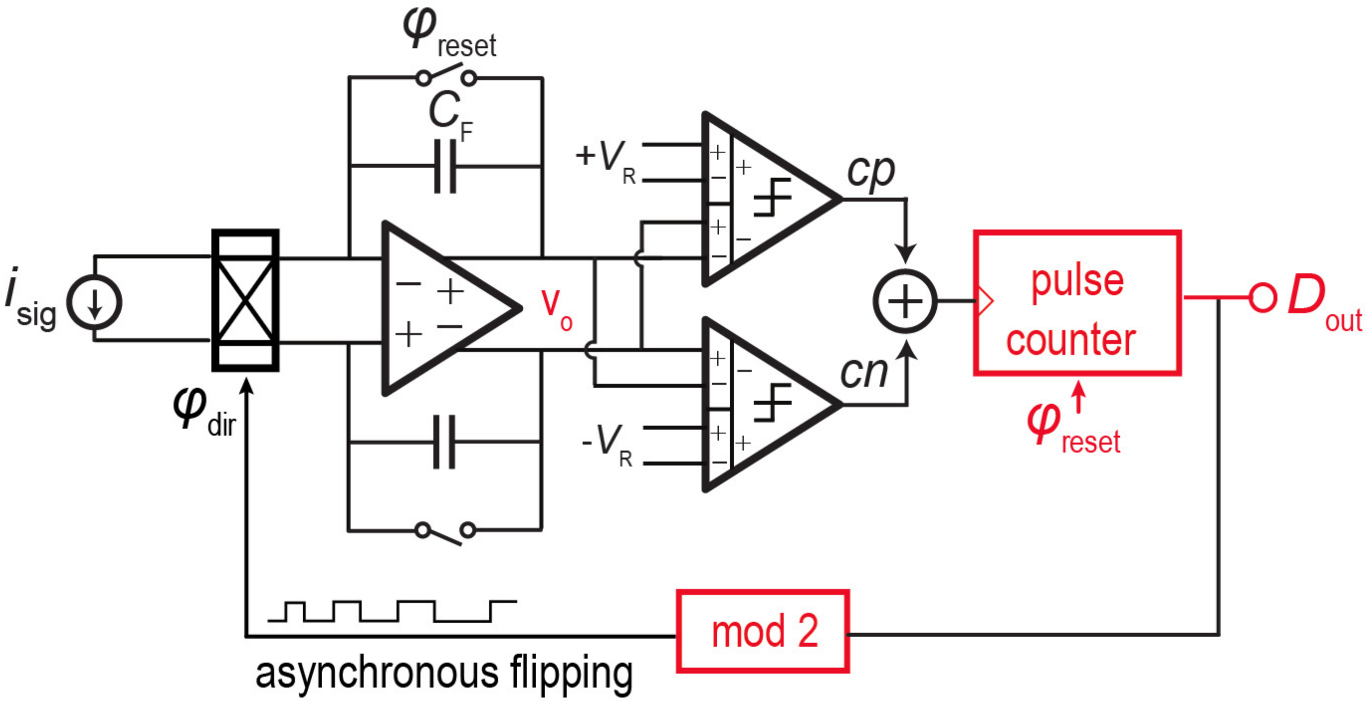
$$v_{\mathrm{o,unfolded}} \equiv \underbrace{\frac{i_{\mathrm{sig}}T_{\mathrm{p}}}{C_{\mathrm{F}}}}_{\text{Analog Input}} = (2\underbrace{D_{\mathrm{out}}}_{\text{Digital Output}} - 1)\,V_{\mathrm{R}} + \underbrace{e_{\mathrm{q}}}_{\text{Quantization Error}}$$

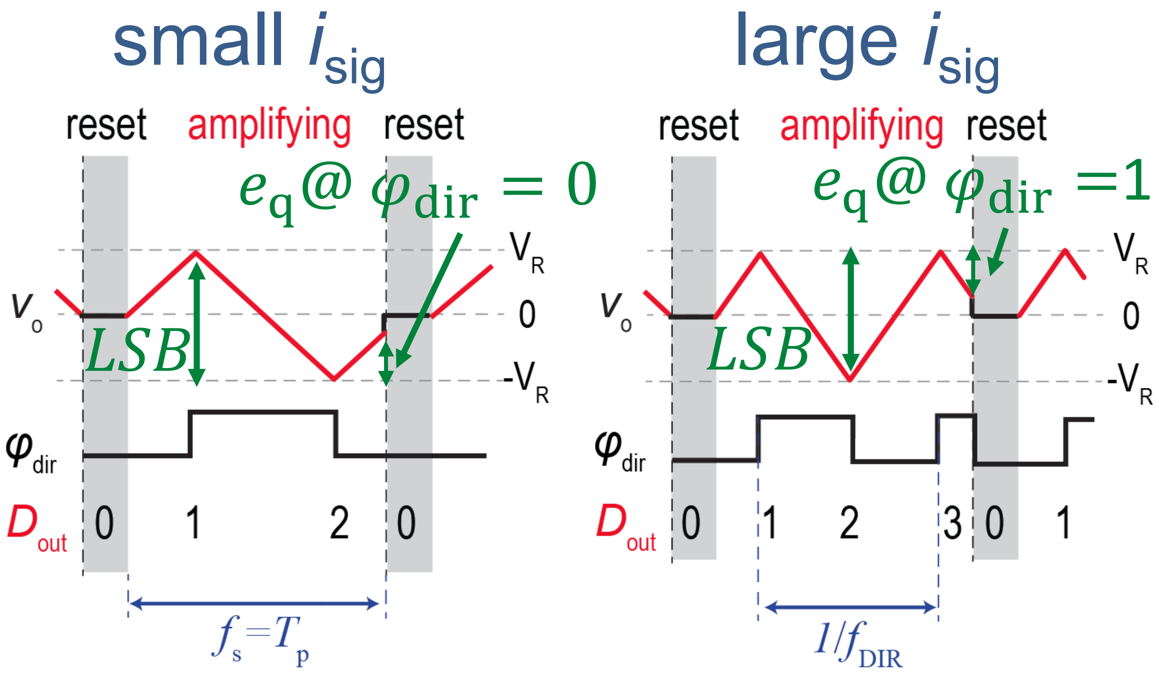
$$LSB = 2V_{\mathrm{R}}C_{\mathrm{F}}/T_{\mathrm{p}}$$

$e_q \in [-V_R, +V_R]$ w.r.t. φ_{dir}

Hourglass ADC

- The comparators work as a 1-bit quantizer

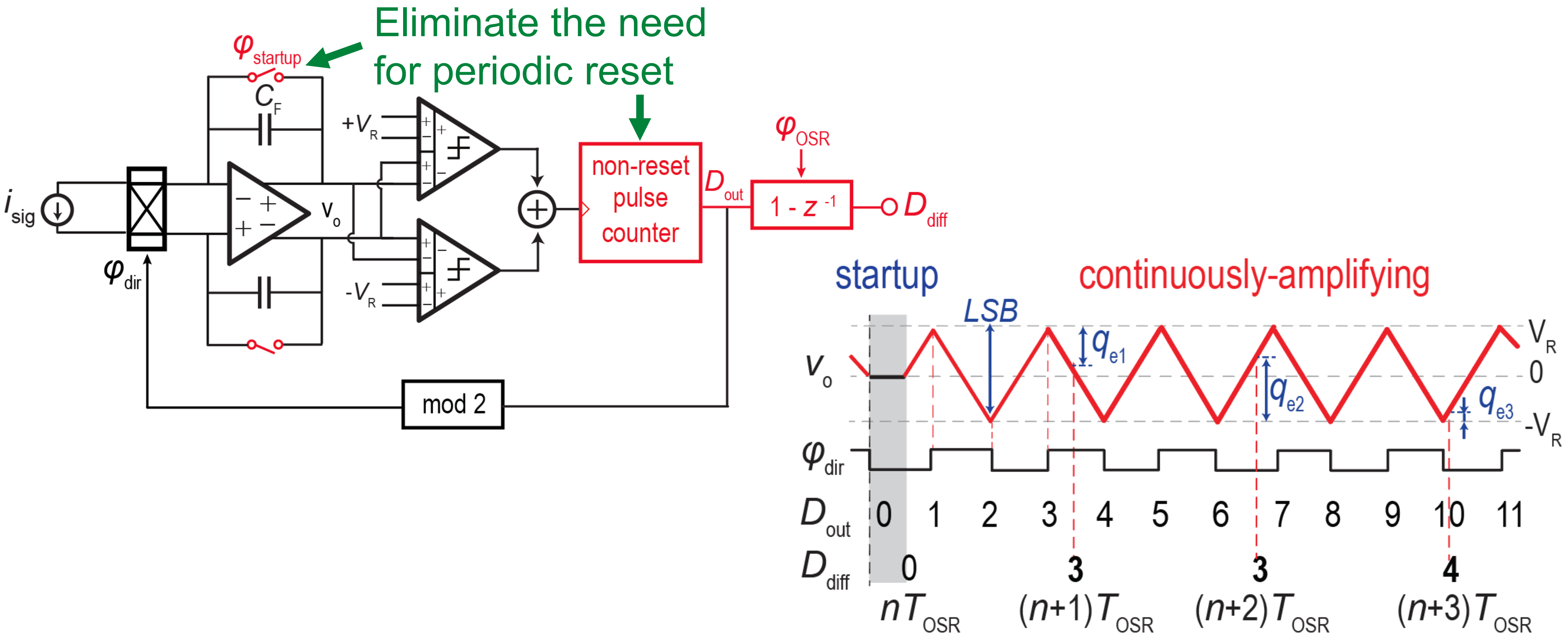




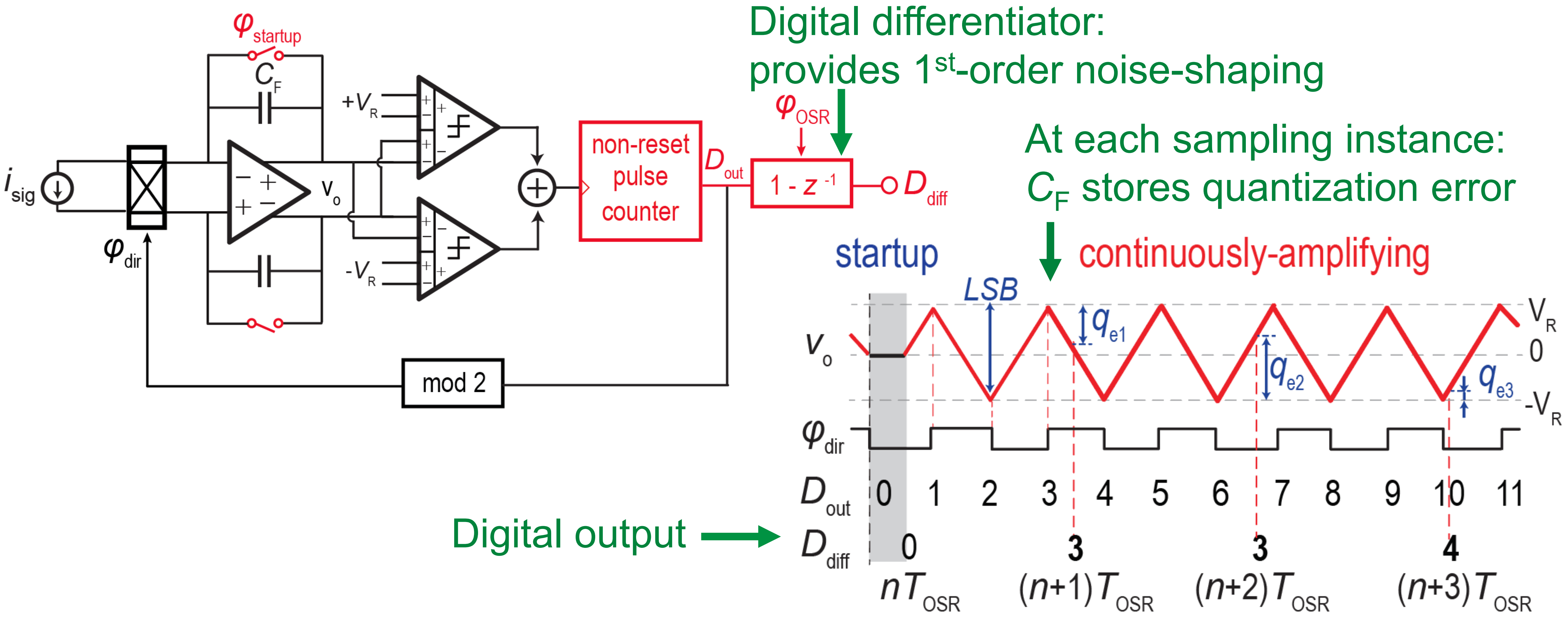
$$v_{\mathrm{o,unfolded}} \equiv \underbrace{\frac{i_{\mathrm{sig}} T_{\mathrm{p}}}{C_{\mathrm{F}}}}_{\text{Analog Input}} = (2\underbrace{D_{\mathrm{out}}}_{\text{Digital Output}} - 1)\, V_{\mathrm{R}} + \underbrace{e_{\mathrm{q}}}_{\text{Quantization Error}}$$

Question:
How to improve the resolution?
Save e_q for extending counting?

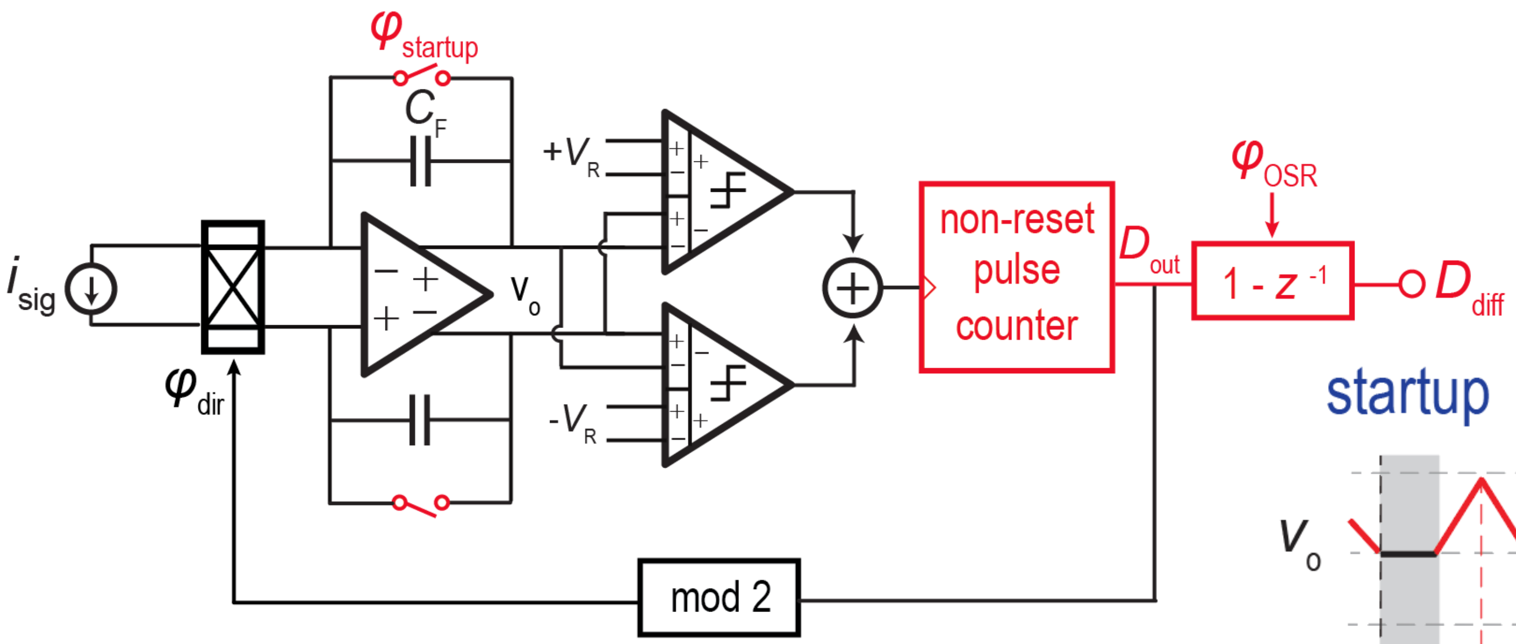
Hourglass ADC with Noise-Shaping

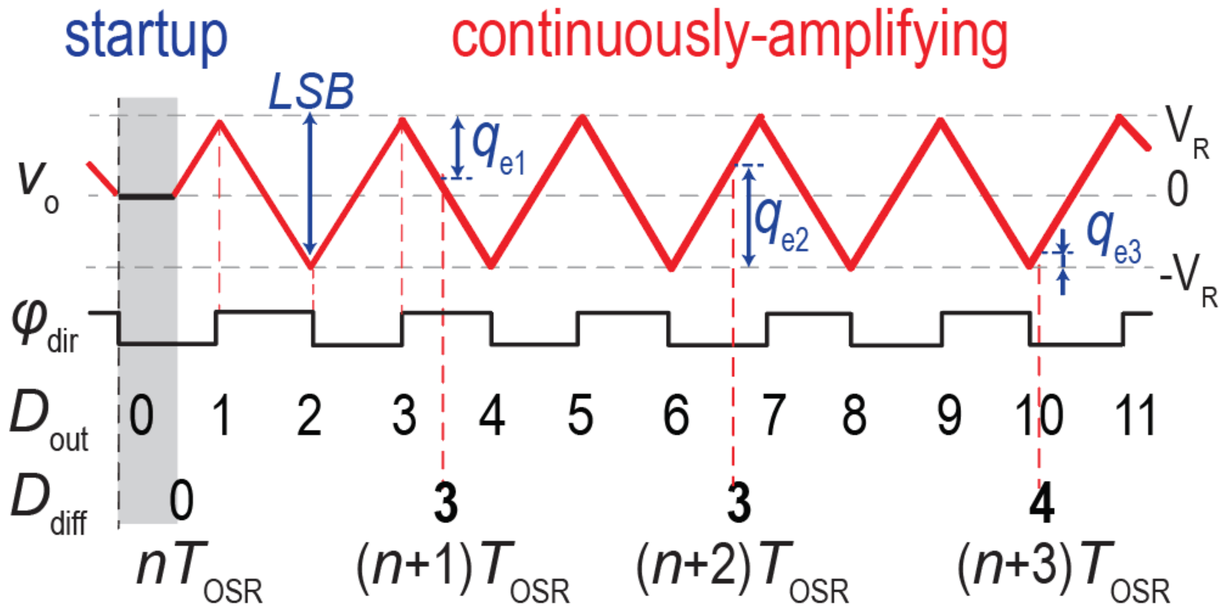


Hourglass ADC with Noise-Shaping



Hourglass ADC with Noise-Shaping



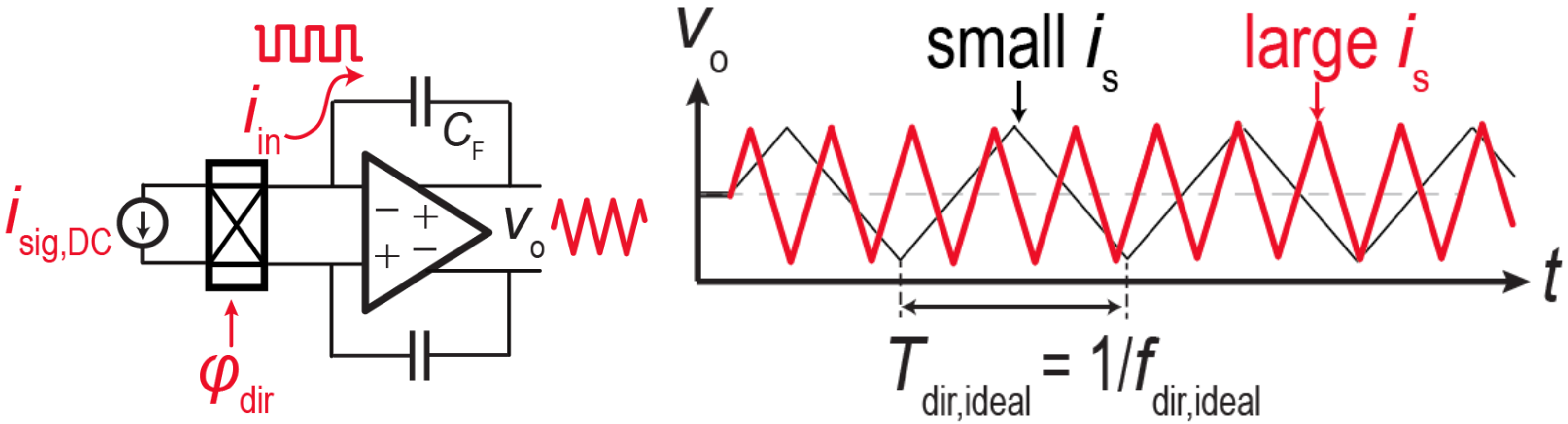


- Equivalent to a CCO-based (Current-Controlled Oscillator) ADC

The Hourglass ADC is an asynchronous 1st-order ΔΣ with improved resolution.

Linearity in Hourglass ADC

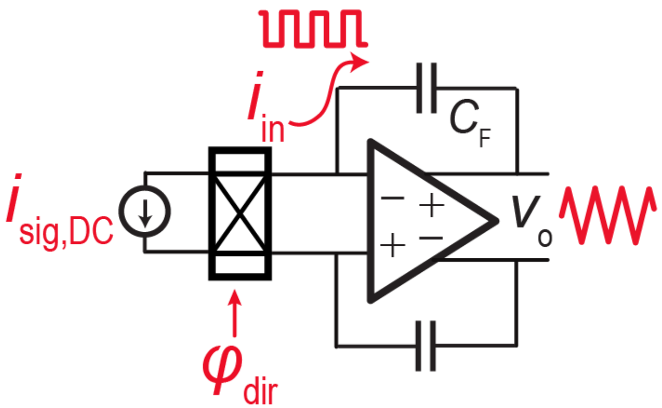
- Ideal I_{sig}-to-$f_{\varphi,dir}$ behavior

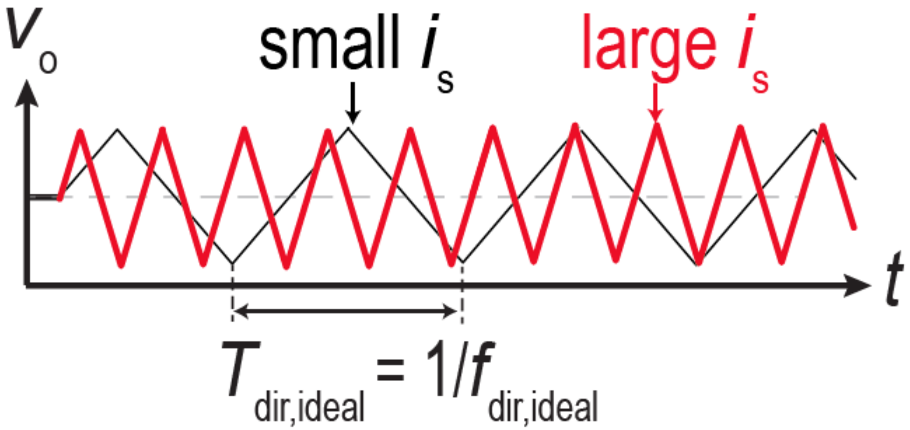


$$f_{\mathrm{dir,ideal}}(i_s, C_F) = \frac{i_{sig}}{4V_R C_F}$$

Linearity in Hourglass ADC

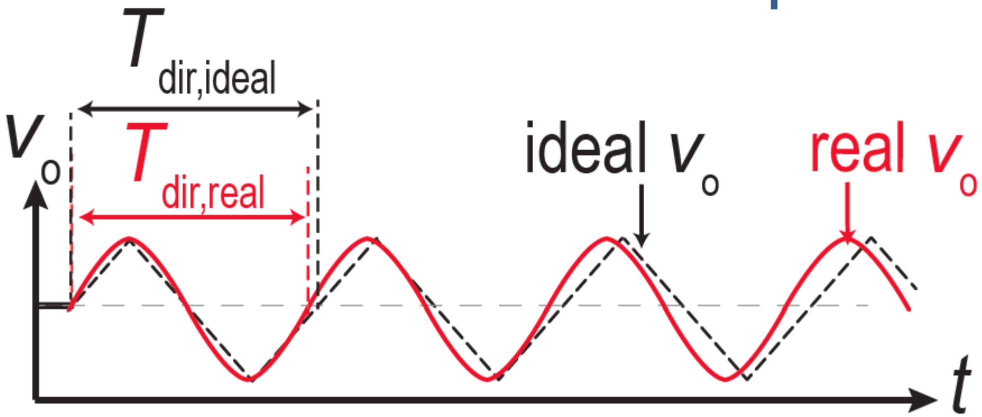
- Ideal I_{sig}-to-$f_{\varphi,dir}$ behavior

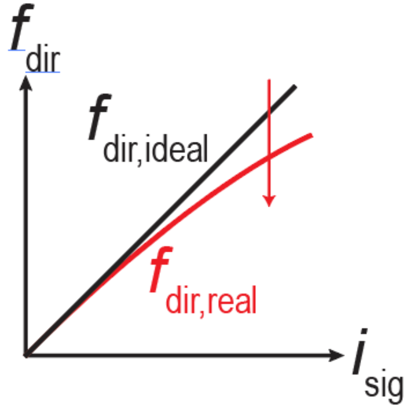




$$f_{\mathrm{dir,ideal}}(i_\mathrm{s}, C_\mathrm{F}) = \frac{i_{\mathrm{sig}}}{4V_\mathrm{R}C_\mathrm{F}}$$

- *I*-to-*F* conversion compressed with a non-ideal OPAMP



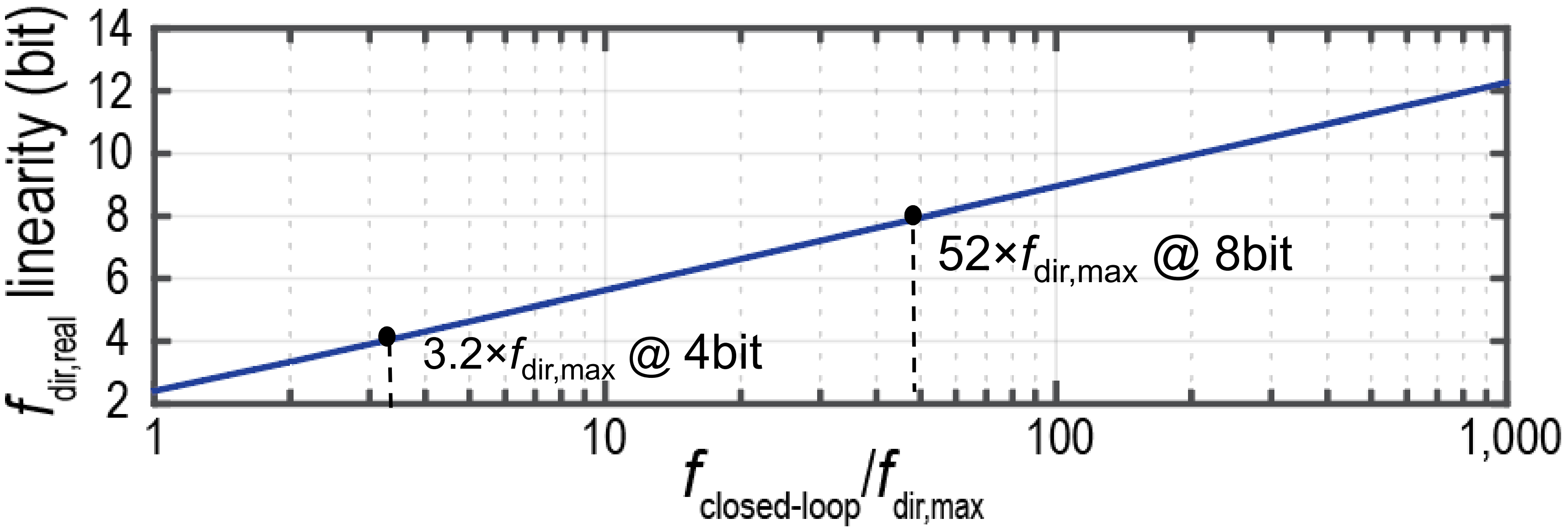


$$f_{\mathrm{dir,real}}(i_\mathrm{s}, C_\mathrm{F}, BW_{\mathrm{loop}}, A_{\mathrm{loop}})$$

The linearity of the *I*-to-*F* conversion in an Hourglass ADC is well-defined.

Linearity Calibration in Hourglass ADC

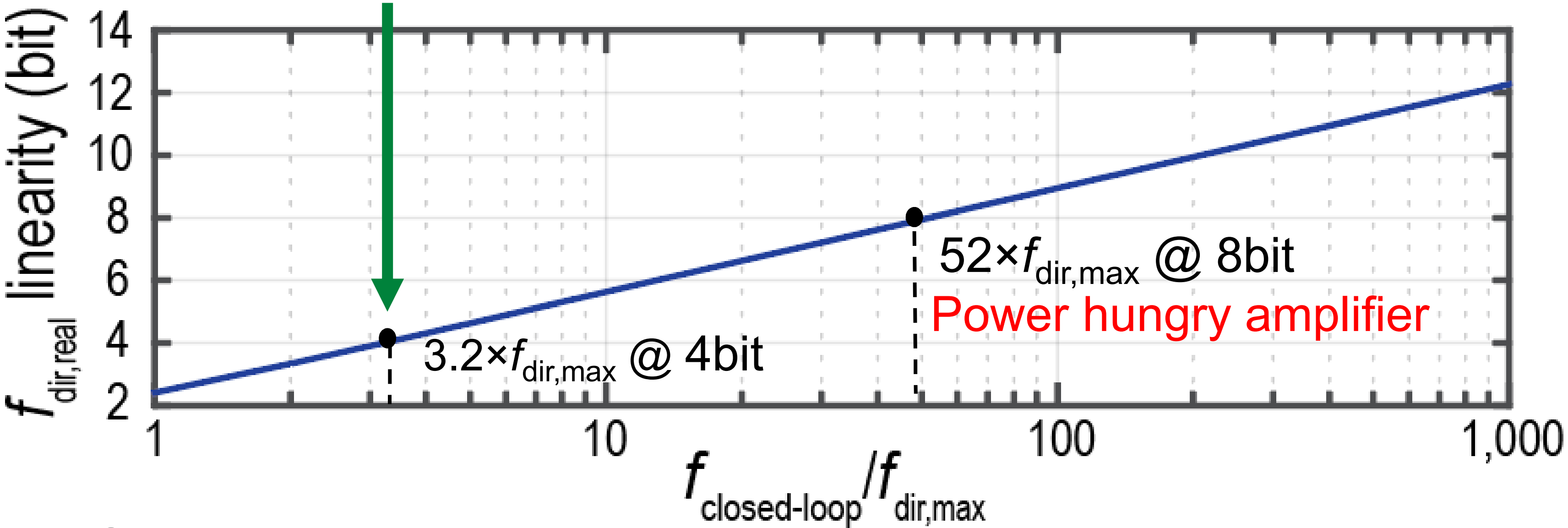
- BW vs. Linearity



Linearity Calibration in Hourglass ADC

- BW vs. Linearity

This design: $3.2\times f_{dir,max}$ w/ linear compensation
@ 16x power reduction compared to the 8-b linearity case



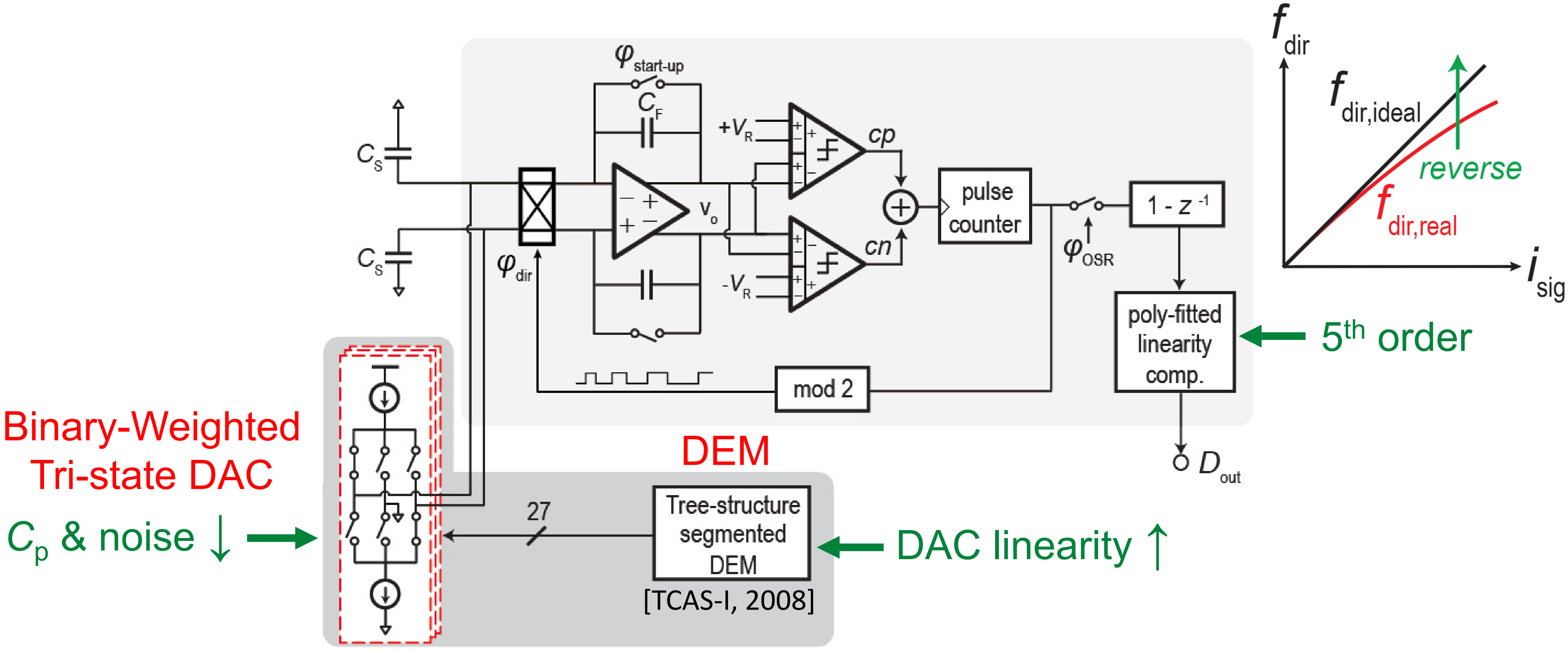
<u>Calibration</u>

- Foreground characterize the *I*-to-*F* curve: BW_{loop} and A_{loop}
- Increase power efficiency using a lower BW OPAMP

The foreground calibration improves the Hourglass ADC energy efficiency.

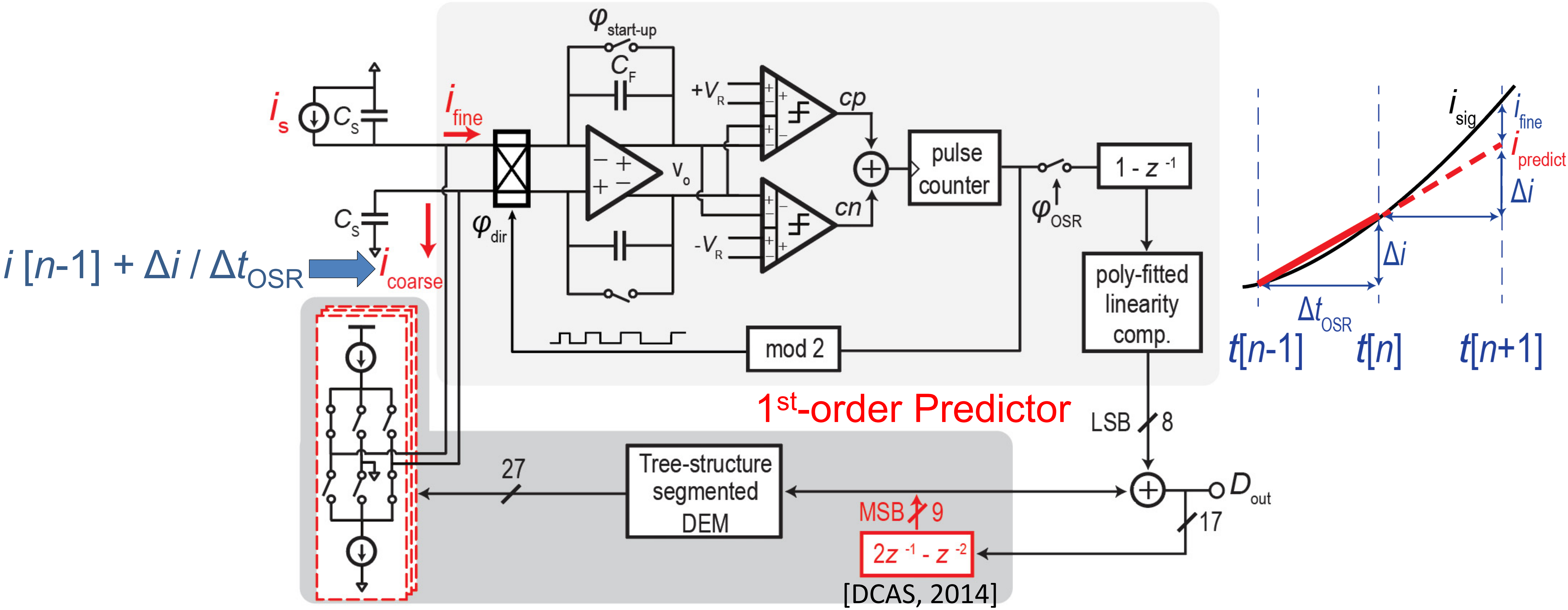
Linearity Calibration in Hourglass ADC

- Use an I-DAC to measure *I*-to-*F* curve and poly-fit the non-linearity



Closed-Loop Hourglass ADC

- The I-DAC subtracts i_s by linear extrapolating the input at f_{OSR}



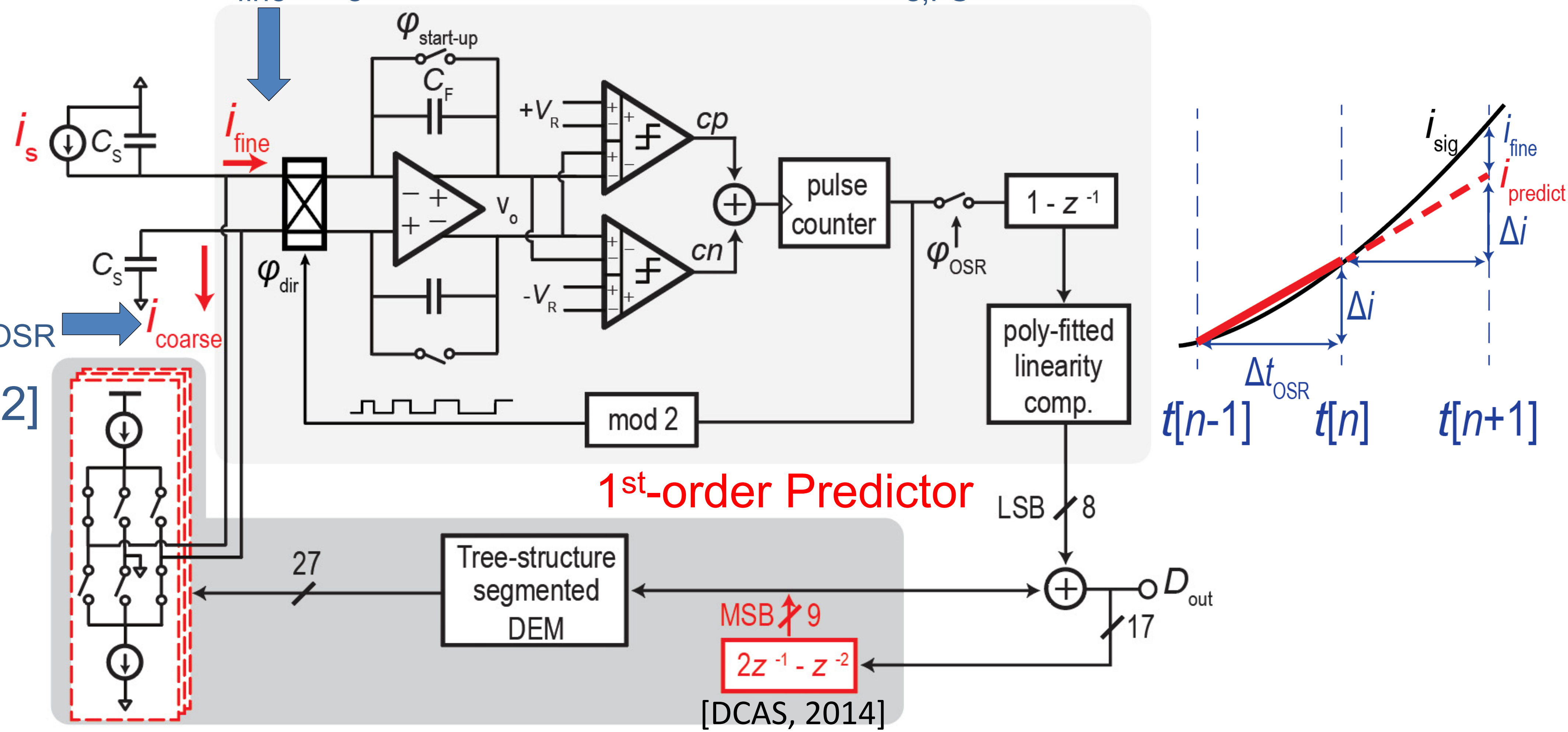
Closed-Loop Hourglass ADC

- The I-DAC subtracts i_s by linear extrapolating the input at f_{OSR}

$i_{fine} = i_s[n] - \{2i[n-1] - i[n-2]\} < i_{s,FS}/2^9$ with $OSR > 71$

$i[n-1] + \Delta i / \Delta t_{OSR}$

$= 2i[n-1] - i[n-2]$

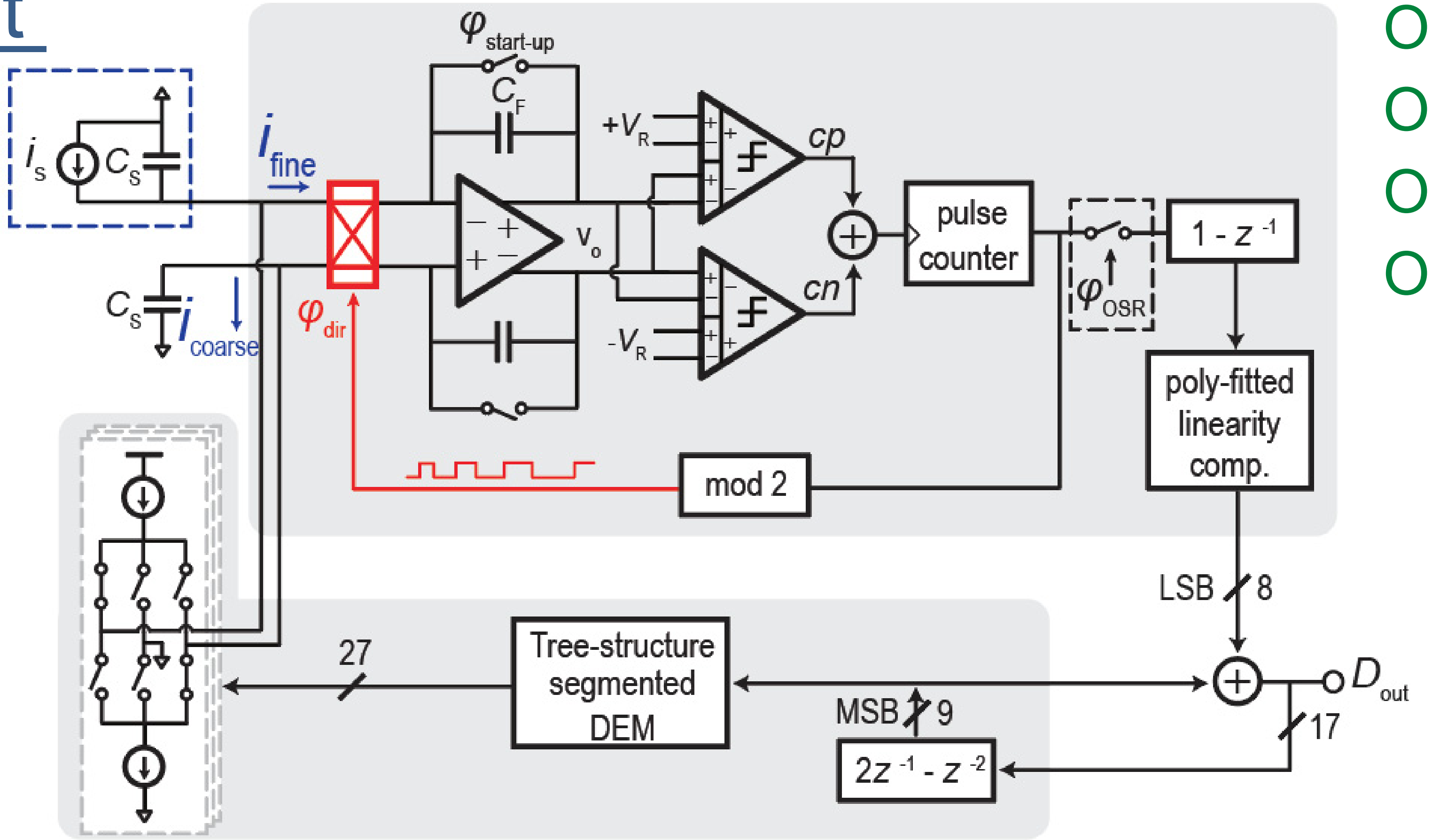


System Overview

Input Current

<1pA to 10μA

Hourglass ADC

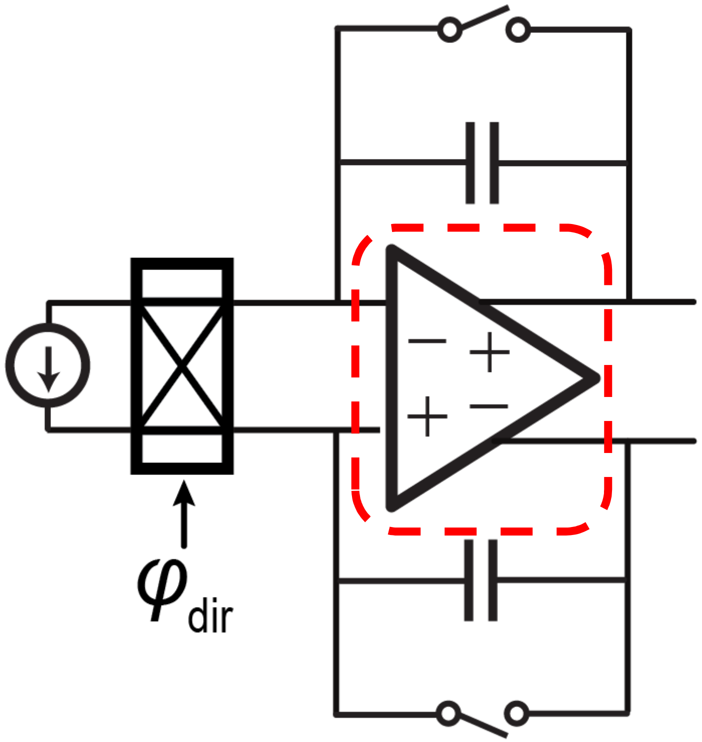


- High DR
- Async. quantization
- Noise-shaping
- High linearity

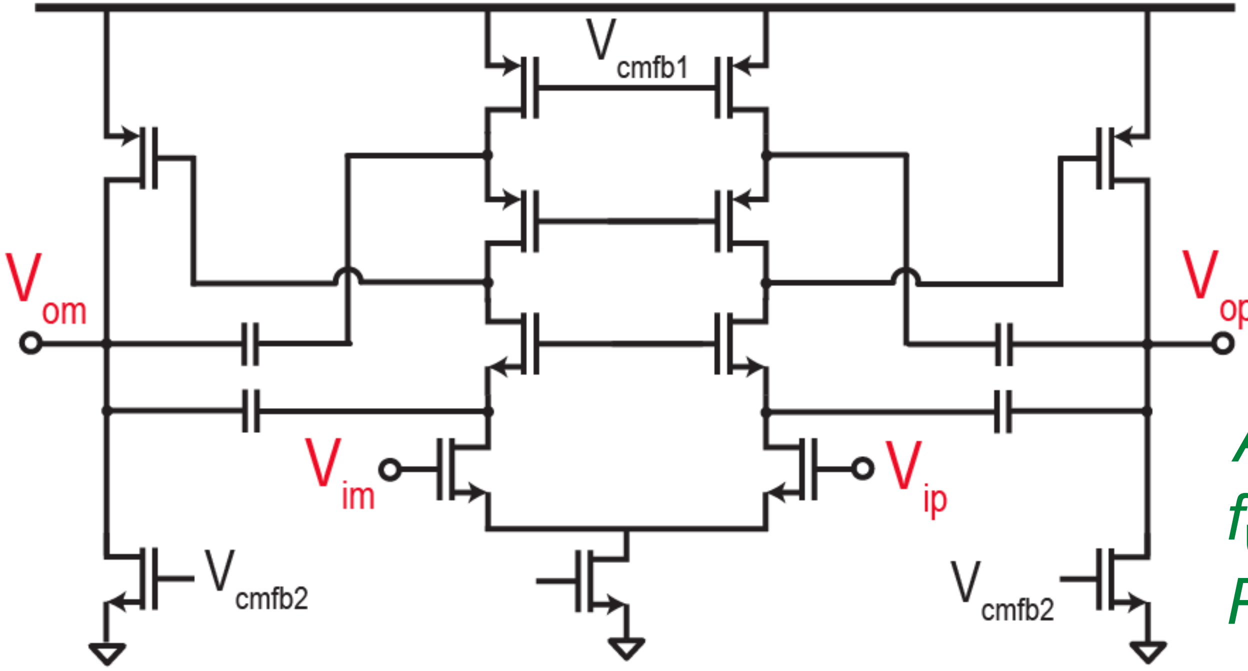
Predictive DAC

- Coarse prediction

C-TIA with Hourglass Switch



Dual Cascode-Compensated Amplifier [TCAS-I, 2004]

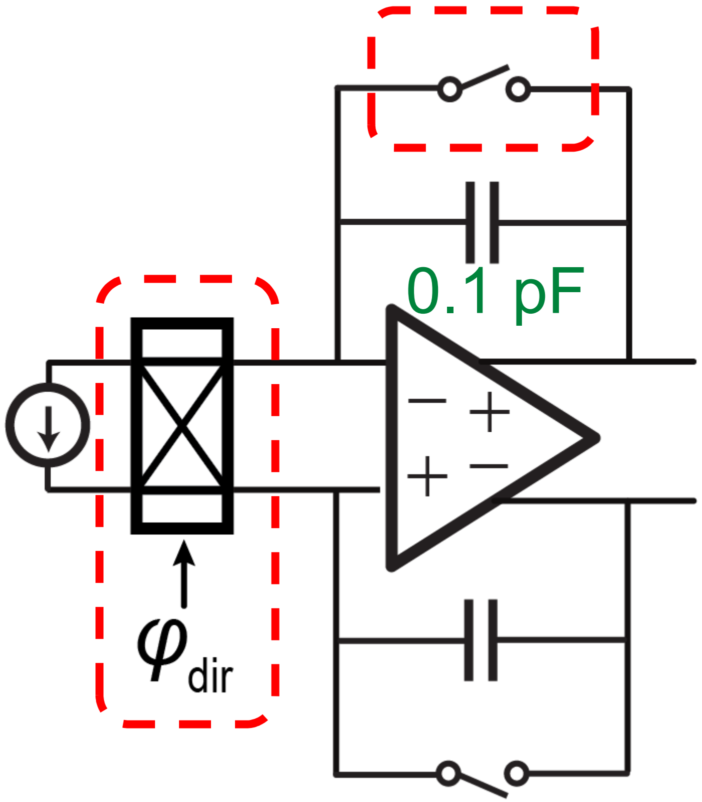


A_{DC} = 99dB
f_{UGB} = 26MHz
Pwr = 180µW

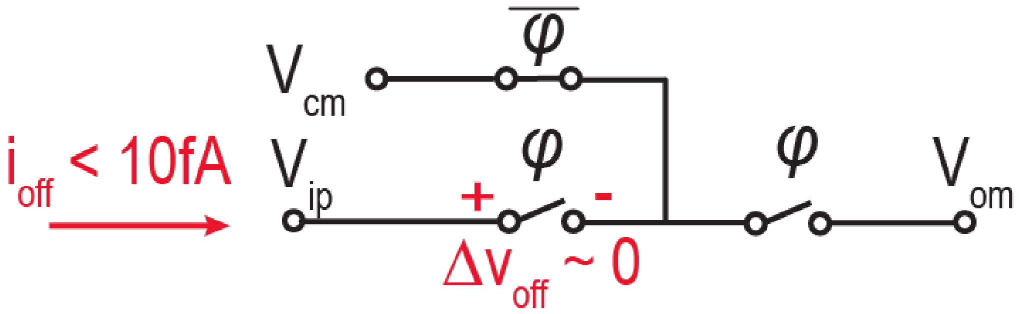
Benefit:

- Increase f_{p2} by $g_m R_o$
- Reduce C_c by 3-4×
- Improve power efficiency

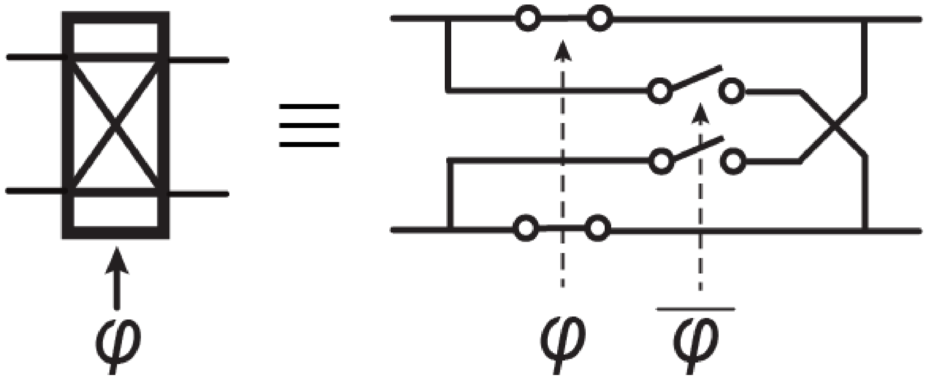
C-TIA with Hourglass Switch



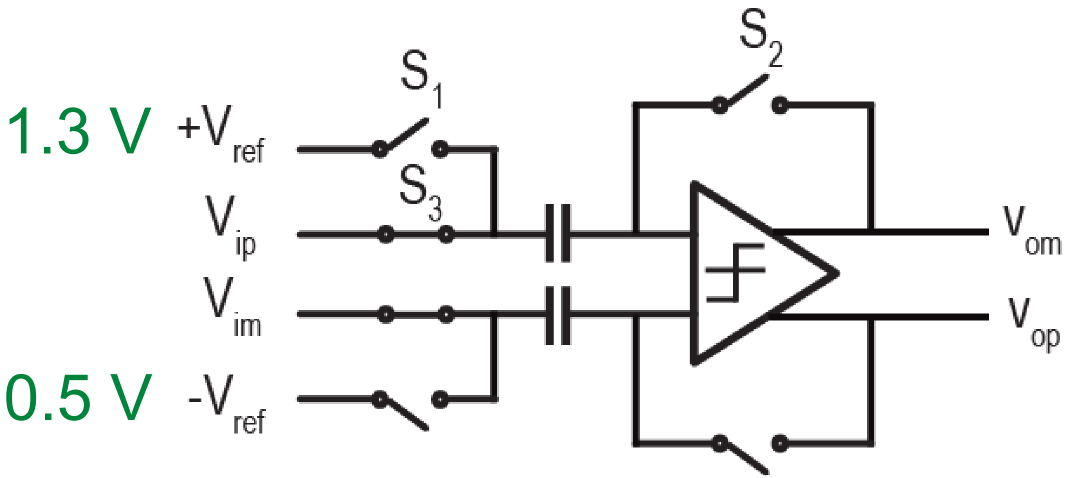
Low-Leakage Switch



Hourglass Switch

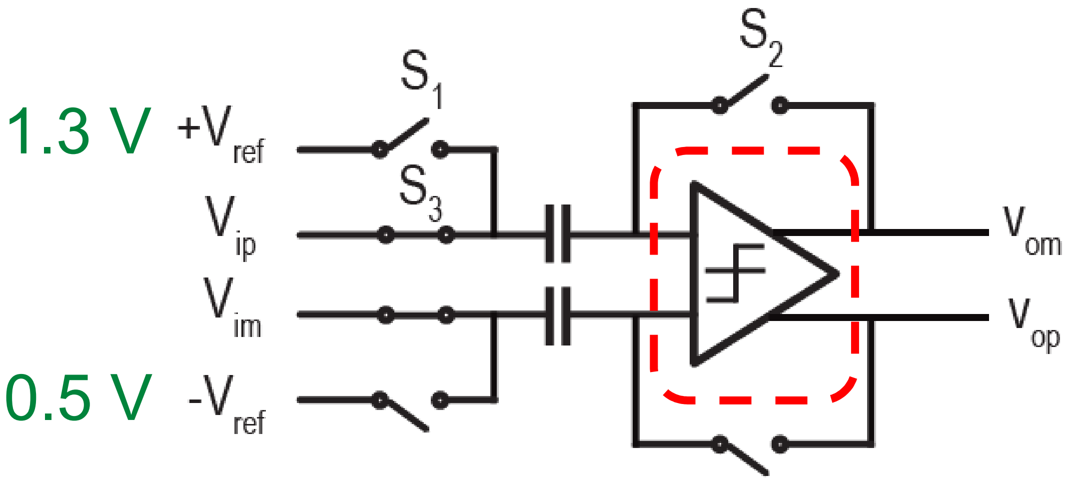


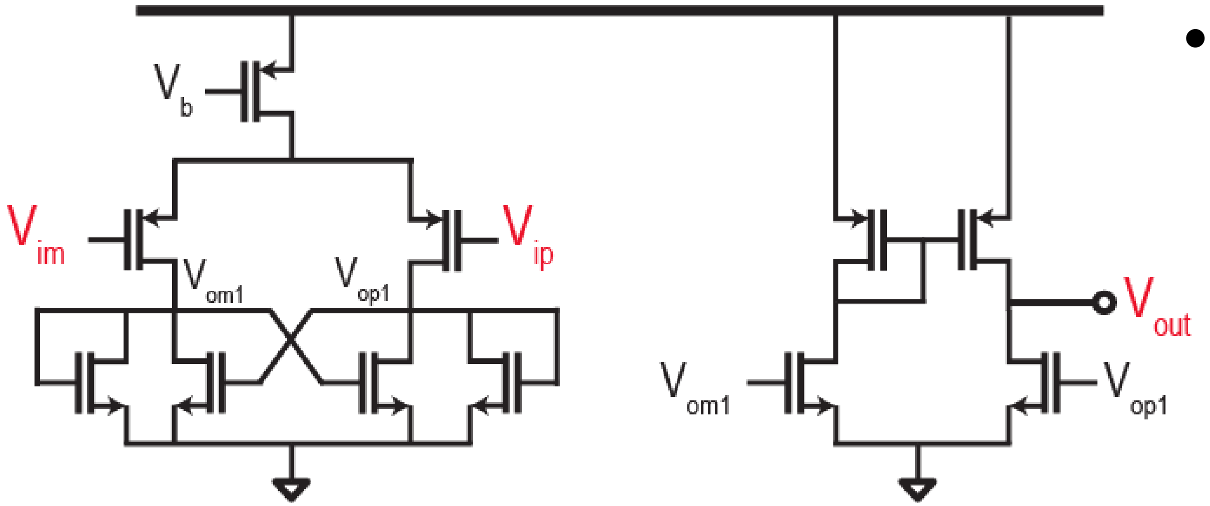
Continuous-Time Comparator



- Switched-capacitor sampling:
  - Sample at start-up
  - Store both V_R and V_{os}

Continuous-Time Comparator

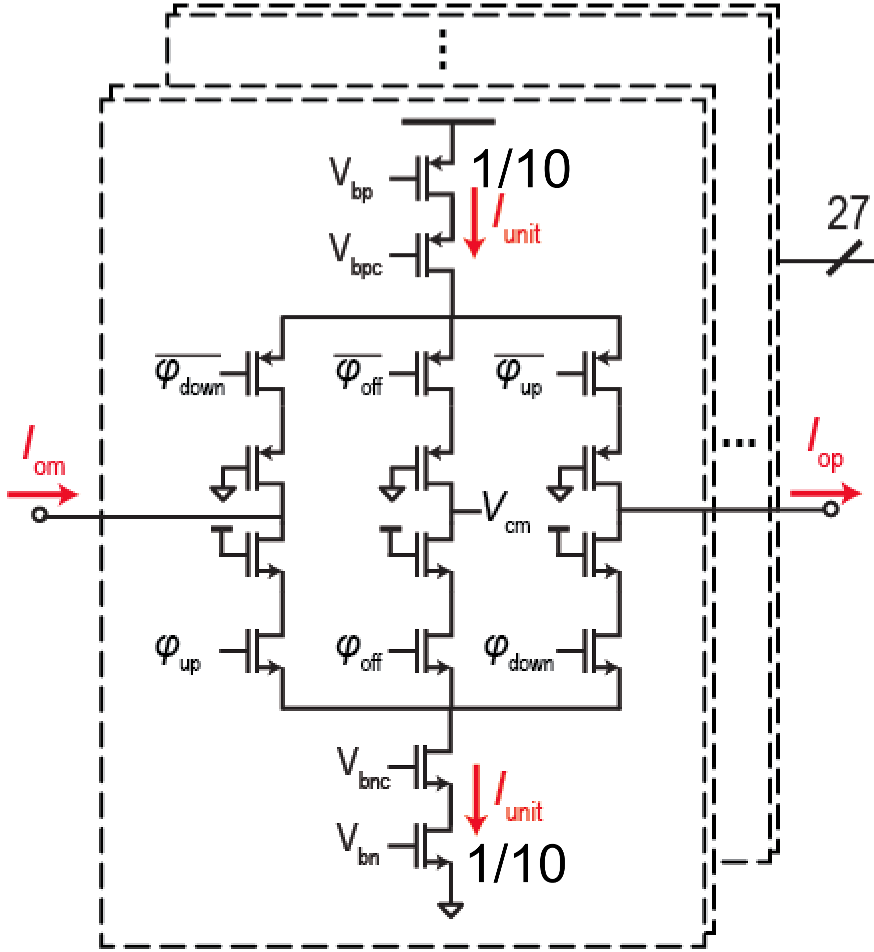




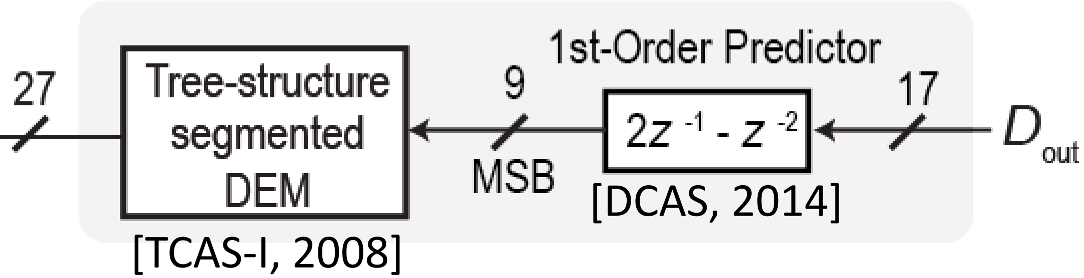
- Switched-capacitor sampling:
  - Sample at start-up
  - Store both V_R and V_{os}
- Pre-amp + dynamic amp:
  - Reduce propagation delay

Feedback Loop

9-bit Binary-Weighted I-DAC



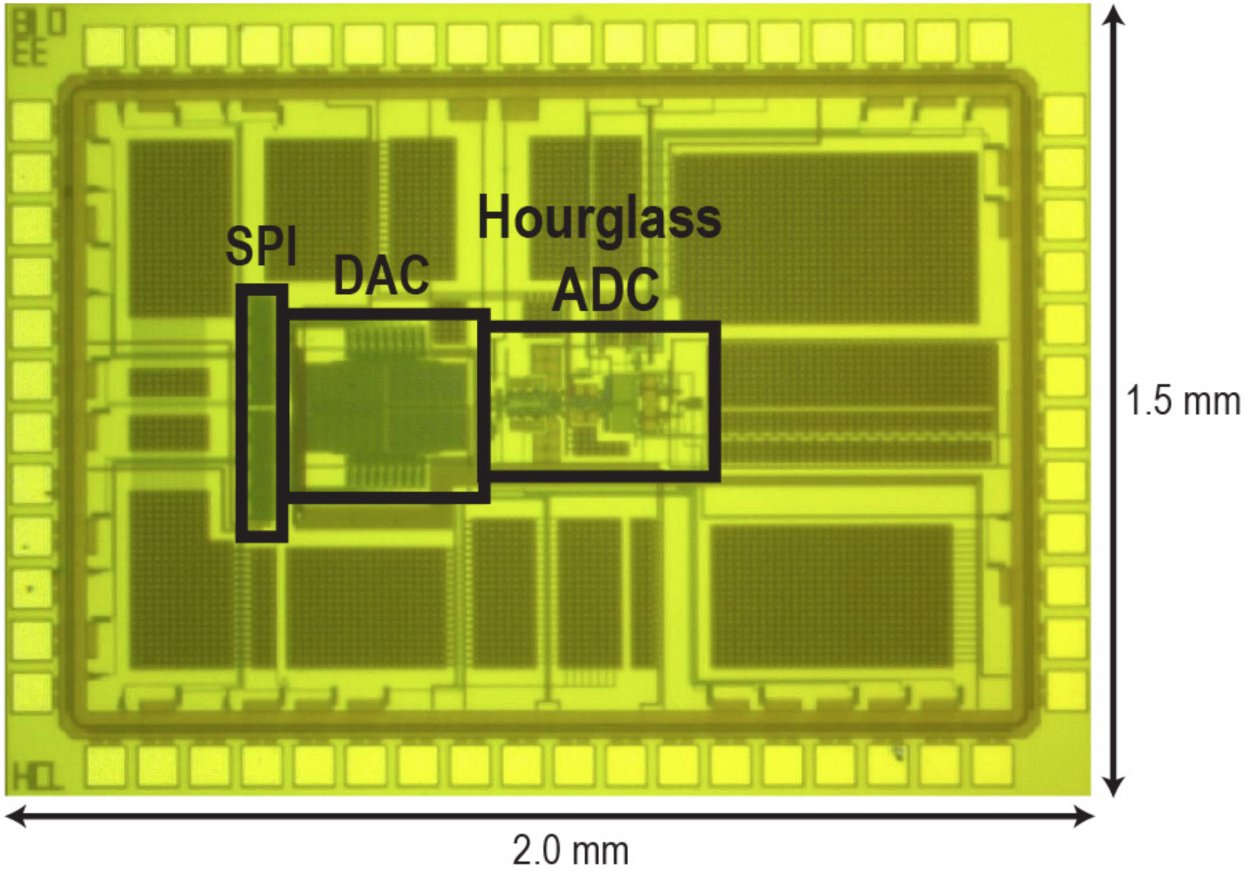
Digital blocks in FPGA



- Biasing: g_m/I_D ~ 4, thermal noise ↓
- Large size: matching ↑ & flicker noise ↓
- Cascoded tail current: R_{out} ↑

Die Photo

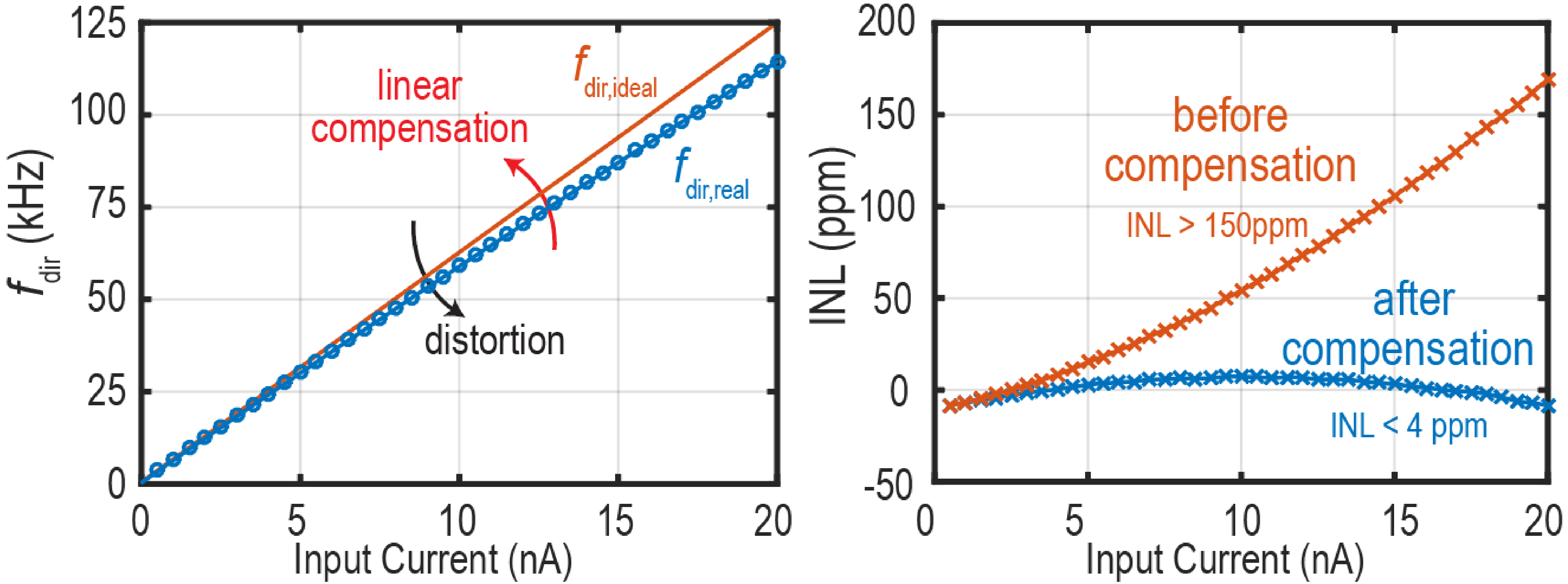
TSMC 180nm CMOS process



Core area ~$0.5mm^2$

Measurement Results

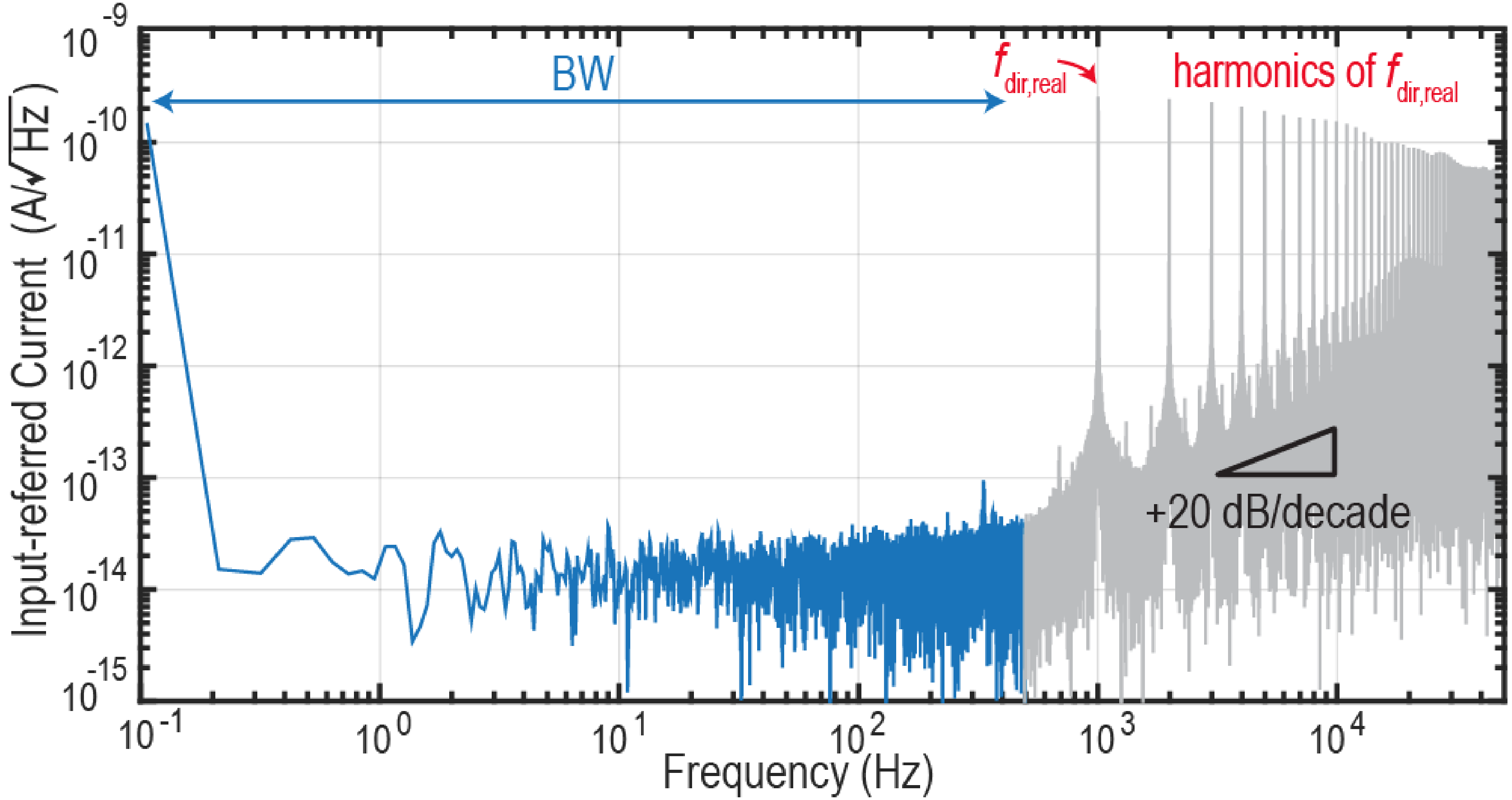
- Hourglass ADC with DAC off



The linearity of the Hourglass ADC is improved by >37×.

Measurement Results

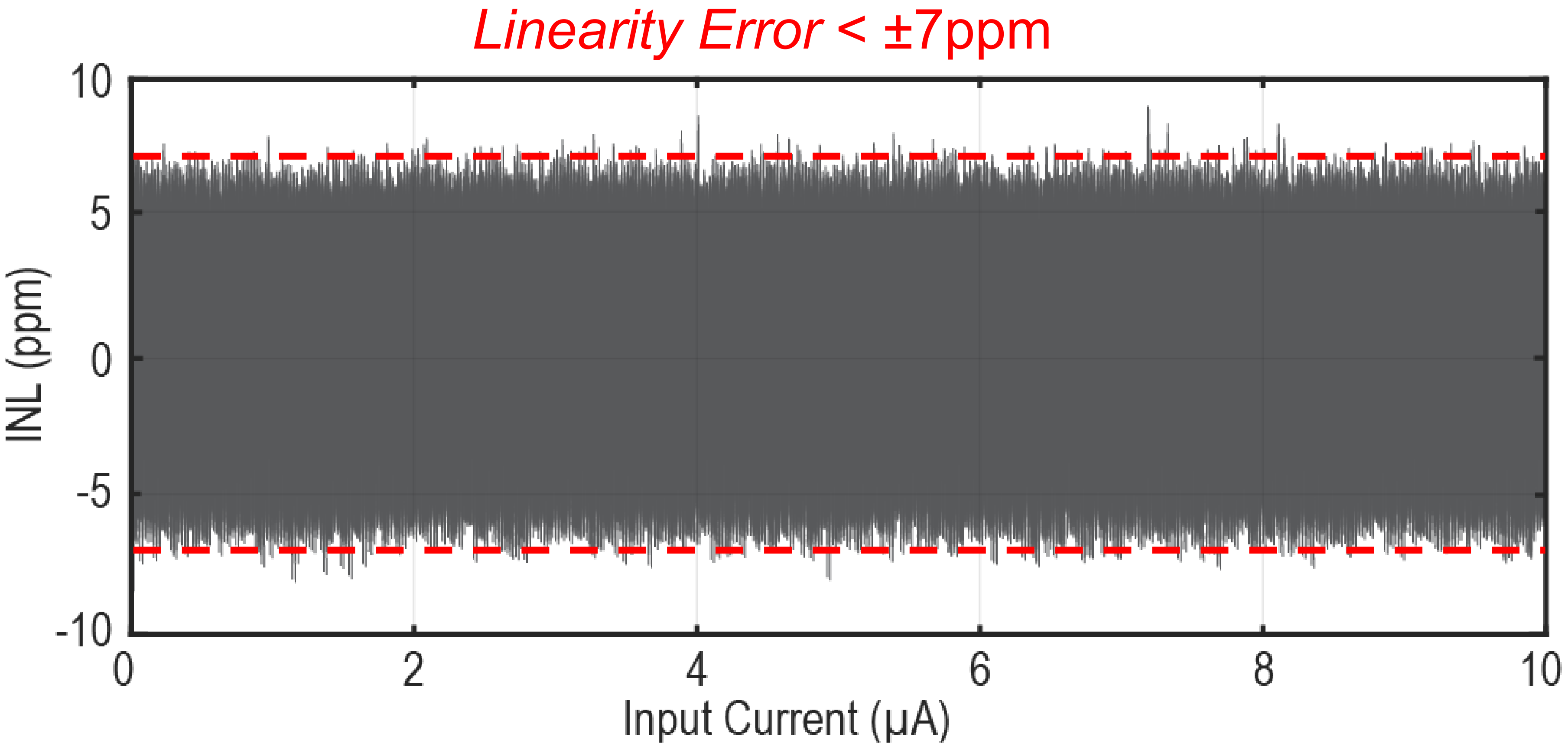
- Hourglass ADC with DAC off



The input-referred noise in the Hourglass ADC is < 30fA/√Hz.

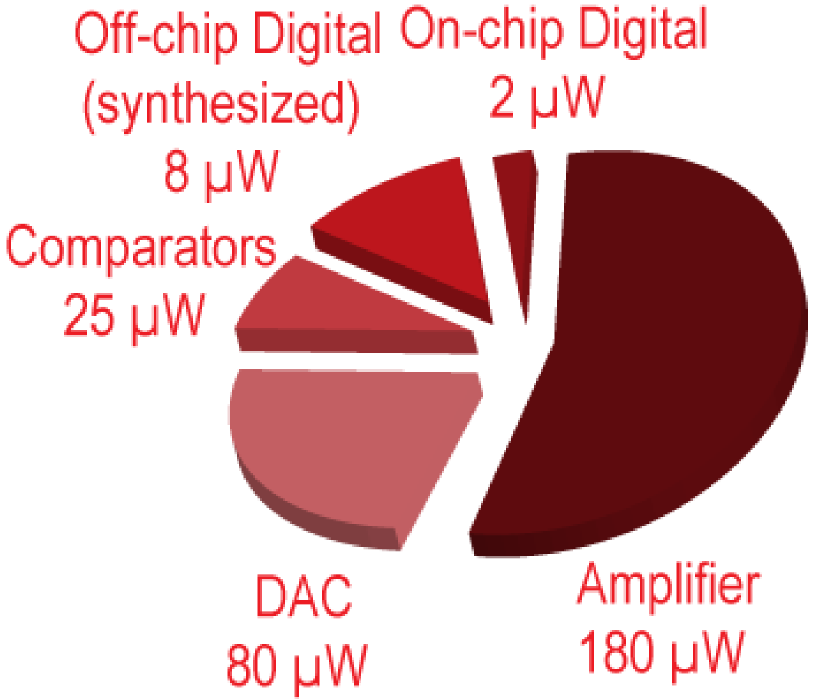
Measurement Results

- Hourglass ADC with DAC on



The linearity of the entire current-measurement front-end is < ±7ppm.

Power Breakdown



The total power consumption is 295 µW.

Summary & Comparison

	TBioCAS 07	TBioCAS 08	TBioCAS 15	JSSC 15	TBioCAS 16	TBioCAS 17	**This Work**
Architecture	SDM	SDM	I-to-F	SDM	SDM	SDM	**A-SDM**
Process [μm]	0.5	0.5	0.18	0.18	0.5	0.35	**0.18**
Power [μW]	80	60	5,220	80	240	16.8	**295**
Min Input	100 fA	12 pA	204 fA	1 nA	100 fA	100 pA	**100 fA**
Max Input	1 μA	430 nA	11.6 μA	4 μA	16 μA	3 μA	**10 μA**
Conversion time for Min Input [ms]	8,330	10,000	250	400	1,000	4	**400**
Normalized conversion time for 1nA [ms]	838	120	0.1	400	1	0.4	**0.04**
Max Linearity Error	3.9 nA	3.0 nA	1.16 μA	0.9 nA	1.6 nA	0.1 nA	**70 pA**
Dynamic Range @ BW [dB]	140 @ <0.1Hz	91 @ <0.1Hz	155 @ 1.4Hz	72 @ 2.5Hz	164 @ 1.0Hz	88.9 @ 1 kHz	**100 @ 1.8kHz 120 @ 180Hz 140 @ 18Hz 160 @ 1.8Hz**
$FOM_{Schreier}$ [dB]	172	132	181	103	183	158	**167 @ 1.8kHz 177 @ 180Hz 187 @ 18Hz 197 @ 1.8Hz**

$$FOM_{Schreier}\ (dB) = DR(dB) + 10\log(1/2/T_{conv}/P)$$

Summary & Comparison

DR = 160 dB

	TBioCAS 07	TBioCAS 08	TBioCAS 15	JSSC 15	TBioCAS 16	TBioCAS 17	**This Work**
Architecture	SDM	SDM	I-to-F	SDM	SDM	SDM	**A-SDM**
Process [μm]	0.5	0.5	0.18	0.18	0.5	0.35	**0.18**
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Conversion time for Min Input [ms]	8,330	10,000	250	400	1,000	4	**400**
Normalized conversion time for 1nA [ms]	838	120	0.1	400	1	0.4	**0.04**
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Dynamic Range @ BW [dB]	140 @ <0.1Hz	91 @ <0.1Hz	155 @ 1.4Hz	72 @ 2.5Hz	164 @ 1.0Hz	88.9 @ 1 kHz	**100 @ 1.8kHz 120 @ 180Hz 140 @ 18Hz 160 @ 1.8Hz**
$FOM_{Schreier}$ [dB]	172	132	181	103	183	158	**167 @ 1.8kHz 177 @ 180Hz 187 @ 18Hz 197 @ 1.8Hz**

$$FOM_{Schreier}\,(dB) = DR(dB) + 10\log(1/2/T_{conv}/P)$$

Summary & Comparison

T_{conv} 2.5× faster

	TBioCAS 07	TBioCAS 08	TBioCAS 15	JSSC 15	TBioCAS 16	TBioCAS 17	**This Work**
Architecture	SDM	SDM	I-to-F	SDM	SDM	SDM	**A-SDM**
Process [μm]	0.5	0.5	0.18	0.18	0.5	0.35	**0.18**
Power [μW]	80	60	5,220	80	240	16.8	**295**
Min Input	100 fA	12 pA	204 fA	1 nA	100 fA	100 pA	**100 fA**
Max Input	1 μA	430 nA	11.6 μA	4 μA	16 μA	3 μA	**10 μA**
Conversion time for Min Input [ms]	8,330	10,000	250	400	1,000	4	**400**
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$FOM_{Schreier}$ [dB]	172	132	181	103	183	158	**167 @ 1.8kHz 177 @ 180Hz 187 @ 18Hz 197 @ 1.8Hz**

$$FOM_{Schreier}\,(dB) = DR(dB) + 10\log(1/2/T_{conv}/P)$$

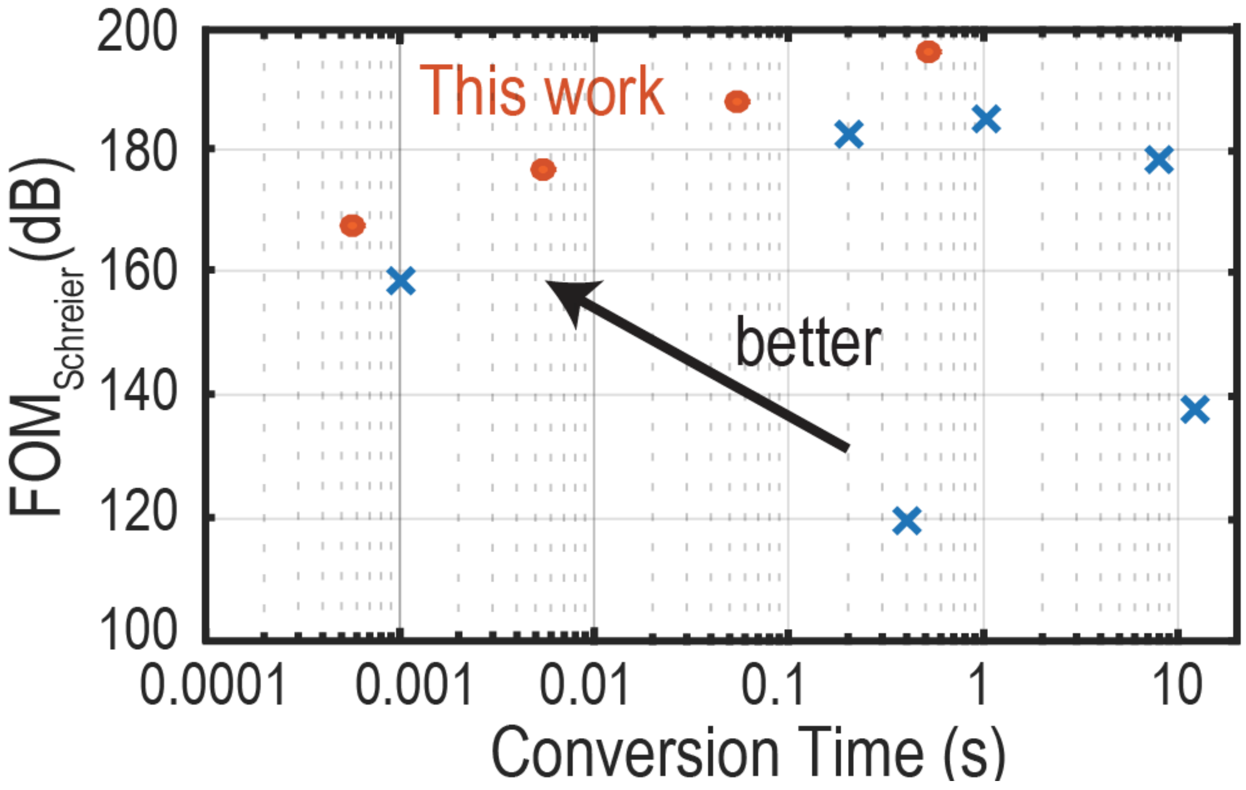
Summary & Comparison

FOM = 197 dB

	TBioCAS 07	TBioCAS 08	TBioCAS 15	JSSC 15	TBioCAS 16	TBioCAS 17	**This Work**
Architecture	SDM	SDM	I-to-F	SDM	SDM	SDM	**A-SDM**
Process [µm]	0.5	0.5	0.18	0.18	0.5	0.35	**0.18**
Power [µW]	80	60	5,220	80	240	16.8	**295**
Min Input	100 fA	12 pA	204 fA	1 nA	100 fA	100 pA	**100 fA**
Max Input	1 µA	430 nA	11.6 µA	4 µA	16 µA	3 µA	**10 µA**
Conversion time for Min Input [ms]	8,330	10,000	250	400	1,000	4	**400**
Normalized conversion time for 1nA [ms]	838	120	0.1	400	1	0.4	**0.04**
Max Linearity Error	3.9 nA	3.0 nA	1.16 µA	0.9 nA	1.6 nA	0.1 nA	**70 pA**
Dynamic Range @ BW [dB]	140 @ <0.1Hz	91 @ <0.1Hz	155 @ 1.4Hz	72 @ 2.5Hz	164 @ 1.0Hz	88.9 @ 1 kHz	**100 @ 1.8kHz 120 @ 180Hz 140 @ 18Hz 160 @ 1.8Hz**
$FOM_{Schreier}$ [dB]	172	132	181	103	183	158	**167 @ 1.8kHz 177 @ 180Hz 187 @ 18Hz 197 @ 1.8Hz**

$$FOM_{Schreier}\,(dB) = DR(dB) + 10\log(1/2/T_{conv}/P)$$

Summary & Comparison



$$FOM_{Schreier}\,(dB) = DR(dB) + 10\log(1/2/T_{conv}/P)$$

Conclusions

- The current measurement front-end enables precise wide dynamic range for bio-sensing applications
- Key challenges: **dynamic range** and **linearity**
- To address this, we:
  - Designed an Hourglass ADC to increase DR and decrease quantization noise
  - Designed a DAC with a 1st-order predictor to further increase DR and improve the front-end power efficiency
  - Used DEM and linearity compensation to improve linearity
- Result:
  - A current measurement front-end with **160dB DR, 7ppm INL, and 197dB FOM**