A 9.7-nT_{rms}, 704-ms Magnetic Biosensor Front-End for Detecting Magneto-Relaxation

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Abstract—This article reports a low-noise magnetic sensor front-end with an 18-bit Zoom ADC for detecting temporal magnetic nanoparticle (MNP) relaxation. Techniques such as dynamic element matching (DEM) and magnetoresistive correlated double sampling (MRCDS) are proposed to remove the sensor and analog front-end (AFE) 1/f noise while a fast-settling Miller compensation (FSMC) technique is proposed to reduce the amplifier power. Collectively, these result in state-of-the-art input-referred noise performance (9.7 nT_{rms}) and a figure-of-merit (FoM) that is 6.6× and 210× better than previously reported magnetic sensor and relaxation-based AFEs, respectively. A relaxation-based magnetic immunoassay (MIA) was performed to demonstrate the concept. This design is implemented in a 0.18- μ m CMOS process and consumes 4.32 mW from a 1.8-V supply.

Index Terms— Magnetic immunoassay (MIA), magnetic sensor, relaxometry, sensor analog front-end (AFE), Zoom ADC.

I. INTRODUCTION

OINT-OF-CARE (PoC) biomolecular testing is gaining momentum worldwide for rapidly diagnosing disease and remotely monitoring disease progression [1]-[3]. Such tests need compact, fast turn-around time, and accurate biosensors. Most PoC biosensors today are either colorimetric lateral flow immunoassays based on an enzyme-linked immunosorbent assay (ELISA) or electrochemical sensors with enzymatic assays (e.g., glucometers) [4], [5]. While extremely prevalent, lateral flow assays have low sensitivity and are only semi-qualitative, typically relegating them to applications with binary outcomes (e.g., pregnancy and strep throat) and high abundance biomarkers [6]. On the other hand, electrochemical sensors can be extremely sensitive and compact, but often suffer from matrix effects (e.g., pH, ionic strength, and temperature) requiring sample pretreatment steps. These assays can also be sensitive to redox active interfering species [7], [8]. Thus, there remains an unmet need for highly sensitive biosensors for PoC applications.

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(3)

Fig. 1. (a) Illustration of an MIA where underlying MR sensors detect MNP labeled antigen-antibody complexes, and (b) transient response of an MR sensor in an MIA.

Magnetic sensors have been reported for high sensitivity biomolecular testing [9]-[17]. The high sensitivity is, in part, due to the sample matrix (*i.e.* urine, saliva, and blood) being devoid of a magnetic background enabling matrix-insensitive biomarker detection [18], [19]. The small size and CMOS compatibility make magnetic sensors attractive for PoC applications [20], [21]. Several types of magnetic sensors have been demonstrated, such as LC oscillator-based sensors [11], Hall-effect sensors [12], [13], and magnetoresistive (MR) sensors [14]–[17]. MR sensors were chosen for this work due to their high transduction efficiency enabling detection of nanometer-sized magnetic nanoparticles (MNPs) [19]. While the transduction method differs (e.g., spin-dependent scattering versus tunneling), all MR sensors can generically be modeled as a differential resistance proportional to the magnetic field [22].

A magnetic immunoassay (MIA), a modified form of an ELISA, is used to deploy an MR sensor for biosensing, as shown in Fig. 1(a). Initially, capture antibodies are immobilized on the sensor surface (Step 1). Next, the sample is added, and the target biomarkers bind to the capture antibodies (Step 2). Then MNP-conjugated detection antibodies are added and bind to form a sandwich structure, as shown in Step 3. Since the MNPs are superparamagnetic, they have a random orientation without an applied field and exert zero net field on the underlying sensors. Thus, the MR sensor remains at its nominal resistance, R_0 . During Step 4, an external magnetic

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Fig. 2. Prior MRX-based AFEs. (a) Liu, JSSC 2012. (b) Gambini, JSSC 2013.

field, H_A , is applied along the sensor's short axis that polarizes the MNPs generating a stray field that is proportional to the number of tethered MNPs. The sensor resistance changes to $R_0 + R_{MR} + R_{mag}$, where R_{MR} is the magnetoresistance due to H_A and R_{mag} is the magnetoresistance signal due to the stray field from the tethered MNPs. The transient sensor response, R_S , is illustrated in Fig. 1(b). Conventional magnetometry measures R_{mag} at Step 4 to quantify the number of MNPs, which is directly proportional to the number of captured biomarkers [14]–[17]. However, the large baseline to signal ratio (R_0/R_{mag}) requires the AFE to have a dynamic range (DR) of >140 dB.

To cancel the baseline, magneto-relaxometry (MRX) was proposed to detect the temporal relaxation of the tethered MNPs rather than the static magnetization [12], [13]. Instead of measuring R_{mag} superimposed on R_0 and R_{MR} during Step 4, an additional step (Step 5) is added where H_A is rapidly removed resulting in the MNPs losing their magnetization. The MNPs return to a random state via Néel and/or Brownian relaxation. Brownian relaxation rotates the whole particle via Brownian motion [23] whereas Néel relaxation uses internal domain movement [24]. Since the MNPs are immobilized by the antibodies, Néel relaxation dominates the process [25]. The MNP magnetization as a function of time [26] can be written as

$$M_{\rm N}(t) = C \cdot \ln\left(1 + \frac{t_{\rm C}}{t}\right) \tag{1}$$

where *t* is the time after removing H_A , t_C is the characteristic time that depends on the magnetization time and applied field strength, and *C* is a scaling factor dependent on the surface coverage, magnetic viscosity, and initial magnetization [27]. $M_N(t)$, in units of A/m, is proportional to the number of MNPs after considering particle-to-particle interactions and the MNP size/shape distribution [27], [28]. Therefore, by measuring the temporal relaxation signal, R_{rlx} , during Step 5, the number of tethered MNPs can be quantified. Using magnetic correlated double sampling (MCDS) where the signal at Step 5 is subtracted from the signal at Step 3, the baseline can be eliminated [13], [29]. Compared to magnetometry, MRX eliminates the baseline and relaxes the H_A uniformity requirement.

A few CMOS AFEs have been reported for MRX using Hall-effect sensors. Fig. 2(a) shows an AFE with a programmable gain amplifier (PGA) and an offset cancella-

 TABLE I

 TARGET SPECIFICATIONS OF THE MAGNETIC SENSOR AFE

	State-of-the-Art [16]	Target
Sensitivity	N/A	< 0.1 ppm
Baseline	7.09 mT	< 0.3 mT
Total Noise	49 nT _{rms}	$< 14.4 \text{ nT}_{\text{rms}}$
Readout Time	250 ms	< 1 s
Power Consumption	3.15 mW	< 5 mW

tion loop to remove the equivalent sensor R_0 baseline [12]. An off-chip high-speed ADC captures the fast relaxation signal. In [13], an incremental $\Delta \Sigma$ ADC was used to integrate R_{rlx} during the relaxation phase, as shown in Fig. 2(b). Since R_{rlx} is the largest immediately after removing H_A and decays over time, integrating R_{rlx} at the beginning of the relaxation phase captures most of the signal, while reducing the power consumption, thus achieving high efficiency. While promising, the magnetic sensor figure-of-merit (FoM), defined as Resolution² · Energy/Conversion [30], [31], for both of these designs is $32 \times$ worse than state-of-the-art magnetometry-based AFEs. The challenges for MRX-based AFEs are: 1) MRX requires two more steps (Steps 3 and 5) leading to a $3 \times$ longer readout time and 2) the relaxation signal is broadband and overlaps with the sensor and AFE 1/f noise.

This article targets the best FoM based on MRX. Table I lists the state-of-the-art that is based on magnetometry [16] and our target specifications. A sensitivity (noise in Ω/R_0) of 0.98 parts-per-million (ppm) was reported in [17], so the target sensitivity was set to 0.1 ppm, with a comparable readout time <1 s and power consumption <5 mW. Target baseline and integrated noise are based on the sensor parameters. With $R_0 = 1.3 \text{ k}\Omega$, a transduction coefficient of 9 Ω/mT , and $H_A = 3 \text{ mT}$, the target noise is 14.4 nT_{rms}. To have a negligible baseline, the target baseline is set to 10× smaller than H_A .

To achieve these specifications, we propose a CMOS architecture with a MR-correlated double sampling (MRCDS) technique to reduce the readout time and system 1/f noise. DEM in the sensor bias network shapes and filters the 1/f noise. A fast-settling Miller compensation (FSMC) technique in the capacitively coupled instrumentation amplifier (CCIA) is proposed to reduce the power consumption. These result in an input-referred noise of 9.7 nT_{rms}, a power consumption of 4.32 mW, a readout time of 704 ms, and an FoM of 286 nT² · mJ—6.6× and 210× better than previously reported magnetometry and MRX-based AFEs, respectively.

The rest of the article is organized as follows. Section II describes the MRCDS and the system architecture followed by the circuit implementation in Section III. Section IV shows measurement results and conclusions are drawn in Section V.

II. SYSTEM ARCHITECTURE

A. Magnetoresistive Correlated Double Sampling

Fig. 3(a) shows the readout timing diagram that includes Steps 3–5 with the same duration, T_{cycle} . MCDS subtracts the signal at Step 3 from the signal at Step 5 to eliminate the baseline but suffers from long readout time and poor 1/*f* noise



Fig. 3. Comparison of MCDS and MRCDS. (a) Signal timing diagram. (b) 1/f noise rejection.

TABLE II Comparison of MCDS and MRCDS

	MCDS	MRCDS	
1/f noise rejection	$f < 1/(3T_{\rm cycle})$	$f < 1/(2T_{\text{cycle}})$	
Readout time	$3T_{\text{cycle}}$	$2T_{\rm cycle}$	
Total noise (same readout time)	$\sqrt{1.5} \sim 1.5 \times$	$1 \times$	
Baseline	0	$R_{ m MR}$	
Temp drift cancellation	Good	Fair	
Needs reference sensor?	No	No	

rejection. We propose an MRCDS technique that subtracts the signal at Step 4 from the signal at Step 5. Step 3 is no longer needed and thus the readout time is reduced. The 1/fnoise rejection is illustrated in Fig. 3(b) assuming that the AFE 1/f noise corner frequency is higher than $1/(2T_{\text{cycle}})$. Due to higher correlation, 1/f noise that is $<1/(2T_{cvcle})$ is eliminated for MRCDS while MCDS only removes 1/f noise that is $<1/(3T_{cycle})$. It should be noted that both techniques completely remove 1/f noise at low frequencies, thus enabling an unlimited tradeoff between resolution and readout time. Normalized to the same readout time considering only white noise, the noise improvement from MRCDS is $\sqrt{1.5\times}$ because of the $1.5 \times$ shorter time compared to MCDS; if only 1/fnoise is considered, the noise improvement from MRCDS is $1.5 \times$ because of the 1/f noise rejection. Therefore, the noise reduction for the same readout time is between $\sqrt{1.5}$ and $1.5 \times$. However, MRCDS cannot remove R_{MR} , which must be accommodated by the AFE DR. Given $R_{\rm MR}/R_{\rm rlx} \leq 2 \times 10^5$, the AFE DR requirement is 106 dB. Although 20 dB higher than MCDS that rejects 10× baseline, MRCDS still relaxes the DR requirement by 34 dB compared to when no CDS is applied. Temperature-dependent $R_{\rm MR}$ also limits the temperature drift rejection for MRCDS [16], [32]. The comparison between MCDS and MRCDS is summarized in Table II.

B. System Architecture

Fig. 4 shows a block diagram of the proposed sensor AFE. It consists of a sensor bias block, a CCIA, and a Zoom ADC. A low noise dc bias current, I_{in} , flows into the selected sensor, R_S , which is magnetically biased by an external Helmholtz coil. The resulting voltage, V_{in} , is amplified by the CCIA, which contains a dc reference input, V_R , and a dc servo loop (DSL) to continuously cancel the R_0 baseline. A ripple rejection loop (RRL) rejects the chopping ripple on V_{out} , which is quantized by the ADC. The Zoom ADC consists of a 6-bit SAR and a 13-bit $\Delta \Sigma$ modulator (DSM) for coarse and fine quantization, respectively. It is configured



Fig. 4. Block diagram of the proposed AFE.



Fig. 5. Schematic of the sensor bias block with DEM.

to measure V_{out} twice, either at Steps 3 and 5 for MCDS or Steps 4 and 5 for MRCDS.

III. CIRCUIT IMPLEMENTATION

A. Sensor Bias

Fig. 5 shows a schematic of the sensor bias block. The chopped OTA and the source degenerated current source transistors, M_0 , form a negative feedback loop to provide a voltage-controlled current, $3I_{in} = V_{bias}/R_{set}$, where R_{set} is an off-chip precision resistor and V_{bias} is an externally provided dc voltage. The current is attenuated by $3 \times$ to bias the selected sensor, R_S . A moscap, C_C , is used for compensation and source degeneration resistors, R_D , are used for noise reduction. The noise power at V_{in} can be written as

$$v_{n,\text{in}}^2 = R_{\text{S}}^2 \left[\left(\frac{v_{n,\text{op}}}{3R_{\text{set}}} \right)^2 + \frac{4k_{\text{B}}T}{9R_{\text{set}}} + \frac{4k_{\text{B}}T\gamma}{g_{\text{m0}}R_{\text{D}}R_{\text{S}}} + \frac{4k_{\text{B}}T}{R_{\text{D}}} + \frac{4k_{\text{B}}T}{R_{\text{S}}} \right]$$
(2)

where $v_{n,op}$ is the input-referred noise of the OTA and g_{m0} is the transconductance of M_0 . Since $V_{\text{bias}}/R_{\text{set}} = 3V_{\text{in}}/R_{\text{S}}$, larger V_{bias} and R_{set} reduce the noise contributed by the OTA and R_{set} . Having $R_{\text{D}} > R_{\text{S}}$ helps reduce the noise from M_0 and R_{D} . R_{S} is fixed from the sensor and V_{in} is limited by the sensor breakdown voltage, thus both R_{set} and R_{D} should be maximized for low noise but are limited by the maximum V_{bias} and minimum V_x , respectively.

To reduce the remaining 1/f noise from M_0 , DEM is added at the cascode node. A 2-to-4 decoder directs one of the branches to the output path and the remaining three branches to the feedback path. It is configured to rotate the four



Fig. 6. Schematic of the CCIA.

branches so the 1/f noise from M_0 is upmodulated to the DEM frequency, f_{DEM} . The mismatch from M_0 causes ripple on V_{in} at f_{DEM} but is out-of-band and subsequently filtered by the ADC decimation filter.

B. Chopped Capacitively Coupled Instrumentation Amplifier

Fig. 6 shows a schematic of the chopped CCIA that includes a DSL and an RRL. The CCIA has a dc gain of C_1/C_2 , where C_1 is a 2-bit programmable capacitor for variable gain. The reset switches used in the integrators of the DSL and RRL are implemented by low-leakage switches (leakage < 1 fA in simulation) [33]. The OTA has two stages, where g_{m1} is a differential-difference folded-cascode OTA for low noise and g_{m2} is a current mirror OTA for high output swing. g_{m1} and g_{m2} are simulated to be 4.1 and 0.8 mS, respectively. Although current reuse OTAs or stacked OTAs have been reported for better efficiency, their limited swing limits the performance in this application [34]-[36]. Both OTAs use switched-capacitor common-mode feedback for high output swing. Feedback resistors, $R_{\rm B}$, are implemented by duty-cycled resistors (DCRs) and an FSMC technique is proposed to maintain the stability, as will be discussed later.

The voltage across the sensor, V_{in} , and an externally provided dc voltage, V_R , are fed into the CCIA to form a pseudo-differential input. V_R is chosen to be $\sim I_{in}R_0$ to reject the R_0 baseline. This can be implemented by a low-matching replica as the offset between V_R and V_{in} can be further nulled up to $(C_3/C_1)V_{DD}$ by the DSL, which consists of



Fig. 7. (a) Schematic of the pulse generator. (b) DCR timing diagram.

an integrator and a 1-bit programmable capacitor, C_3 . The input-referred noise from the DSL is $(C_3/C_1)v_{n,DSL}$, where $v_{n,\text{DSL}}$ is the noise of the DSL. This presents a tradeoff between the maximum tolerable offset and the noise. The OTA, $g_{m,DSL}$, cannot be chopped due to the need for high input impedance and thus the 1/f noise from this OTA dominates the CCIA noise at low frequencies. The proposed MRCDS rejects this 1/f noise, thus it was not worth the effort to implement a mixed-mode DSL that would solve this [37]. Both the sensor mismatch and temperature dependence set the maximum input offset, thus the ratio of C_3/C_1 . The sensor mismatch can be up to $\pm 5\%$ [38], which results in up to 25 mV of offset. Thus, C_3/C_1 must be >0.014. Since C_1 is programmable for closed-loop gain control, C_3 is tuned in tandem to maintain the ratio. To have headroom to accommodate the R_0 temperature dependence, we designed C_3/C_1 to be 0.02–0.033 in all gain configurations.

The DSL sets the CCIA high-pass corner frequency to

$$f_{\rm HP} = \frac{C_1}{C_3} \frac{1}{2\pi R_{\rm DSL} C_{\rm DSL}} \tag{3}$$

where R_{DSL} and C_{DSL} are the resistor and capacitor in the DSL integrator. Since V_{in} is a pulsed waveform, the CCIA distorts the signal and f_{HP} determines the voltage drop on V_{out} at Steps 4 and 5 (Fig. 6, bottom left). The Zoom ADC is first configured as an SAR to coarsely quantize V_{out} and then "zoom" into ± 1 SAR_{LSB} for fine quantization, thus the voltage drop in one ADC conversion cannot exceed one SAR_{LSB}. Simulation shows that f_{HP} must be <1 Hz to not saturate the ADC. Given $C_3/C_1 = 0.02-0.033$, $C_{\text{DSL}} = 100$ pF (limited by area), R_{DSL} must be >80 G Ω . Therefore, R_{DSL} is implemented by a DCR with a 32-M Ω poly-resistor and a duty cycle of <1/2500. Further reducing the duty cycle to save the area results in a lower switching frequency for R_{DSL} , which causes aliasing [39].

To achieve such a small duty cycle, an on-chip pulse generator was designed, as shown in Fig. 7(a), where 2-bit programmable capacitors, C_{delay} , adjust the pulsewidth to compensate for process variation [34]. The pulsewidth was simulated to be



Fig. 8. (a) FSMC timing diagram and simulated transient results. (b) Equivalent schematics.

1.3–3.8 ns, based on C_{delay} . Since the multiplexed sensor array is read in a time-sequenced manner, the settling time when switching between sensors significantly increases the array readout time. Thus, fast-settling DCRs are used to improve the settling [17]. In Fig. 7(b), the DSL and RRL are first reset when switching sensors. The switches for R_B are kept closed to generate a low impedance path from V_b to $V_{a+/-}$, enabling fast settling at $V_{a+/-}$. When the DSL starts to operate, the switches for R_{DSL} are closed so the DSL integrator can quickly find the input offset due to the low impedance. In both the reset and settling phases, $EN_{DCR} = 0$ so $\varphi_{out} = \varphi_{in}$ for both DCRs. After the CCIA is fully settled, EN_{DCR} changes to 1 to place both DCRs into duty-cycled mode. Following a short idle period, the ADC sampling clock, φ_{samp} , starts quantizing V_{out} .

To ensure the CCIA stability, Miller compensation is commonly used to create a dominant pole internally with the nondominant pole at the output due to the ADC sampling capacitor, C_4 . Unfortunately, dc offsets from the input and V_{DSL} cause signal-dependent charge injection, which require sufficient settling time to maintain the linearity. The settling time is inversely proportional to the CCIA bandwidth (g_{m1}/C_C) . To ensure proper settling before ADC sampling, the most straightforward solution is to increase g_{m1} , resulting in an increased power consumption.

We propose an alternative approach, FSMC, whereby the compensation is dynamically changed, as shown in Fig. 8(a). A similar technique was used in an LDO to compensate different loads [40], but is different in that FSMC changes the compensation periodically. The timing of the CCIA and ADC is adjusted so that the sample switch is turned off right before every chopping edge to ensure that C_4 does not load V_{out} when the spikes appear. EN_{C2} disconnects C_{C2} so that only C_{C1} compensates the CCIA, enabling fast spike settling (due to the higher bandwidth). EN_{C2} closes the switches right before the next rising edge of φ_{samp} to guarantee C_{C2} is included to compensate the CCIA when C_4 loads V_{out} . The equivalent schematics in both phases of operation are illustrated in Fig. 8(b). Simulation results show that although FSMC results in larger spikes due to the higher bandwidth, the spikes settle much faster than the case that always connects $C_{C1} + C_{C2}$. A nulling poly-resistor, R_C , is placed in series with the compensation capacitors to generate a zero that cancels the



Fig. 9. RRL timing diagram and simulated results during (a) MRX and (b) FSMC.

nondominant pole. The value of R_C can be calculated as

$$R_{\rm C} = \frac{C_{\rm C1} + C_2}{g_{\rm m2}C_{\rm C1}} \tag{4}$$

$$R_{\rm C} = \frac{C_{\rm C1} + C_{\rm C2} + C_4}{g_{\rm m2}(C_{\rm C1} + C_{\rm C2})} \tag{5}$$

for $EN_{C2} = 0$ and $EN_{C2} = 1$, respectively. By selecting the capacitances properly, $R_{\rm C}$ can be equal in both cases. Inaccurate $R_{\rm C}$ causes mismatch between the pole and zero, but would not increase the settling time since the pole-zero doublet is placed close to the unity-gain bandwidth [41]. $C_{\rm C2}$ is designed to be $3 \times$ larger than $C_{\rm C1}$ to have a worst case phase margin of >75°. The proposed FSMC technique relaxes $g_{\rm m1}$ by $4 \times$ and thus reduces the CCIA power consumption by $2.5 \times$.

An RRL eliminates the ripple from the OTA g_{m1} offset [42]. The ripple at f_{chop2} passes through ac-coupling capacitors, C_{ac} , and is then downmodulated to dc. After the integrator, the RRL dynamically adjusts the g_{m1} offset through another differential pair, that consumes $10 \times$ less power than the main differential pair in the OTA. Compared to a conventional RRL, one more switch is added after $C_{\rm ac}$ to disable the RRL during the voltage pulses on V_{out} . Without this switch, the instantaneous voltage changes at V_{out} pass through C_{ac} to change V_{RRL} , thus creating an additional ripple, as illustrated in Fig. 9(a). It is simulated to take > 100 μ s to settle, significantly increasing the deadzone time. Instead, the switch is turned on ($Dis_{RRL} = 1$) right before the voltage changes to short the integrator inputs, thus $V_{\rm RRL}$ remains unchanged. After $V_{\rm out}$ is settled, the switch is turned off ($Dis_{RRL} = 0$) so the RRL returns to normal operation and keeps track of the g_{m1} offset. It should be mentioned that the RRL is required for FSMC, as shown in Fig. 9(b). Without the RRL, the ripple leads to a different V_{out} before and after $EN_{\text{C2}} = 0$. When EN_{C2} changes from 0 to 1, g_{m1} needs to charge C_{C2} , leading to another settling issue. The RRL cancels the V_{out} ripple so the voltage remains unchanged before and after $EN_{C2} = 0$. Accordingly, g_{m1} only needs to settle the charge injection from the EN_{C2} switches, which include half-sized dummy switches to absorb the charge injection [43].

C. Analog-to-Digital Converter

A Zoom ADC is a hybrid ADC for dc-input, high-resolution conversion [44]. Fig. 10(a) shows the block diagram, where a



Fig. 10. (a) Block diagram and (b) schematic of the Zoom ADC, (c) bootstrapped sampling switch, and (d) ADC timing diagram.

6-bit SAR coarsely quantizes V_{out} and then adjusts the reference voltages of the DSM with a 6-bit DAC. A pseudorandom bit sequence (PRBS) for non-segmented DEM is implemented off-chip by an FPGA to shape the DAC mismatch [45]. The mismatch-shaping DEM turns the spurious tones into white noise, which is spectrally shaped [46]. A first-order, single-bit DSM quantizes the residue voltage with an oversampling ratio (OSR) of 9956 and an on-chip counter decimates the bitstream, providing a 13-bit output. Since the SAR result needs to be extended by ± 1 SAR_{LSB} to avoid saturating the DSM, the Zoom ADC has a resolution of 18-bit. The sampling frequency is 1 MHz for a bandwidth of 100 Hz. The voltage residue during the DSM phase cannot exceed ± 1 SAR_{LSB}, so the maximum input frequency, f_{sig} , is

$$f_{\rm sig} < \frac{V_{\rm ref}}{2\pi A_{\rm sig} T_{\rm ADC} 2^6} \tag{6}$$

where $V_{\text{ref}} = V_{\text{ref}+} - V_{\text{ref}-}$ is the ADC reference voltage, A_{sig} is the input signal amplitude, and T_{ADC} is the ADC cycle time. Considering a full-scale sinusoidal input ($A_{\text{sig}} = V_{\text{ref}}/2$), $T_{\text{ADC}} = T_{\text{cycle}} = 10$ ms, f_{sig} must be <0.5 Hz to not saturate the ADC.

The implementation of the Zoom ADC is shown in Fig. 10(b). It consists of a switched-capacitor integrator, a dynamic latched comparator, and digital logic that generates



Fig. 11. (a) Annotated die photo. (b) Power distribution.



Fig. 12. (a) Measurement setup. (b) Measured sensor response to an applied field.

the clocks. 64×100 fF unit-caps implement the 6-bit, non-segmented CDAC. Bootstrapped sampling switches improve the linearity from 10.7 to 17.7 bits in simulation, as shown in Fig. 10(c). Instead of using 64 independent switches, the switches share the control transistors and the level shift capacitor, $C_{\rm bs}$. This reduces the area and minimizes the parasitic capacitance, C_{par} , at V_{bst} , which attenuates $V_{\rm GS}$ of $M_{\rm samp}$ during the sampling phase. The ADC timing diagram is shown in Fig. 10(d). The ADC is first configured as an SAR that samples V_{out} with $3 \times$ periods for settling. Then, $6 \times$ SAR conversion cycles are conducted with charge redistribution between C_4 and C_5 . Afterward, the SAR output adjusts the reference voltages for the DSM. Specifically, SAR_{out} ± 1 unit-caps C_{4j} connect to V_{ref+} , while the others connect to $V_{\text{ref}-}$, where D_{out} determines the sign. Timing of the Zoom ADC is critical for proper operation. The comparator clock, φ_{comp} , needs to be set up such that there is enough time for the delays of the comparator, DEM propagation, and scan chain. These delays limit the ADC speed. The reference voltages of the ADC, V_{ref+} and V_{ref-} , are set to V_{DD} and GND, respectively. Like a conventional DSM, bottom plate sampling and correlated double sampling are applied for high linearity and low 1/f noise, respectively.

IV. MEASUREMENT RESULTS

This chip was fabricated in a 180-nm CMOS process. An annotated die photo is shown in Fig. 11(a). It operates from a single 1.8-V supply and consumes 4.32 mW excluding the sensor bias, which is dependent on the sensor resistance and consumes 3.9 mW for the 1.3-k Ω sensors used in this work. The relative power contributions of each block (CCIA: 52%, ADC: 22%, digital: 20%, bias: 6%) are plotted in Fig. 11(b).

The measurement setup is shown in Fig. 12(a). A power amplifier (Kepco BOP 36-12ML) is connected to a custom coil driver and a Helmholtz coil, which generates a 3-mT



Fig. 13. Measured sensor bias noise spectra.



Fig. 14. Measured CCIA linearity versus input offset.

pulsed magnetic field for 10 ms. The coil driver, which is controlled by the FPGA (Opal Kelly XEM6310), enables a fast decay magnetic field for the sensor to minimize the deadzone (<2 μ s) [29]. The same FPGA is used for clocking and control signals for the chip, as well as capturing data from the ADC. The sensor array (MagArray, Inc.) is composed of an 8 × 10 array of sensors, where each sensor is 100 × 100 μ m². The array is read out in a time-sequenced manner where one sensor is selected at a time by two off-chip analog muxes. The sensors have an average R_0 of 1.3 k Ω and an average transduction coefficient of 9 Ω /mT, as shown in Fig. 12(b). The MR ratio, defined as $(R_{max} - R_{min})/R_{min}$, is 7.74% and the sensor mismatch within the same die is 1.6% (1 σ).

Fig. 13 shows the measured noise spectra at node $V_{\rm in}$ in the sensor bias block. The DEM reduces the 1/*f* noise corner frequency from ~300 Hz to <10 Hz and the spot noise at 50 Hz by 2.2× to 13.6 nV/ $\sqrt{\text{Hz}}$. It should be noted that only the spot noise at 50 Hz is relevant because MRCDS eliminates 1/*f* noise that is <50 Hz for $T_{\rm cycle} = 10$ ms. Upmodulated 1/*f* noise and current mirror mismatch generate tones at $f_{\rm DEM}$



Fig. 15. Measured ADC DNL and INL.



Fig. 16. Measured spectra of the signal path (CCIA+ADC).

and f_{chop} , which are out-of-band and filtered by the ADC decimation filter.

Fig. 14 shows the measured CCIA total harmonic distortion (THD) versus the input dc offset using a sinusoidal input with an output swing of 1.6 V_{pp} superimposed on the dc offset. This range covers up to a 4.3-mT magnetic field. Larger offset leads to more distortion due to incomplete settling of the ADC from the DSL. The FSMC technique settles these spikes faster and improves the CCIA linearity variation from 10 to 1.2 dB across the input offset range. The spectra at $V_{os} = -17$ mV have an 18-dB improvement in HD2. The asymmetric input offset range is due to the DSL offset. The linearity across the input range is >85 dB. The measured input-referred spot noise at 50 Hz is 6.6 nV/ \sqrt{Hz} .

The ADC was characterized using a dc sweep histogram by an audio analyzer (APx555B). Fig. 15 shows the measured differential nonlinearity (DNL) and integral nonlinearity (INL) over the input range of -0.8–0.8 V. The ADC has a DNL of -0.87/+1.19 LSB and an INL of -4.2/+4.5 LSB. The equivalent 95-dB SFDR is 10 dB higher than the CCIA THD. The ADC noise PSD is 745 nV/ \sqrt{Hz} , which is 14.9 nV/ \sqrt{Hz} when input-referred to the CCIA input. This is comparable to the noise from the other two stages, thus 18-bit resolution is



Fig. 17. Measured integrated noise versus readout time.

required to reduce the quantization noise. Although the CCIA gain can be increased to reduce the ADC noise contribution, it is in contrast with the DR requirement in MRCDS.

The signal path (CCIA+ADC) was characterized by applying a fully-differential sinusoid to the CCIA. The input frequency is 0.154 Hz, which satisfies (6) to not saturate the ADC. Fig. 16 shows the measured spectra, with and without DEM enabled. The spectra are truncated for a readout time of 704 ms. The SNDR improved from 61 to 81 dB by enabling the DEM. It should be noted that the 1/*f* noise shown in the spectra can be eliminated when MCDS or MRCDS is applied.

Fig. 17 shows the measured input-referred integrated noise versus the readout time. The proposed MRCDS has a 22-ms readout time, which consists of 2 ms for reset and 20 ms for measurement. MCDS needs 32 ms due to the additional cycle. The data can be averaged to lower the noise with a longer readout time. Both MCDS and MRCDS show a linear tradeoff between the readout time and the integrated noise on a log scale because the 1/f noise is eliminated. Without CDS, the residual 1/f noise limits the resolution for long readout times. MRCDS was measured to reduce the integrated noise by $1.34 \times$ compared to MCDS, which matches the theoretical range of $\sqrt{1.5-1.5 \times}$.

The input-referred baseline was measured for both MCDS and MRCDS, as shown in Fig. 18. MRCDS does not reject the R_{MR} baseline, and thus has higher baseline than MCDS. The residual baseline in MCDS comes from the DSL. Although f_{HP} in the CCIA is low enough to not saturate the ADC, it still distorts the waveform, leading to a residual baseline. Increasing R_{DSL} decreases f_{HP} , and thus reduces the baseline. The AFE has a measured baseline of 0.12 mT in the standard configuration of the CCIA, that is 25× smaller than MRCDS.

Fig. 19 shows the measured temperature response. Cold isopropyl alcohol (-18 °C) was added on the sensor surface at t = 3 min while the system was continuously measuring for 33 min. MR sensors typically have temperature coefficients (TCs) of 10.4 ppm/°C [17]. MRCDS and MCDS reduce the temperature dependence to 1.24 and 0.07 ppm/°C, respectively. Although both R_0 and R_{MR} are temperature sensitive, R_0 drift is rejected by both the DSL and the CDS



Fig. 18. Measured input-referred baseline versus DSL integrator resistance.



Fig. 19. Measured temperature dependence.

techniques. R_{MR} drift, however, can only be rejected by MCDS because MRCDS still contains the R_{MR} baseline. The AFE was measured to have a smaller temperature dependence (0.06 ppm/°C) and thus would not limit the performance.

Biological experiments were conducted for proof-ofprinciple demonstration. 40-nm MNPs (Ocean Nano-Technologies SHS-30-01) were dried on the sensor surface to mimic the MIA described in Fig. 1. To observe the temporal relaxation signal, an off-chip ADC (NI-6289) measured the CCIA output with a sampling rate of 500 kS/s and an 18-bit resolution. It should be mentioned that the on-chip Zoom ADC does not have the speed to capture this temporal signal but will be used to integrate the signal for higher efficiency in MIA experiments. Fig. 20(a) shows the measured relaxation curves of 70 sensors. With a relaxation time of 10 ms, the signal amplitude ranges from 1200 to 1500 ppm, depending on the surface coverage of the MNPs. Normalizing the relaxation curves by their final amplitudes, all curves follow (1), with a $t_{\rm C}$ of 19.3 ms. While $t_{\rm C}$ is highly dependent on the magnetization time and the magnetic field strength, the measured $t_{\rm C}$ matches empirical results in the literature [27].

An MIA was then conducted to demonstrate the system, as shown in Fig. 20(b). The first row of the sensor array (ten sensors) was covered by epoxy to prevent MNP binding, thus serving as a negative control. The other 70 sensors were functionalized with NHS-Biotin through APTES surface chemistry. Briefly, the sensors were immersed in 100 μ L of 1% KOH in deionized water (DIW) for 10 min at 37 °C.



Fig. 20. (a) Measured temporal relaxation curve for dried MNPs. (b) MIA real-time binding curves for active and reference sensors. (c) MIA coverage map.

	H. Wang ISSCC'09 [11]	D.A. Hall JSSC'13 [16]	T. Costa TBCAS'17 [15]	X. Zhou TBCAS'19 [17]	P. Liu JSSC'12 [12]	S. Gambini JSSC'13 [13]	This work (MCDS)	This work (MRCDS)
Sensor Type	LC	GMR	GMR	GMR	Hall	Hall	GMR	
Sensor Resistance (k Ω)	N/A	1.92	0.85	0.15	N/A	N/A	1.3	
MR Ratio (%)	N/A	9.2	5.37	9.04	N/A	N/A	7.74	
MNP Size (nm)	1,000	50	250	50	1,000	1,000	40	
Technology Node (µm)	0.13	0.18	0.35	0.18	0.18	0.18	0.18	
Sensing Method	Magneto	Magneto	Magneto	Magneto	MRX	MRX	MRX	
AFE Architecture	<i>LC</i> oscillator	TIA	Amplifier	PGA + Mixer	PGA	V/I Converter	CCIA	
ADC Architecture	VCO-based	ΔΣ	No ADC	Inc. $\Delta\Sigma$	No ADC	Inc. $\Delta\Sigma$	Zoom	
Input-referred Integrated Noise (nT _{rms})	N/A	32.8 ^ψ 49	11.5Ψ N/A	436 460	15♥ N/A	N/AΨ 1207	9.6 ^v 13	6.9 ^ψ 9.7
Readout Time/Ch. (ms)	400	250	1,000	11	64,000	50	704	
Power/Ch. (mW)*	N/A	2.24 ^{\varphi} 3.15	4.9 ^ψ	0.43 1.39	6.2Ψ	N/AΨ 0.825	2.5 ^v 4.32	
Area/Ch. (mm ²)	N/A	0.219	3.17	0.249	N/A	0.012	1.92	
Number of Ch.	8	16	1	1	1	160	1	
Input-referred Baseline (mT)	N/A	7.09	1.84	<0.235	< 0.001	0.007	0.12	3
Temperature Correction	Yes	Yes	No	Yes	Yes	Yes	Yes	No
Resolution FoM [†] (nT ² ·mJ)	N/A	602♥ 1,891	648 ^ψ N/A	899Ψ 3,235	89,280 N∕A	N/A ^ψ 60,143	162 [♥] 514	84 ^ψ 286

 TABLE III

 COMPARISON WITH STATE-OF-THE-ART MAGNETIC SENSOR AFES

* Power/Ch does not include sensor bias and magnetic field generator. * Does not include ADC. * FoM=Resolution²×Energy/Conversion.

The sensors were then washed with 300 μ L of DIW and allowed to dry. 70 μ L of 100% APTES was added for 1 h at 37 °C (paraffin was wrapped around the sensor well to prevent evaporation). The sensors were then washed 5× with 300 μ L of phosphate-buffered saline (PBS) and 50 μ L of NHS-Biotin (1 mg/mL in dimethyl sulfoxide) was added to the sensors for 1 h at 37 °C prior to washing 3× with 300 μ L of PBS. Blocking was accomplished by adding 100 μ L of 10% bovine serum albumin (BSA) in PBS for 15 min at 37 °C before removal and washing 3× with 300 μ L of PBS. Lastly, 100 μ L of PBS was added before the sensor array was moved to the measurement setup.

After removing the PBS and adding 50 μ L of MNPs, the active sensors showed signals of ~140 ppm, while the reference sensors showed no signal. The error bars represent one standard error. Since each sensor has a slightly different temperature dependence, the error bars increased with time because MRCDS was used. Fig. 20(c) illustrates the signal map of the 8×10 sensor array, where each signal amplitude represents the signal difference before and after adding the MNPs for each sensor. Compared to the dried MNPs, the MIA shows $\sim 10 \times$ smaller signal amplitude because of the increased distance between the MNPs and the sensor as well as the lower density due to the binding equilibrium. The signal variation is mainly from different number of binding sites on each sensor due to the blanket functionalization procedure used here.

This work is summarized in Table III. Compared to other magnetic sensor front-ends, this work has the lowest inputreferred noise, along with comparable power consumption and readout time. It results in a best-reported FoM of 286 and 514 nT² · mJ, respectively, for MRCDS and MCDS, which is 6.6× better than other magnetic AFEs and 210× better than MRX-based AFEs. While MRCDS shows the best FoM, MCDS has advantages on the baseline reduction and temperature drift cancellation. This work supports both techniques.

V. CONCLUSION

In this article, we present an MR sensor AFE with a Zoom ADC to detect MNP relaxation. A sensor bias block with DEM reduces 1/f noise from the bias transistors by $2.2 \times$. A CCIA with FSMC reduces the CCIA power consumption by $2.5 \times$, while maintaining the linearity and stability. An 18-bit Zoom ADC quantizes the CCIA outputs with an INL of 4.5 LSB. The system uses either MRCDS or MCDS to capture the signal, reject *R*0 baseline, and remove noise/time tradeoff limitation by eliminating 1/f noise. While MCDS is better for baseline rejection and temperature drift cancellation, MRCDS provides better 1/f noise rejection and takes less readout time, thus resulting in a better FoM. Experiments with dried MNP and an MIA were conducted to demonstrate the system. This work has a best-reported FoM, that is $6.6 \times$ better than other magnetic AFEs and $210 \times$ better than MRX-based AFEs.

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