A 6.1-nW Wake-Up Receiver Achieving −80.5-dBm Sensitivity Via a Passive Pseudo-Balun Envelope Detector

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***Abstract*—A wake-up receiver (WuRX) that achieves −80.5-dBm sensitivity with only 6.1 nW of power is presented. High sensitivity is achieved via a passive pseudo-balun envelope detector (ED) with a high input impedance (>750 kΩ ‖ <1.4 pF) that enables a 30.6-dB passive voltage gain transformer while providing differential output and improving the conversion gain by 2× compared to a conventional single-ended input passive ED for a given input capacitance. The WuRX is implemented in a 180-nm CMOS process and operates from a 0.4-V supply.**

***Index Terms*—Low-power wide-area network (LPWAN), low-power wireless, wake-up radios, wake-up receivers (WuRXs).**

I. Introduction

Low-power wide-area networks are a key component of future smart cities where infrastructure will be connected via an Internet of Everything. Many such connected devices (e.g., smart meters, environmental sensors, and threat monitors) must operate for years from small batteries or energy harvesters, and communicate over long distances. This necessitates inclusion of ultralow power radios with high sensitivity—two parameters that generally trade off directly with each other.

One way to significantly reduce average power consumption, particularly in event-driven networks with low-average throughput, is to replace energy expensive synchronization routines of the main radio with a low power, always-on wake-up receiver (WuRX). However, reducing the WuRX power below that of the main radio typically comes at the cost of reduced sensitivity via a low-complexity direct-envelope detector (ED) architecture (e.g., −45 dBm sensitivity at 116 nW [1]). Unfortunately, compromising sensitivity is not pragmatic, as network coverage is limited by the least sensitive receiver.

Reducing the data rate (i.e., baseband bandwidth) is an effective technique to improve the sensitivity of a WuRX. The most important metrics for WuRXs in low-average throughput applications are the power and sensitivity; data rate (and thus wake-up latency) is often appropriate to compromise in applications that communicate at low duty-cycles. In other words, energy/bit is not the most appropriate metric for WuRXs. Prior work has shown that through a combination of low carrier frequency operation (i.e., FM-band) and reducing the WuRX data rate, large passive RF voltage gain (at the expense of larger passive components) when combined with a high input impedance active ED results in improved sensitivity at extremely low power (e.g., −69 dBm at 4.5 nW [2], [3]), with wake-up latencies that still support the needs of low-average throughput applications.

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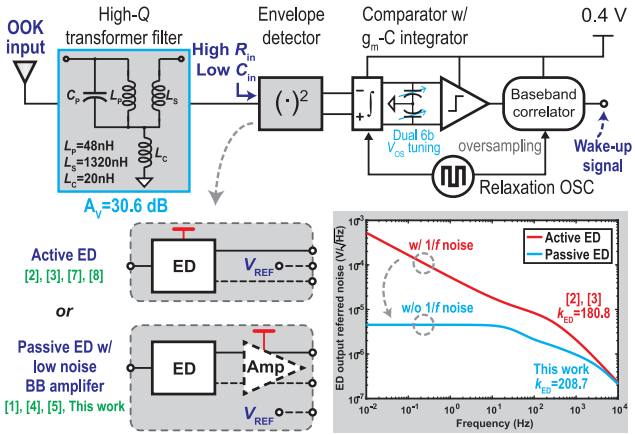

Fig. 1. Block diagram of the proposed WuRX.

Despite these improvements, WuRX sensitivity still lags that of most main radios, and must be further improved upon. Since the ED is the dominant noise source in a direct-ED receiver [3], recent work has shown that by implementing a multistage passive ED architecture, which, unlike active EDs, does not have any $1/f$ noise [4], high sensitivity at sub-10 nW is possible (i.e., −76 dBm at 7.6 nW [5]).

This letter presents the design of a WuRX that achieves −80.5-dBm sensitivity with only 6.1 nW by:

1) arranging the passive ED in a pseudo-balun topology to perform single-ended to differential conversion and improve the conversion gain by 2× compared to a conventional single-ended passive ED for a given input capacitance under the same input signal level [1], [5];
2) using higher V_t devices than in conventional passive EDs [1], [6] to increase the effective input resistance as well as a body-biasing technique to reduce the input capacitance, which enables the design of a passive voltage gain impedance transformer with 30.6 dB gain;
3) using a current-reuse baseband amplifier with asymmetric pseudo-resistors that increase the amplifier input impedance while avoiding prohibitively long start-up time.

The proposed WuRX architecture along with the passive pseudo-balun ED are described in Section II, while Section III presents the measurement results and concludes this letter.

II. System and Circuits Implementation

In this section, we present the working principle of each circuit block. Fig. 1 shows a block diagram of the proposed WuRX architecture where an OOK-modulated waveform is amplified and filtered by a high-Q passive transformer/filter. To support the passive gain, the ED must provide large enough R_{in} to not degrade the equivalent R_p of the transformer. Active EDs [2], [3], [7] offer R_{in}>100's of kΩ

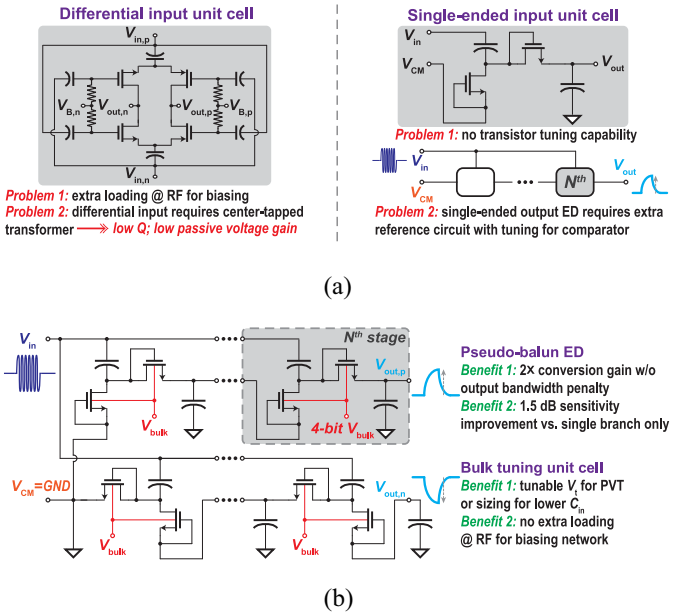

Fig. 2. (a) Conventional passive ED unit cells and architectures. (b) Proposed passive pseudo-balun ED with bulk tuning unit cell.

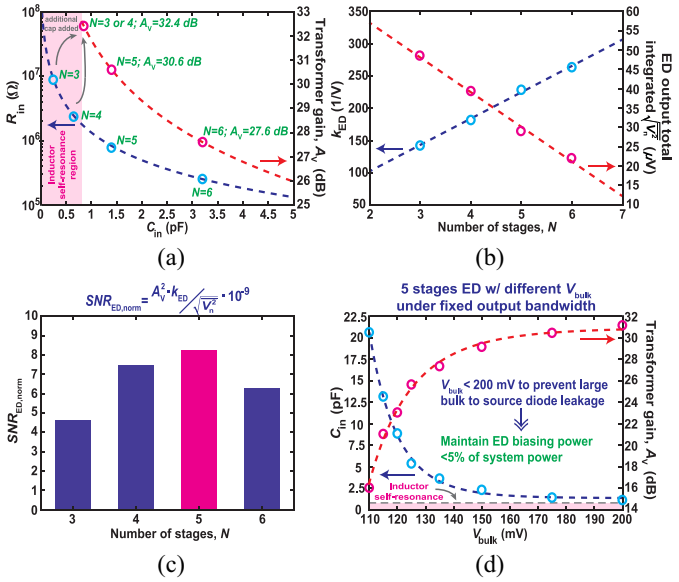

Fig. 3. Simulation results of ED tradeoffs for N stages with a fixed output bandwidth: (a) R_{in} and A_V versus C_{in}, (b) k_{ED} and $\sqrt{\overline{v_n^2}}$ versus N, (c) passive ED $SNR_{ED,norm}$, and (d) $N = 5$ stages ED tradeoffs for different V_{bulk}.

with wide bandwidths, but suffer from 1/f noise. Passive EDs, on the other hand, were historically designed with low-V_t devices [6] or with standard high-V_t devices along with V_t-cancelation techniques to maximize power (not voltage) conversion efficiency, which results in a small R_{in}. By using higher V_t devices, passive EDs can achieve comparable R_{in} to active EDs, and, most importantly, do not have any 1/f noise [4] since there are no dc currents. This permits smaller devices and thus lower input capacitance, C_{in}. As such, the proposed passive ED has a lower noise-equivalent power and lower C_{in} than the active ED in [2] and [3]. The lower C_{in} allows for a larger secondary coil (at the same carrier frequency), resulting in 30.6 dB of passive gain. The ED output is fed to a low-noise baseband amplifier followed by a tunable comparator and a 36-bit digital correlator, both clocked by a relaxation oscillator. The hamming distance between the 6× oversampled code and a programmable code is compared against a programmable threshold to determine a wake-up event.

A. Passive Pseudo-Balun Envelope Detector

Fig. 2(a) and (b) depict conventional and the proposed passive ED unit cells and architectures. Cross-coupled self-mixers [4] rectify a differential input signal and thus require a center-tapped transformer, which results in lower Q and thus lower passive gain compared to a single-ended design. Moreover, biasing is implemented using an extra RC network at the RF node that reduces the ED input impedance. On the other hand, a traditional Dickson rectifier operating in sub-V_t [1], [5] can rectify a single-ended input signal, but does not have any tunability and only has a single-ended output, which requires a tunable reference circuit for the comparator. To overcome these issues, a tunable passive pseudo-balun ED architecture is proposed, which is a 2N-stage rectifier with the middle node connected to V_{CM} and the bulk nodes connected to a tunable voltage, V_{bulk}, to set the bandwidth [Fig. 2(b)]. As such, the baseband ac currents flow in opposite directions relative to ground to form a pseudo-differential output. Compared to the original single-branch N-stage Dickson rectifier, this structure achieves 2× conversion gain and a 1.5-dB sensitivity improvement under the same input signal level without sacrificing output bandwidth. Although the second branch of the N-stage ED could be connected in parallel with the first branch without flipping the polarity, this results in the same 1.5-dB improvement in sensitivity, but only half of the conversion gain and is single-ended. V_{bulk} is provided by a diode-connected reference ladder with 4-bit tunability.

To drive a fixed capacitive load from the baseband amplifier, an ED with a large number of stages, N, requires larger transistor widths to maintain the same output bandwidth, and thus has a larger C_{in}, which limits the achievable transformer gain. As the transistor width increases, the parasitic capacitance from the ED starts to add on to the fixed capacitive load at the output node, which thus requires R_{out} to decrease further. As shown in Fig. 3(a), larger transformer passive voltage gain, A_V, is possible with small N, which has higher R_{in} and lower C_{in}. However, as shown in Fig. 3(b), since the conversion gain and thus ED scaling factor, k_{ED}, are proportional to N, an ED with large N is more suitable for post-ED stage noise suppression. Moreover, since the passive ED noise power density is $4k_BTR_{out}$, an ED with a larger N has less total integrated noise, $\sqrt{\overline{v_n^2}}$. To find the optimum N, an objective function was developed to compare designs with different N under the same output bandwidth and operating frequency

$$SNR_{ED,norm} = \frac{A_V^2 \cdot k_{ED}}{\sqrt{\overline{v_n^2}}} \cdot 10^{-9} \quad (1)$$

which is essentially the achievable ED output SNR normalized to its input voltage. As shown in Fig. 3(c), an optimum value of $N = 5$ was found for the ED using this equation. On the other hand, the proposed bulk tuning can not only be used to overcome process variation, but can also effectively reduce C_{in} via smaller devices for an equivalent output bandwidth, and therefore maximize the achievable passive voltage gain at a given carrier frequency. It is depicted in Fig. 3(d) that by forward biasing the bulk-to-source junction diode (< 200 mV), V_t is reduced and allows smaller width transistors to be implemented for a given output bandwidth (33.3 Hz in this design). Although the proposed ED could be designed with pMOS devices in a process without a deep N-well, nMOS is adopted in this design

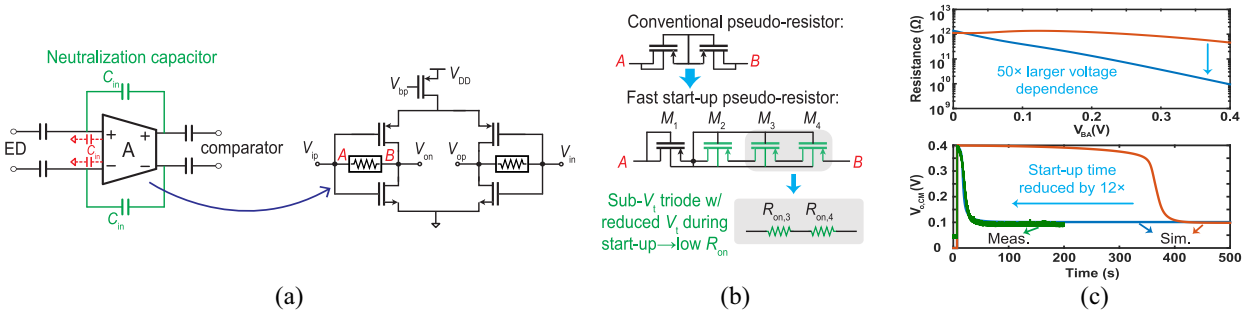

Fig. 4. Schematic of (a) ac-coupled baseband amplifier and (b) fast start-up pseudo-resistor. (c) Simulated and measured resistance and start-up time.

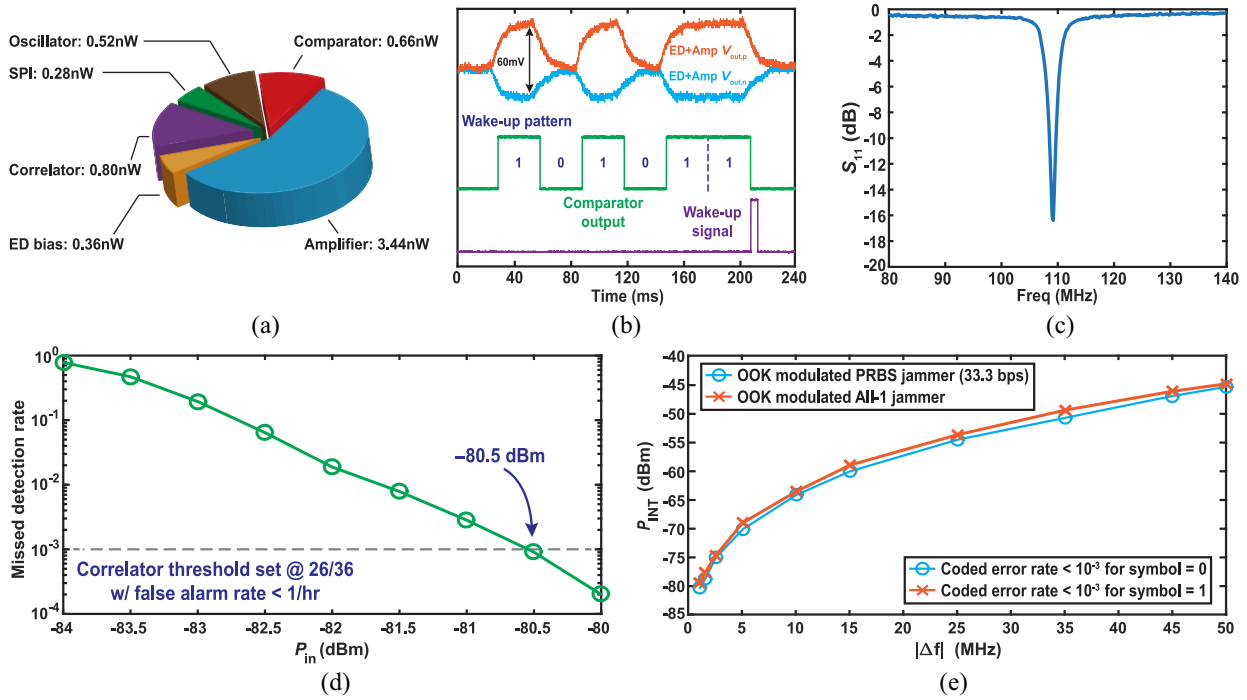

Fig. 5. Measurement results showing: (a) power breakdown, (b) transient waveforms for a wake-up event, (c) S_{11}, (d) MDR versus input signal power, and (e) OOK-modulated interferer power versus frequency.

to leverage the higher mobility and thus lower transistor size for a given output bandwidth.

B. Baseband Circuitry and Coding

With a passive ED, most of the power can be devoted to the subsequent baseband amplifier to minimize its noise. A continuous-time amplifier was implemented using a self-biased, inverter-based structure [Fig. 4(a)]. Both the input and output are ac-coupled to remove dc offset, filter 1/*f* noise, and band-limit the signal. Given the large ED output impedance (> 1GΩ), the amplifier input capacitance must be low enough to maintain the baseband bandwidth while also balancing the 1/*f* noise. Neutralization capacitors were used to mitigate the Miller effect and reduce the input capacitance from 12 to 0.4 pF. To not degrade the ED gain, the pseudo-resistors used for biasing need to be > 1TΩ, which, when implemented using conventional techniques, led to a long start-up time (> 400 s) that could be an issue deploying the WuRX in some applications. An asymmetric pseudo-resistor is proposed that leverages the high nonlinear voltage dependence to speed up settling. When the supply is ramping up, node *B* is rapidly pulled to V_{DD}, while node *A* (without a dc path to the supply) stays near ground. As shown in Fig. 4(b), this drives M_{3-4} into subthreshold triode with reduced V_t ($V_{SG} = V_{SB} \sim V_{DD}/2$ and $V_{SD} \sim 0$) and thus lower dc resistance (50× lower than a conventional implementation), allowing 12× faster startup. Once V_{SG} and V_{SB} approach zero, the pseudo-resistor returns to the high resistance state so as to not affect the small-signal resistance [Fig. 4(c)].

The output of the baseband amplifier is digitized by a comparator implemented using a dynamic g_m-C integrator with two 6-bit tunable load capacitor arrays to adjust the threshold voltage [7]. Using a baseband amplifier relaxes the required tunable threshold step size in the comparator (i.e., 100's of μV instead of a few μV), allowing it to be lower power. The 36-bit digital correlator is implemented using custom logic cells and computes the Hamming distance between the incoming code and a programmable code. The 200-Hz clock for the comparator and digital correlator is generated by a relaxation oscillator consuming only 520 pW. To overcome phase asynchronization, the baseband signal is oversampled by 6×, and the designed pattern provides 2.5-dB coding gain.

III. Measurement Results and Conclusion

This circuit was fabricated in a 0.18-μm CMOS process and consumes 6.1 nW [Fig. 5(a)]. Measured transient waveforms are shown

TABLE I
PERFORMANCE COMPARISON OF STATE-OF-THE-ART SUB-300-NANOWATT WURXS

	[1] CICC'13	[4] CICC'17	[7] ESSCIRC'17	[8] ISSCC'18	[2] ISSCC'17	[5] ISSCC'18	**This Work**
Technology	130 nm	130 nm	180 nm	65 nm	180 nm	130 nm	**180 nm**
Supply Voltage	1.2 / 0.5 V	0.5 V	0.4 V	0.5 V	0.4 V	1.0 / 0.6 V	**0.4 V**
Digital Correlator	31-bit	11-bit*	32-bit	3∼10-bit	32-bit	8-bit	**36-bit**‡
Clock	XTAL osc.	No	Relaxation osc.	Relaxation osc.	Relaxation osc.	Ring osc.	**Relaxation osc.**
Passive RF Voltage Gain	5 dB	27 dB$^{\triangleleft}$	18.5 dB	N.R.$^{\diamond}$	25 dB	27 dB	**30.6 dB**
Demodulator Type	Passive Dickson single-ended ED	Passive self-mixer	Active CG pseudo-balun ED	Active CS-CG single-ended ED	Active CS single-ended ED	Passive Dickson single-ended ED	**Passive Dickson pseudo-balun ED**
Carrier Frequency	403 MHz	550 MHz	405 MHz	57 kHz	113.5 MHz	151.8 MHz	**109 MHz**
Data Rate	12.5 kbps	400 kbps†	300 bps	336 bps	300 bps	200 bps	**33.3 bps**
Wake-Up Latency	2.48 ms	27.5 μs	53.3 ms	8.9∼29.8 ms	53.3 ms	>80 ms$^{\triangleright}$	**180 ms**
Sensitivity	−45 dBm	−56.4 dBm	−63.8 dBm	−60.1 dBm$^{\wr}$	−69 dBm	−76 dBm	**−80.5 dBm**
Sensitivity Normalized to 1/Latency$^{\circ}$	−58 dB	−79.2 dB	−70.2 dB	−68.5 dB$^{\wr}$	−75.4 dB	−81.5 dB	**−84.2 dB**
Power Consumption	116 nW	222 nW	4.5 nW	8 nW	4.5 nW	7.6 nW	**6.1 nW**

*Off-chip and not in the power budget.
‡6-bit code sequence with 6× oversampling.
$^{\triangleleft}$Assuming off-chip inductors with a Q of infinity.
$^{\diamond}$Not reported.
†36.36 kbps data direct-sequence spread spectrum encoded by a 11-bit baker code.
$^{\triangleright}$Half clock cycle value not provided.
$^{\wr}$7-bit wake-up pattern was used for measurement.
$^{\circ}P_{\mathrm{SEN}} - 5\log\frac{1}{Latency}$, where 5 log is used for non-linear squaring demodulator [3].

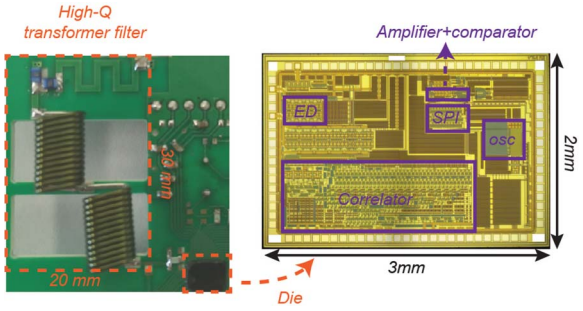

Fig. 6. Board and die photograph.

in Fig. 5(b) with a 180-ms wake-up latency. The measured transformer A_{V} was 30.6 dB, k_{ED} was 208.7/V, and the amplifier gain was 28 dB. Fig. 5(c) shows the measured S_{11}, indicating good matching at 109 MHz. Fig. 5(d) shows missed detection rate (MDR) curves after correlation, where a 0.1% MDR was achieved with random (i.e., unsynchronized) transmission at −80.5 dBm while maintaining a false alarm rate $< 1/\mathrm{h}$. Part-to-part measurements ($n = 5$) showed that the sensitivity and power were all within 0.5 dB and 0.2 nW, respectively. Fig. 5(e) depicts the interferer tolerance where a 33.3-bps PRBS OOK-modulated jammer was used to characterize the coded error rate for symbol-0 (i.e., false alarms), while an all-1 jammer was used for symbol-1 (i.e., missed detections). The interferer power is defined as the power needed to achieve 0.1% MDR when the signal is 1 dB higher than the sensitivity. Table I summarizes the proposed design and compares it to state-of-the-art sub-300-nW WuRXs. This design achieves the best sensitivity and sensitivity normalized to 1/Latency. It should be noted for a WuRX, as long as a reasonable wake-up latency is achieved (e.g., <1 second for many low-average throughput applications), the most important metrics are the power consumption and sensitivity. Metrics, such as the energy/bit and bandwidth, are not as important since a WuRX has, by design, low throughput. A die and PCB photograph are shown in Fig. 6.

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