28.4 A 400mV$_{pp}$ 92.3dB-SNDR 1kHz-BW 2nd-Order VCO-Based ExG-to-Digital Front-End Using a Multiphase Gated-Inverted Ring-Oscillator Quantizer

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Next-generation wearable devices will enable clinical-grade, continuous ExG (ECG, EEG, EMG, etc.) biopotential monitoring, providing medical professionals with valuable longitudinal data outside of hospital settings. These devices must be ultra-low power (<10μW) to enable long battery life while accurately digitizing sub-kHz, μV-level ExG signals in the presence of large motion and/or stimulation artifacts (>100mV) with high input-impedance (Z_{in}>10MΩ) to avoid signal attenuation. Achieving such performance with conventional PGA+ADC architectures is challenging due to the conflicting low-power and >90dB dynamic-range (DR) requirements [1]. To address this, several direct digitization analog front-ends (AFEs) have been reported [2-4]. While these offer wide DR, they typically have low input-impedance (<5MΩ) and/or low power-efficiency (FoM≤172dB). This paper presents a scalable 2nd-order voltage-controlled oscillator (VCO)-only ΔΣ ADC that achieves 92.3dB SNDR in a 1kHz bandwidth using a mismatch tolerant, multiphase gated-inverted ring-oscillator (GIRO) quantizer with dynamic power-scaling. The ADC uses an impedance-booster to maintain >50MΩ input-impedance over the entire bandwidth while consuming 4.25μW during nominal operation and 5.8μW in the presence of artifacts resulting in an FoM of 174.7dB.

Continuous-time ΔΣ ADCs are prime candidates for a high-precision, direct-digitization AFE due to their inherent anti-aliasing and high power-efficiency compared to their discrete-time counterparts. VCO-based ADCs are attractive for sensor AFEs due to their process-node scalability, reduced sensitivity to metastability, and intrinsic mismatch shaping [3]. However, the performance of VCO-based ADCs is limited by: 1) open-loop operation, which has poor linearity (typically <60dB), and 2) 1st-order noise shaping, which requires a large oversampling ratio (OSR) or a high-precision inner quantizer, both of which reduce the power-efficiency. For example, the VCO in [2] is operated open-loop, and while digital nonlinearity correction is used, the input range and SFDR are limited to 50mV and 79dB, respectively. In [3], a closed-loop architecture improves the linearity by reducing the input swing; however, the large OSR requires a high chopping frequency that degrades Z_{in} to 200kΩ, which is not acceptable for many ExG applications. A dc-coupled architecture combining a G_m-C integrator and a VCO quantizer in [4] achieves 92dB SFDR and high dc Z_{in}; however, it is susceptible to 1/f noise and input common-mode voltage variation.

To address these challenges, we propose a 2nd-order VCO-only ΔΣ ADC, as shown in Fig. 28.4.1. The input is chopped and ac-coupled onto a G_m-cell to remove the 1/f noise and improve the common-mode rejection. The reduced Z_{in} due to chopping is remedied by an auxiliary precharge buffer [1] that boosts Z_{in} from 5MΩ to >50MΩ. The G_m drives a 30-stage current-controlled oscillator (CCO) that integrates the input in the phase domain. The CCO output is fed to a phase-frequency detector (PFD) and then an XOR gate to eliminate the dead-band and perform input polarity detection. This enables the use of a tri-state ring-oscillator, a GIRO, which as explained later, reduces the effect of mismatch induced nonlinearity by 20dB. Like a switched-ring-oscillator (SRO) or a gated-ring-oscillator (GRO) quantizer, the proposed GIRO has 1st-order noise shaping for an overall ADC with 2nd-order noise shaping. This system has 5× 4b GIRO quantizers in parallel, each tapping a different phase of the CCO allowing the free-running frequency to be reduced by 5×, thus improving the power efficiency. Since the phase difference encoded in the pulse width is proportional to the input amplitude, the power of the inner quantizers scales dynamically with the input amplitude, reducing the power consumption in the absence of artifacts. The quantizer outputs are summed and fed to a 7b capacitive DAC with segmented dynamic element matching (DEM) to close the loop.

Prior work uses an inner-quantizer where, depending on the input polarity, the PWM-encoded signal is sent to either a positive or negative path each containing a noise-shaped TDC [5]. Path mismatch causes even-order distortion that significantly degrades the linearity, even with just a few percent mismatch despite occurring in the second stage. This architecture also requires the TDC in the "inactive" path to hold its state for a long duration, which is problematic if implemented as a GRO. Simulation with typical mismatch predicts a mean SFDR of 85dB (20dB worse than our target), as shown in Fig. 28.4.2. To address these issues, we propose using a single GIRO. The GIRO is a 3-state oscillator that either maintains, rotates clockwise, or rotates counterclockwise. The PFD outputs go through an XOR gate and a D flip-flop that extract the phase difference and feed forward the sign to the quantizer. This structure enables the two paths to share the capacitance and bias current improving the matching by an order of magnitude for similar sizing, thus ensuring high SFDR across process, voltage, and temperature variation.

A known challenge with PWM encoding is managing the tones generated at the modulation frequency and its harmonics [5]. These tones significantly degrade the performance if no precautions are taken to ensure they do not fold back in band. A single-phase quantizer requires f_{CCO}>>f_s, which is power-inefficient as it requires burning more power in the CCO and increases its noise. To improve upon this, it has been proposed to tap multiple phases of the CCO to increase the effective PWM frequency enabling a reduced f_{CCO} and thus better power-efficiency [5]. However, [5] uses a multi-level SRO that loses the intrinsic linearity associated with two-level quantizers. To address this, we propose using multiple quantizers in parallel, as illustrated in Fig. 28.4.3 (for a 3-phase case). By tapping equidistant nodes in the CCO, the TDCs pulses are encoded at equidistant phases. Critically, while the main tone generated by the input is in-phase across the quantizers, the PWM tones are out-of-phase, but at f_{CCO}. The tones still fold in-band but are cancelled when the quantizer outputs are digitally summed. Since each quantizer operates only between two states, they maintain their intrinsic linearity property. To keep the loop dynamics constant, the frequency of each GIRO quantizer is inversely scaled with the number of quantizers, thus the increase in power consumption is negligible. There is a tradeoff as increasing the number of quantizers increases the quantization noise but decreases the in-band tone folding. Simulations show a shallow optimum around 5 phases, which is what we chose.

This chip is fabricated in 65nm CMOS occupying 0.075mm^2. The AFE consumes 5.8μW when operated from 1.2 and 0.8V supplies. Figure 28.4.4 shows a measured output spectrum with a 400mV$_{pp}$ full-scale input achieving 92.3dB SNDR and DR in a 1kHz bandwidth. The dynamic power scaling of the second stage results in 35% lower power for typical ExG input amplitudes (<10mV). Figure 28.4.5 shows the artifact resilience with two 200mV$_{pp}$ tones, where the intermodulation distortion (IMD) tones are -99.8dBc. Z_{in} is boosted by >12× to 60MΩ due to the auxiliary pre-charge path across the entire bandwidth. The input-referred noise was measured to be 3.56μV$_{RMS}$ in-band. An ECG lead II measurement was collected using the AFE. Motion artifacts were intentionally induced to demonstrate that the ECG is still recoverable. Figure 28.4.6 compares this work with state-of-the-art sensor front-ends and Fig. 28.4.7 shows an annotated die photo. This work demonstrates a unique dynamic power scaling feature while providing the high Z_{in} necessary for interfacing with dry electrodes and achieves a state-of-the-art 174.7dB FoM and 110.3 dB SFDR.

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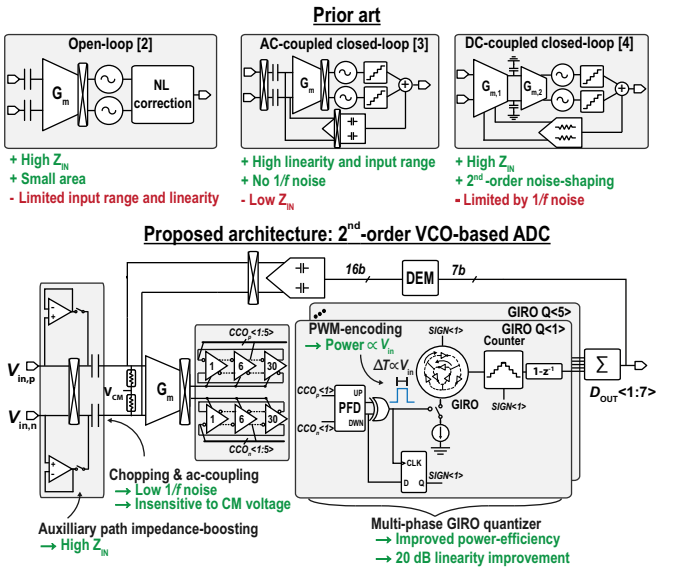

Figure 28.4.1: Pros and cons of prior VCO-based sensor interfaces and proposed architecture.

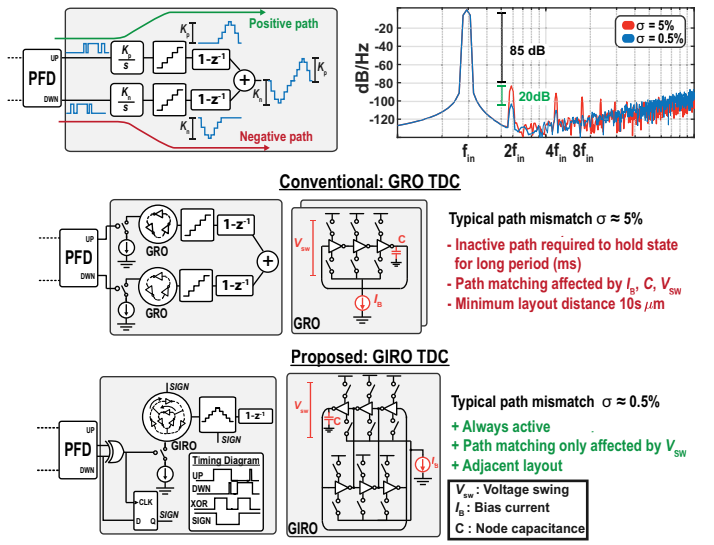

Figure 28.4.2: Issue with pseudo-differential path mismatch and simulation results of mismatch induced distortion, conventional GRO-based TDC, and proposed GIRO TDC.

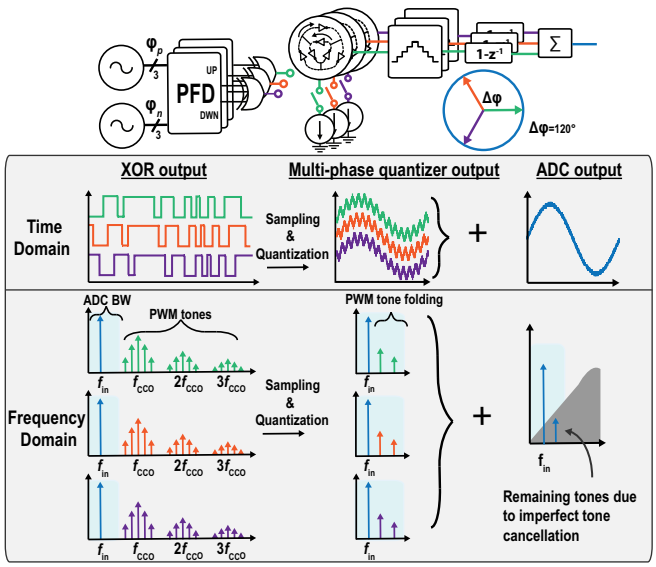

Figure 28.4.3: Proposed sampled multi-PWM based quantizer; time and frequency domain representation of the signals.

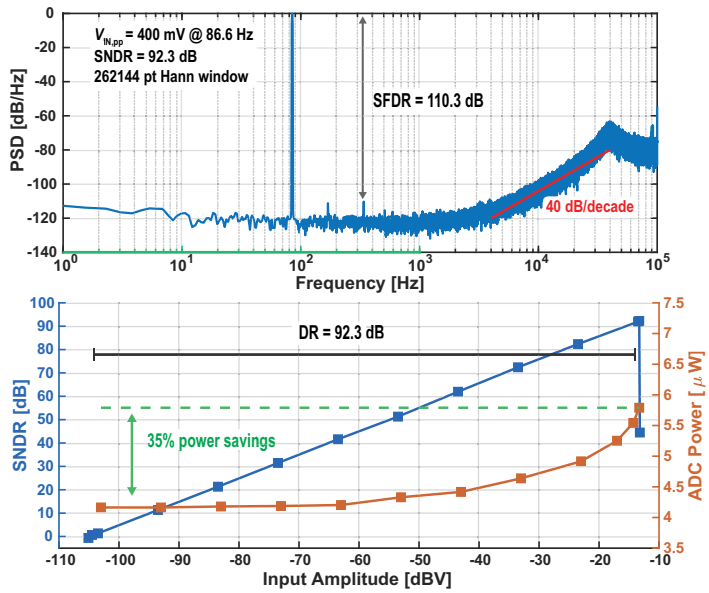

Figure 28.4.4: Measured spectrum; SNDR and power versus input amplitude.

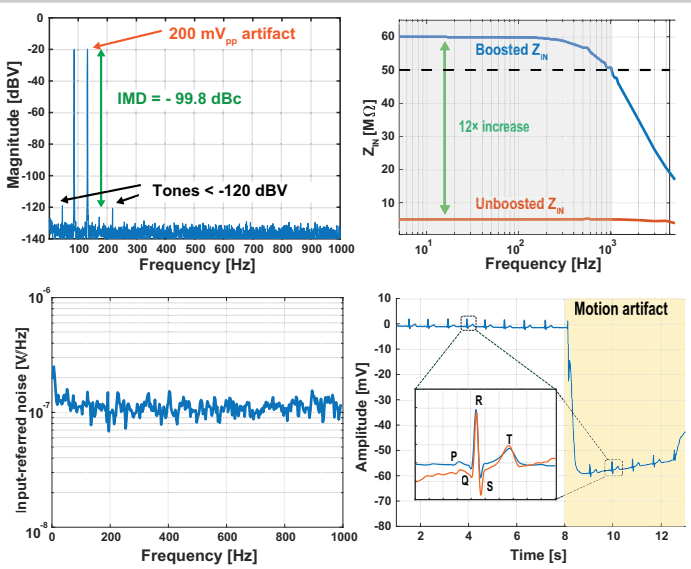

Figure 28.4.5: Measured linearity, Z_{in}, input-referred noise, and an ECG with a motion artifact.

	J.Huang VLSI 2020	S.Li CICC 2020	W.Jiang JSSC 2017	C.Lee ISSCC 2020	J-S Bang VLSI 2018	H.Chandrakumar JSSC 2019	This work
Integration Domain	Time	Time	Time	Hybrid	Voltage	Voltage	**Time**
Topology	1st-ord. VCO	1st-ord. VCO	Open-loop VCO	2nd-ord. Gm-C/VCO	3rd-ord. CTΔΣ	CCIA + 3rd-ord. CTΔΣ	**2nd-ord. VCO**
Technology [nm]	65	40	40	65	180	65	**65**
Area [mm²]	0.08	0.025	0.135	0.078	0.5	0.113	**0.075**
Supply (A/D) [V]	1.2/0.7	0.8/0.6	1.2/0.45	1	1	1.2	**1.2/0.8**
Power [μW]	3.2	4.5	7	6.5	6.5	7.3	**4.25/5.8**
Coupling	ac	ac	ac	dc	ac	ac	**ac**
Input-range [mV_{pp}]	250	100	100	300	360	200	**400**
Sampling frequency [kHz]	32	2500	3	1280	12.8	400	**200**
BW [kHz]	0.5	10	0.2	10	0.3	5	**1**
CMRR [dB]	98	83	66	76	84	78	**89**
Input-referred noise [nV/√Hz]	53	36	367	95	265	90	**110**
SNDR [dB]	88.1	78.5	75.2	80.4	84.3	78	**92.3**
DR [dB]	94.2	79	77.4	80.4	84.3	81	**92.3**
SFDR [dB]	105.1	91	79	92.2	104.7	81	**110.3**
Z_{in} at DC [MΩ]	4	0.22	∞	∞	39	1500	**60**
Z_{in} at BW [MΩ]	4	0.22	8	13.3	39	19.6	**50**
FoM_{SNDR}[dB]	170	172	149.6	172.3	160.9	166.4	**174.7**

FoM_{SNDR} = SNDR + 10log10(BW/Power)

Figure 28.4.6: Summary of performance and comparison to the state-of-the-art.

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