# A 400mVpp 92.3dB-SNDR 1kHz-BW 2nd-Order VCO-Based ExG-to-Digital Front-End Using a Multiphase Gated-Inverted Ring-Oscillator Quantizer

**Corentin Pochet**, Jiannan Huang, Patrick Mercier, and Drew A. Hall


University of California, San Diego

# Self Introduction

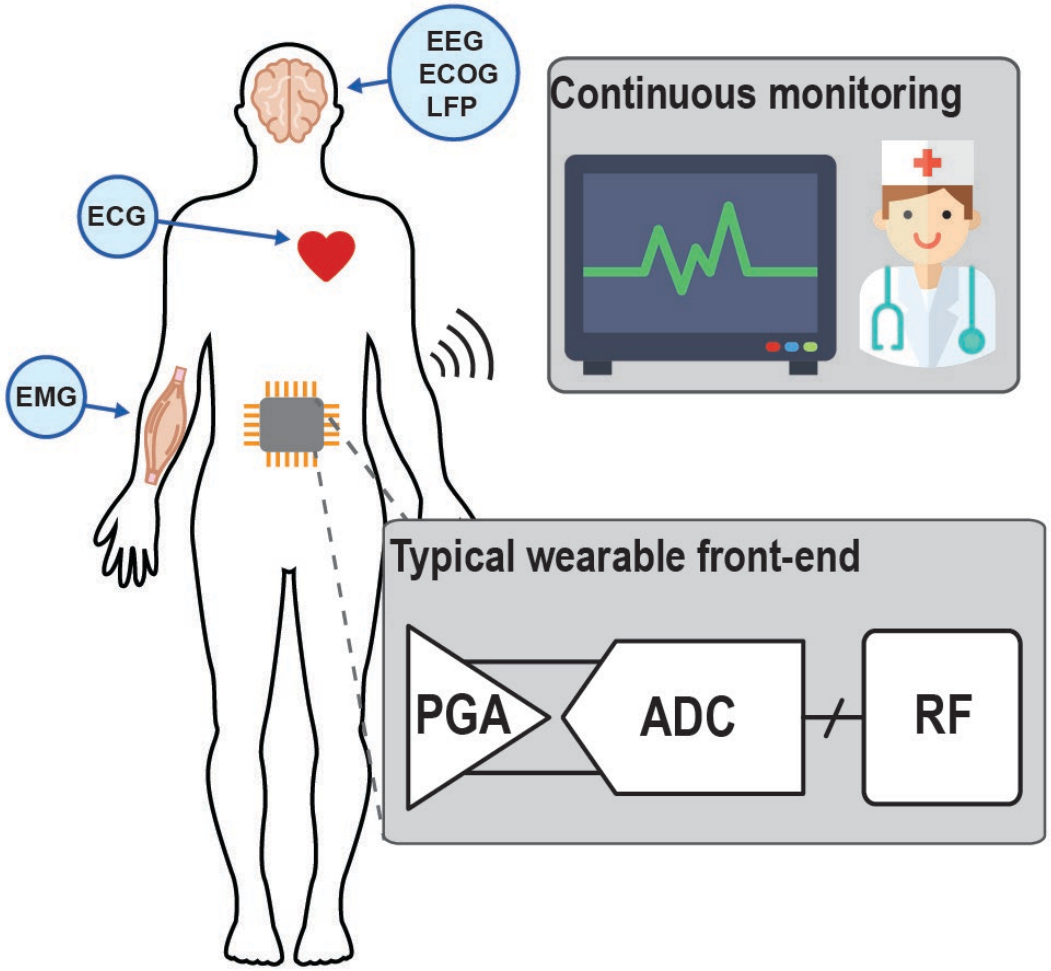
## Corentin Pochet

- B.Sc. and M.Sc. from ULB, Brussels, Belgium
- Henri Benedictus BAEF Fellow
- Ph.D. student in the Biosensor and Bioelectronics lab at the University of California, San Diego
- Research focused on low-power power sensor front-ends and time-based ADCs

# Needs and Challenges

## Continuous wearable physiological monitoring:

- Improved health monitoring
- Sport performance monitoring
- Rare event (anomaly) detection



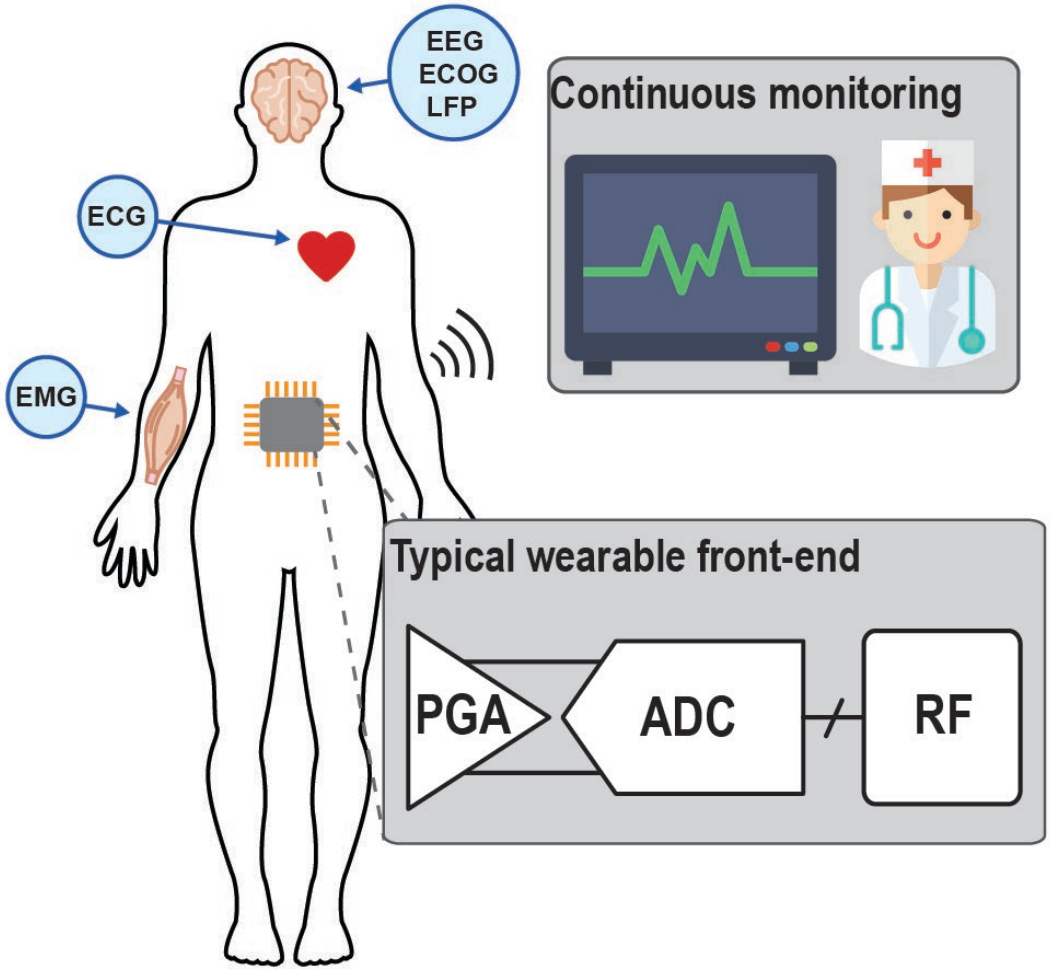
# Needs and Challenges

## Continuous wearable physiological monitoring:

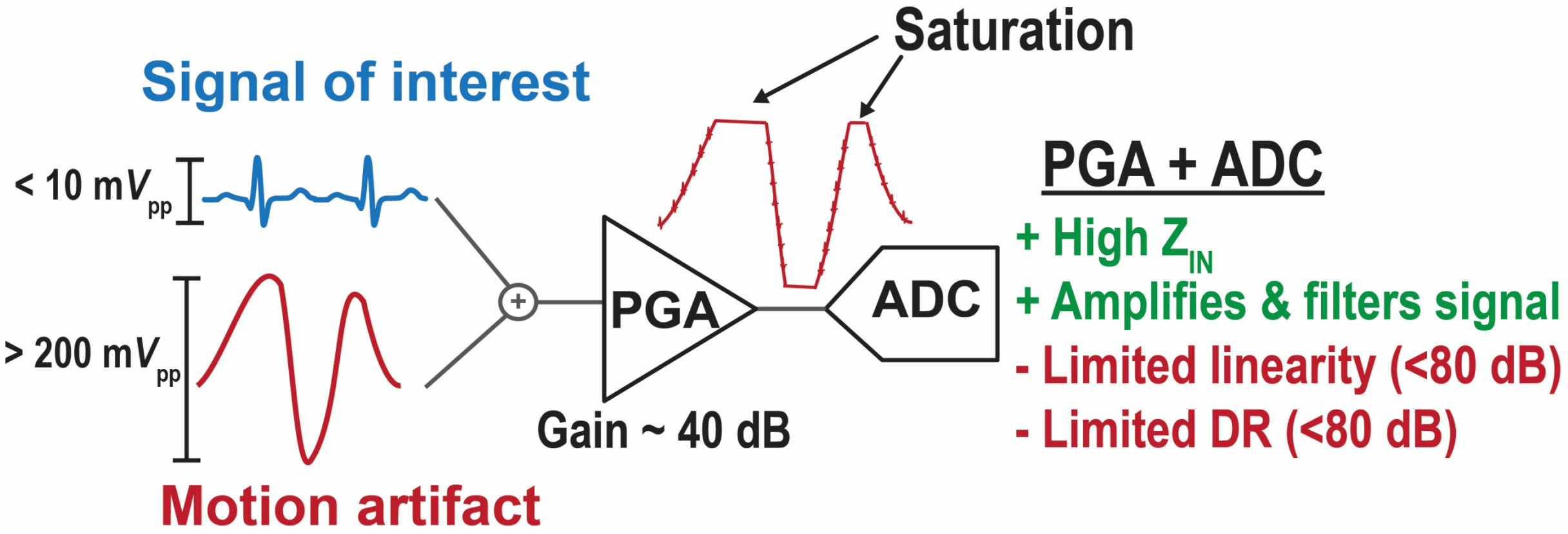
- Improved health monitoring
- Sport performance monitoring
- Rare event (anomaly) detection

## Requirements:

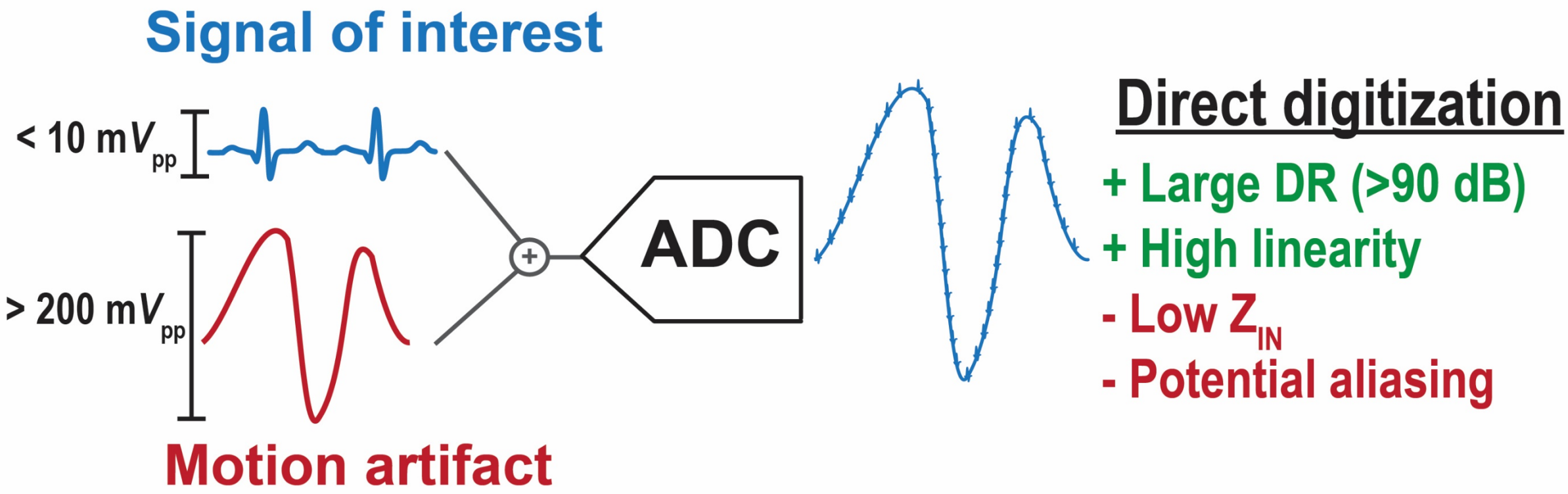
- Low power (<10 μW)
- Low noise (<5 μVrms)
- Low bandwidth (< 1 kHz)
- High input-impedance (>50 MΩ)
- High dynamic range (>90 dB)



# PGA-ADC Front-ends



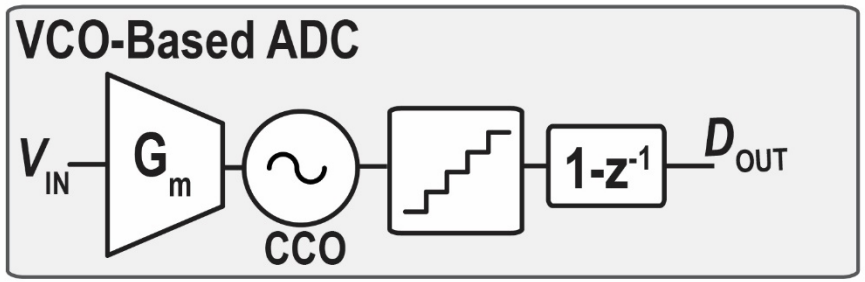
# Direct Digitization Front-ends

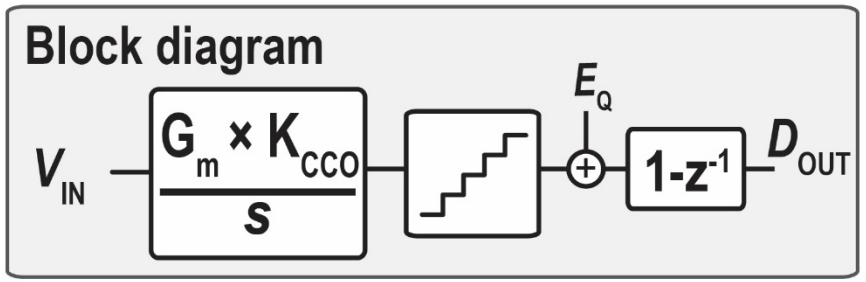


# VCO-based ADCs

## Pros:

- Continuous-time ΔΣ
- Open-loop noise-shaping
- High scalability with process




$$D_{OUT} = \underbrace{(G_m K_{CCO})}_{G_{ADC}} V_{IN} + E_Q(1-z^{-1})$$

noise shaping

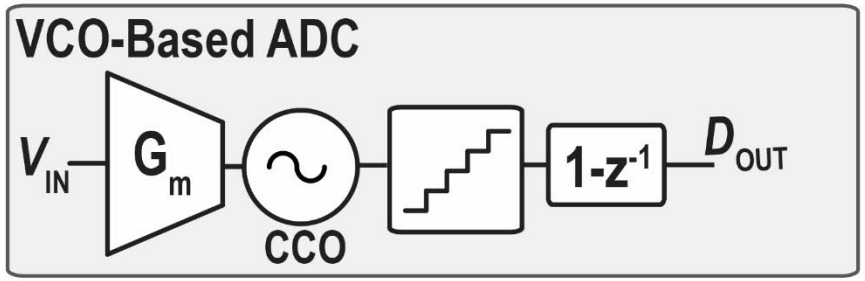
# VCO-based ADCs

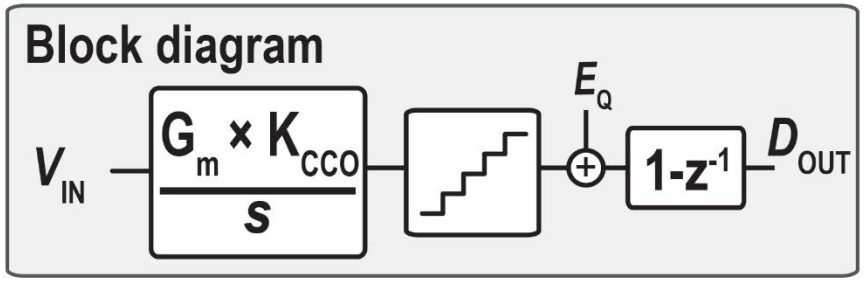
## Pros:

- Continuous-time ΔΣ
- Open-loop noise-shaping
- High scalability with process

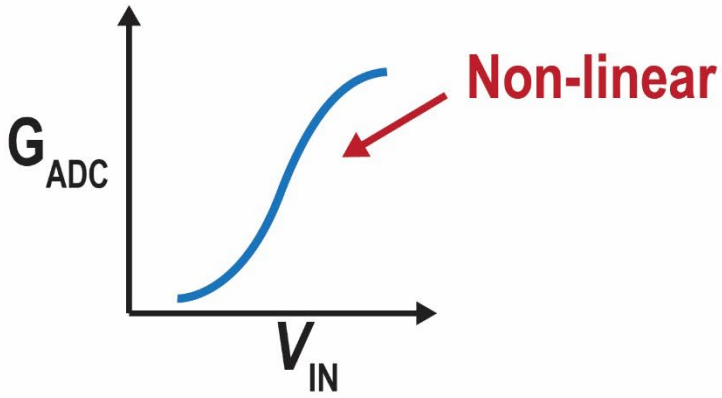
## Cons:

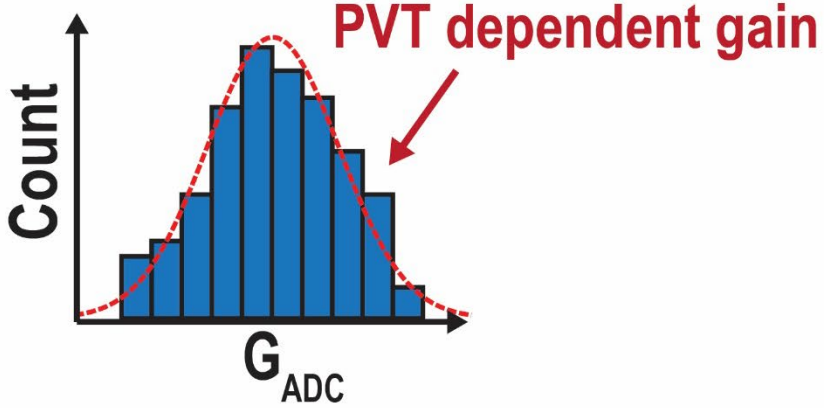
- Very non-linear
- PVT dependent gain
- Limited to 1st -order noise-shaping

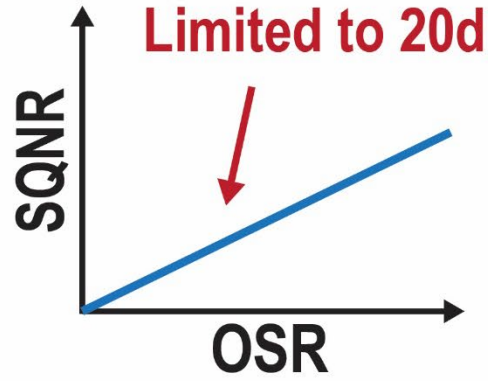


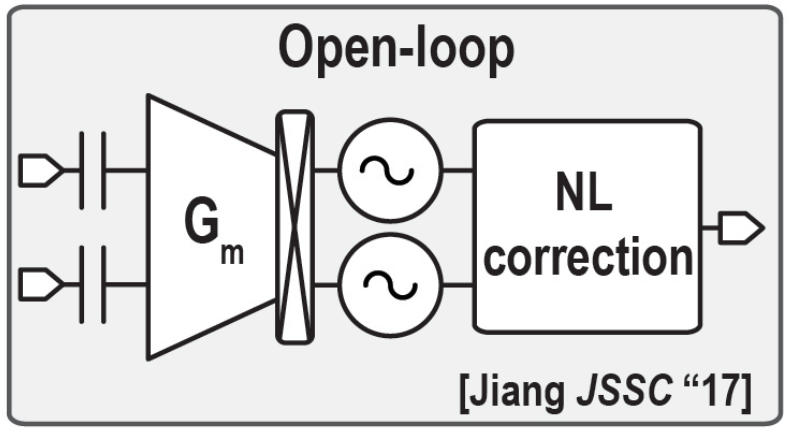

$$D_{OUT} = \underbrace{(G_m K_{CCO})}_{G_{ADC}} V_{IN} + E_Q(1-z^{-1})$$



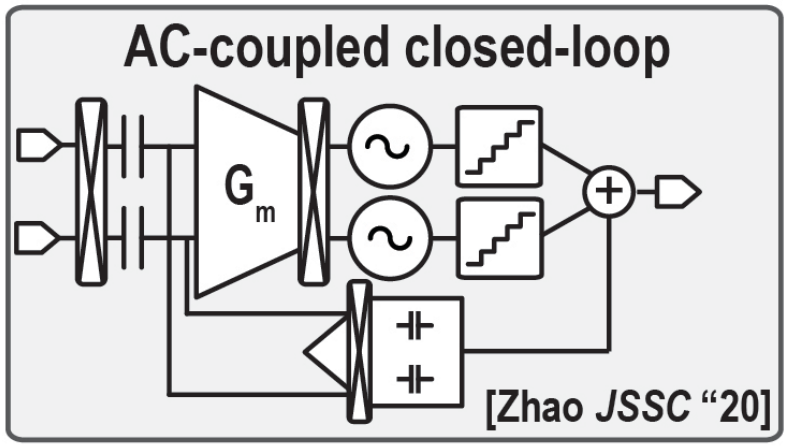



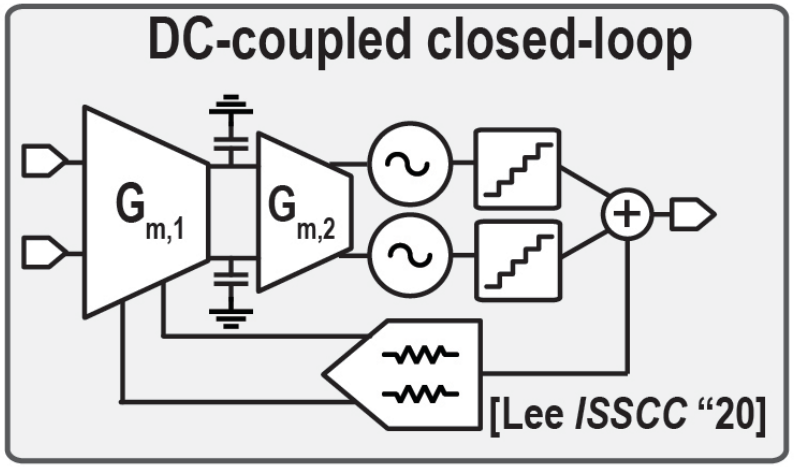
# VCO-based ADCs – Prior art




+ High $Z_{IN}$
+ Small area
- Limited input range and linearity



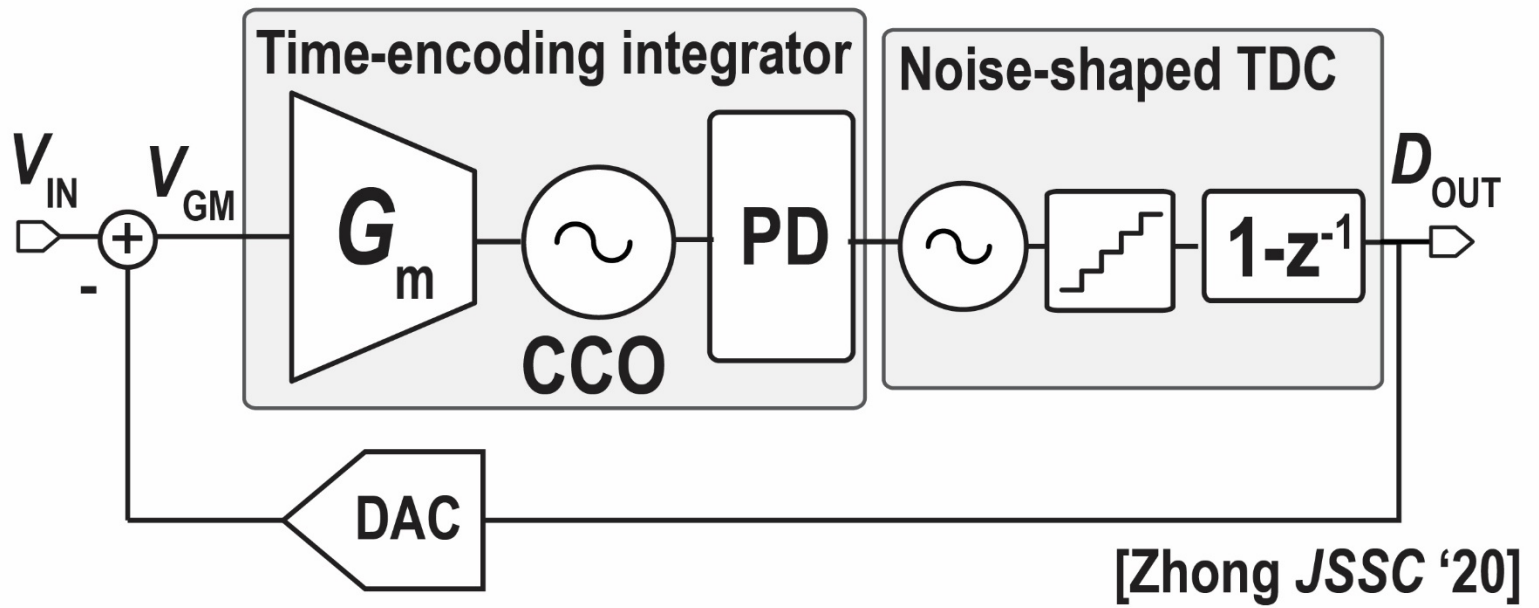

+ High linearity and input range
+ No 1/*f* noise
- Low $Z_{IN}$

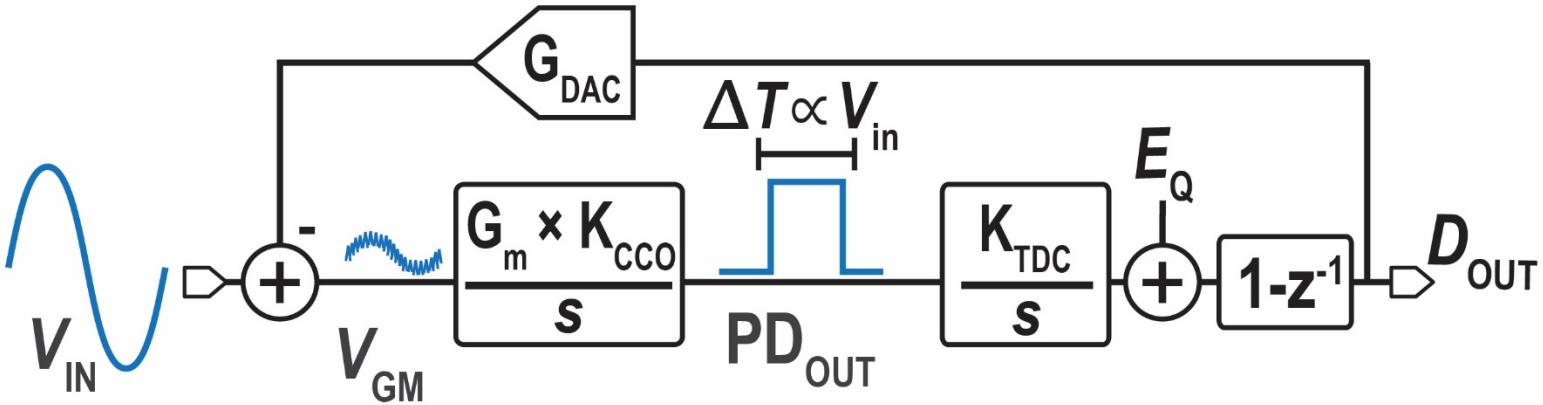



+ High $Z_{IN}$
+ 2nd-order noise-shaping
- Flicker noise sensitive
- Common-mode sensitive

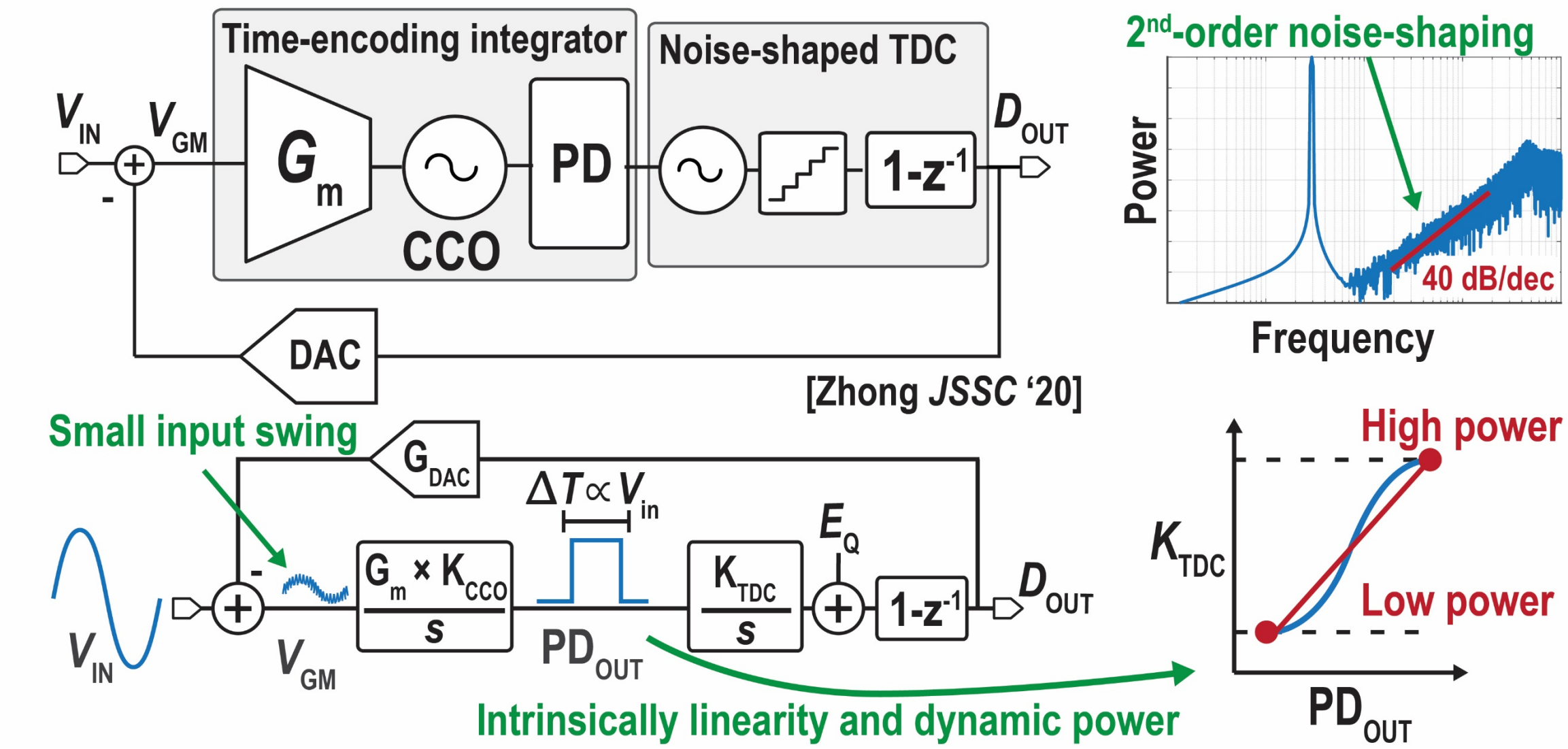
# System design

# 2nd order ADC - Core concept

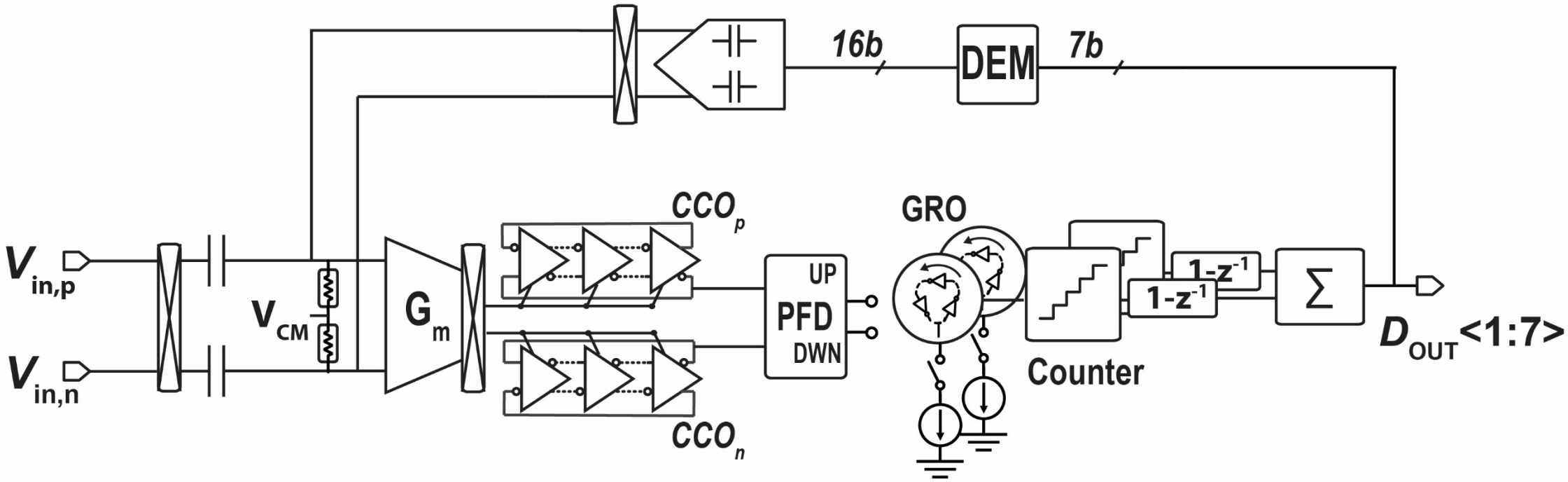


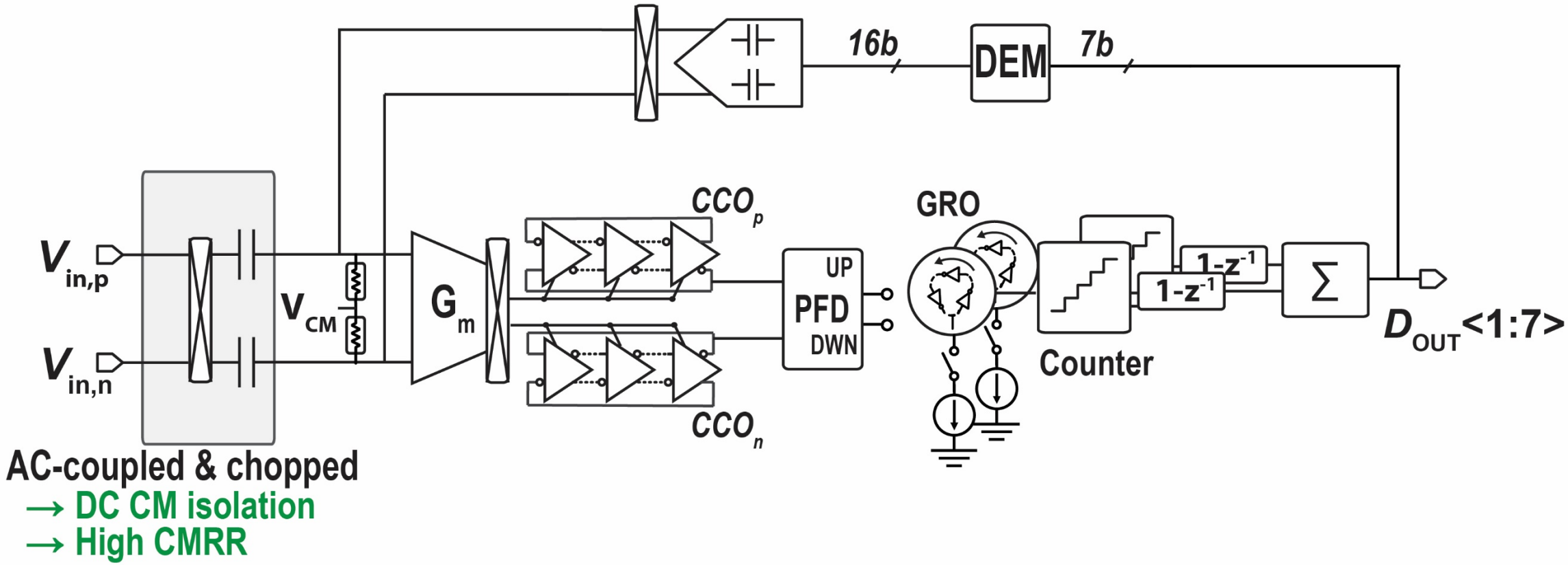
# 2nd order ADC - Benefits



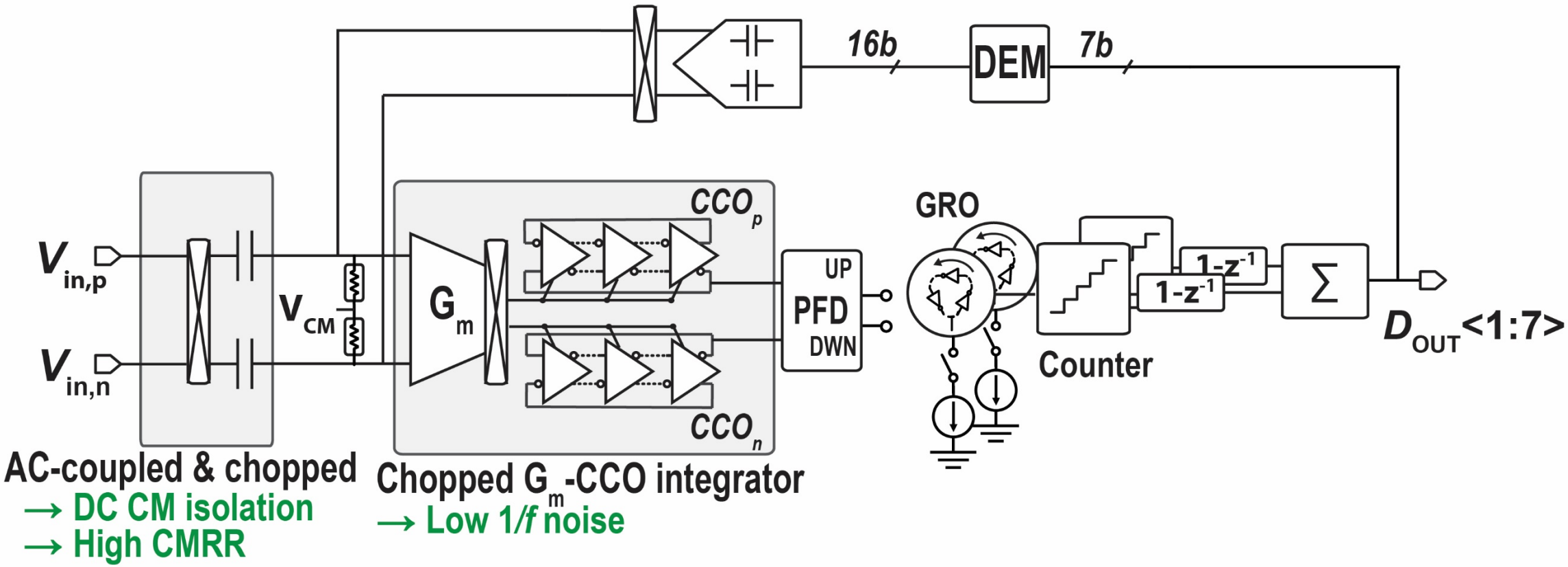
# “Basic” front-end implementation



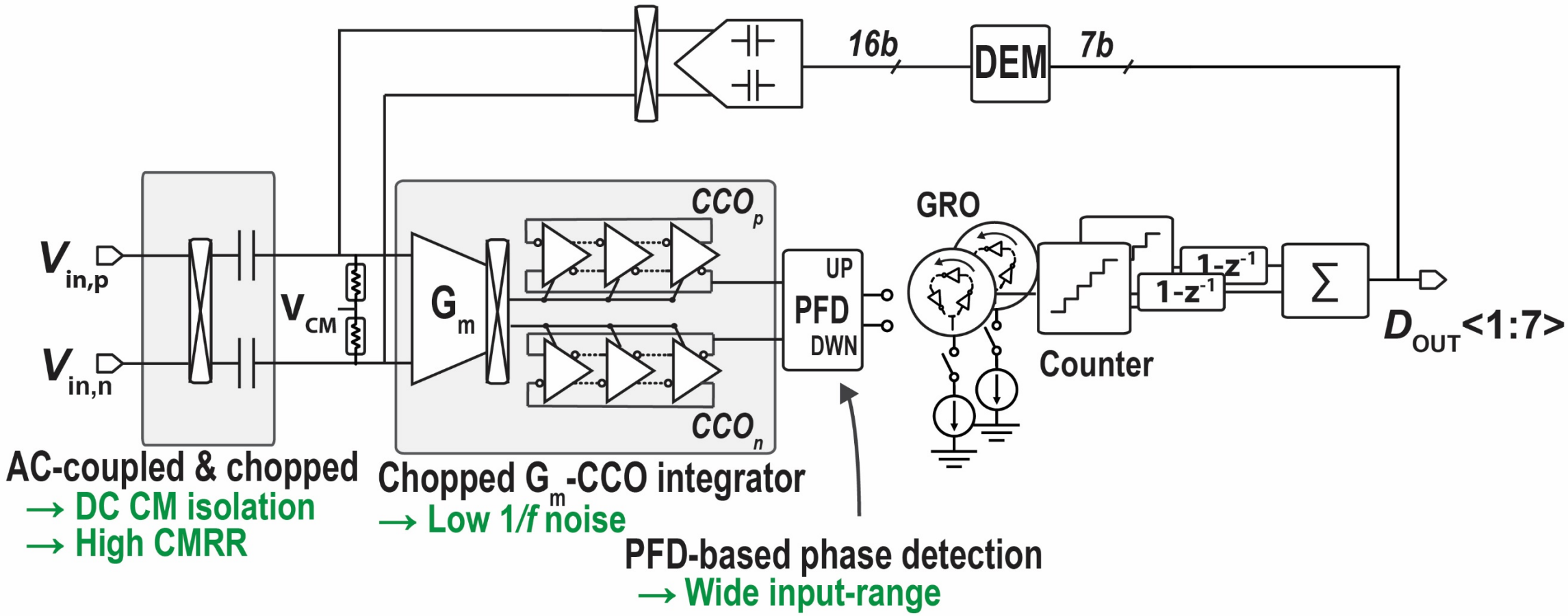
# “Basic” front-end implementation



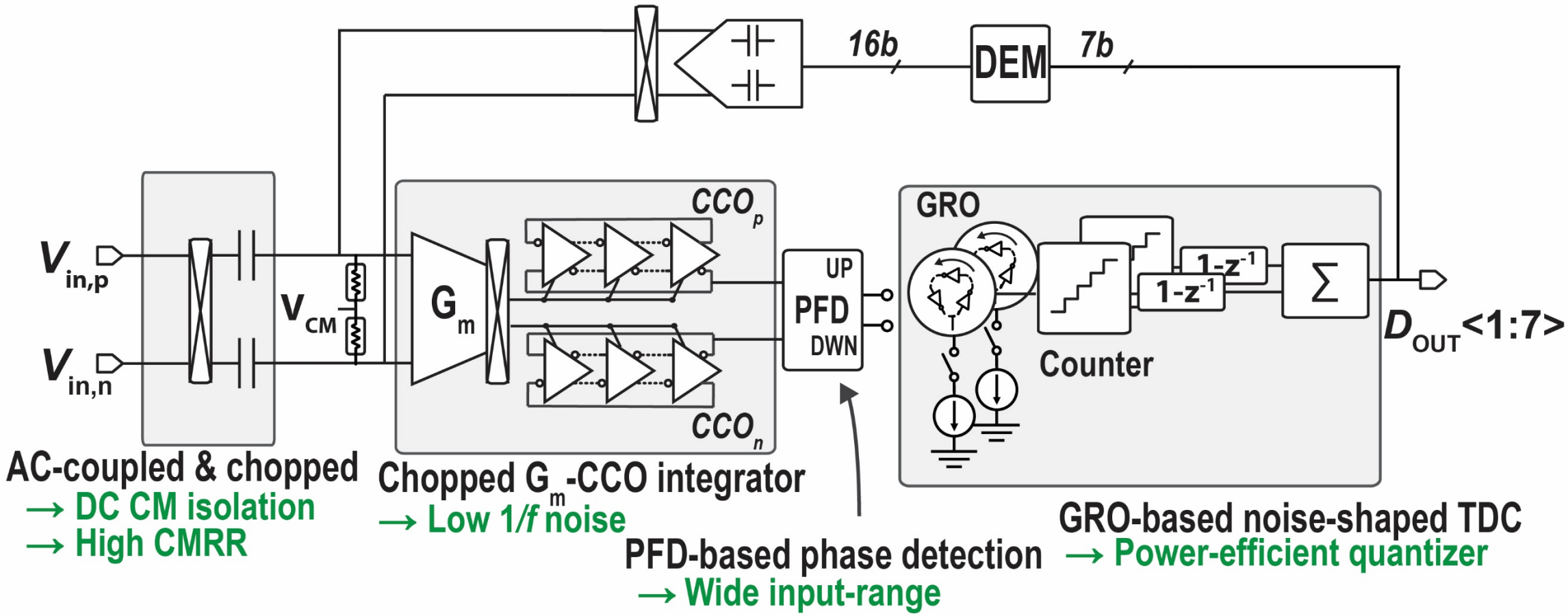
# “Basic” front-end implementation



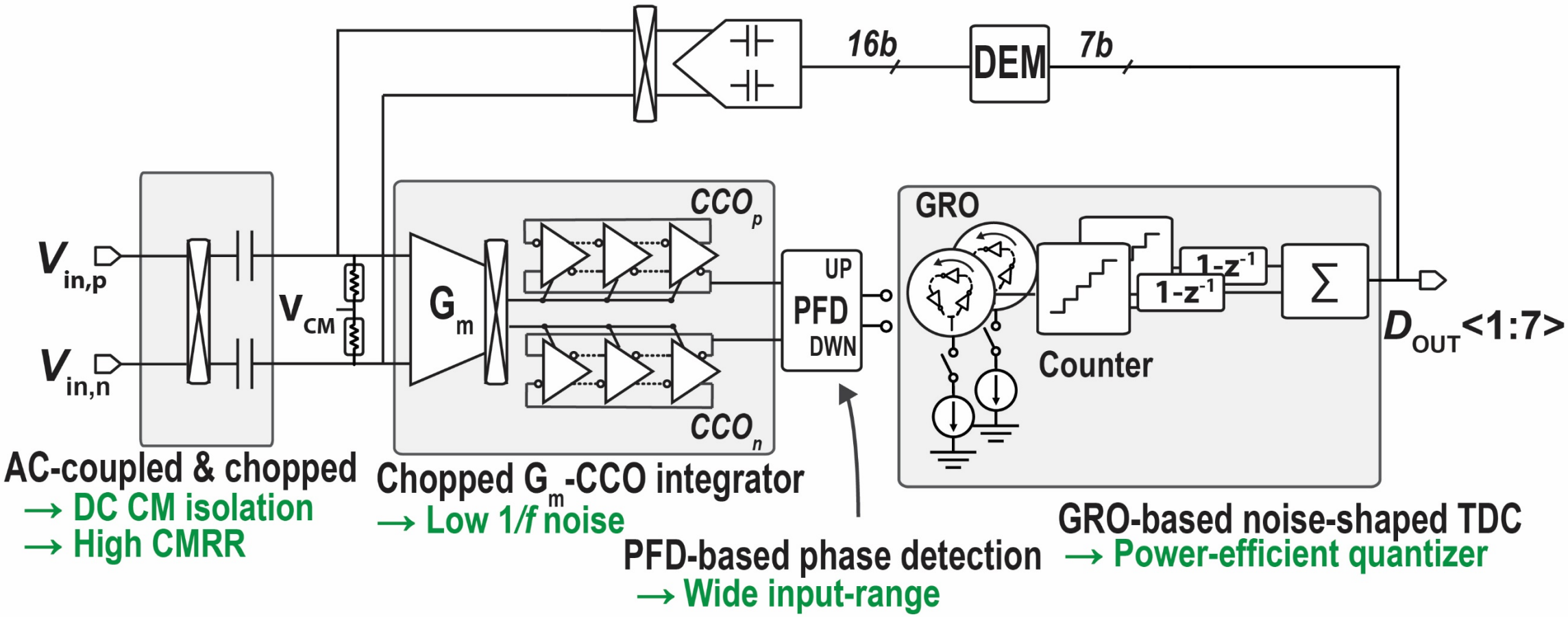
# “Basic” front-end implementation



# “Basic” front-end implementation

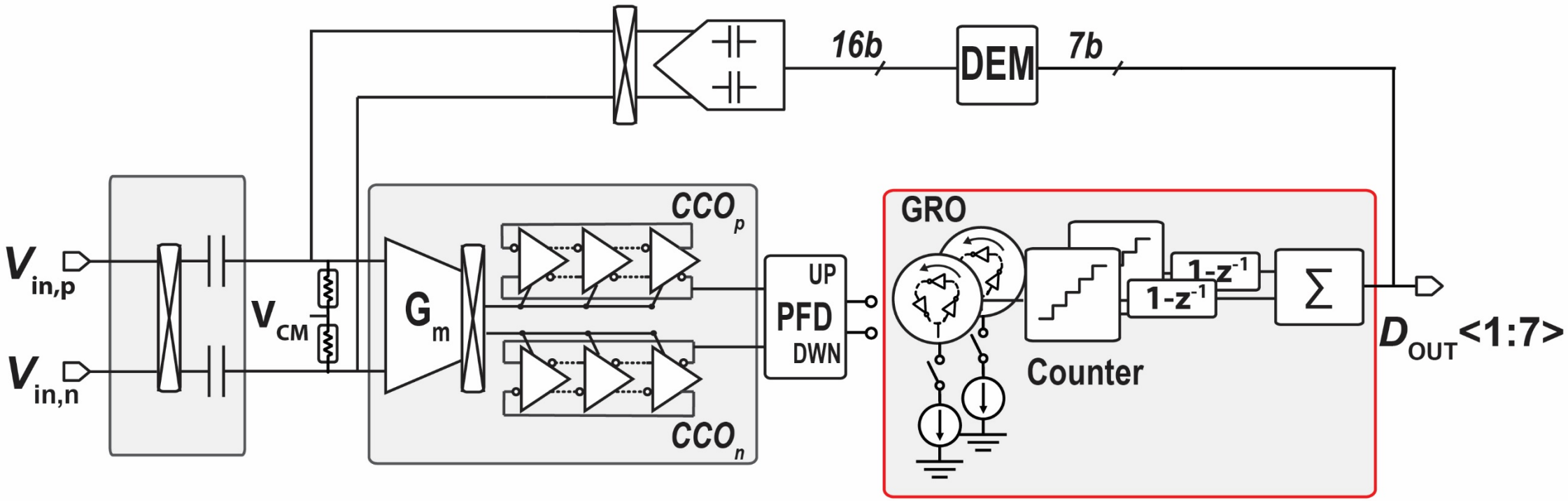


# “Basic” front-end implementation




**But, there are a few issues with this architecture…**

# Issue #1: Gated Ring Oscillator quantizer

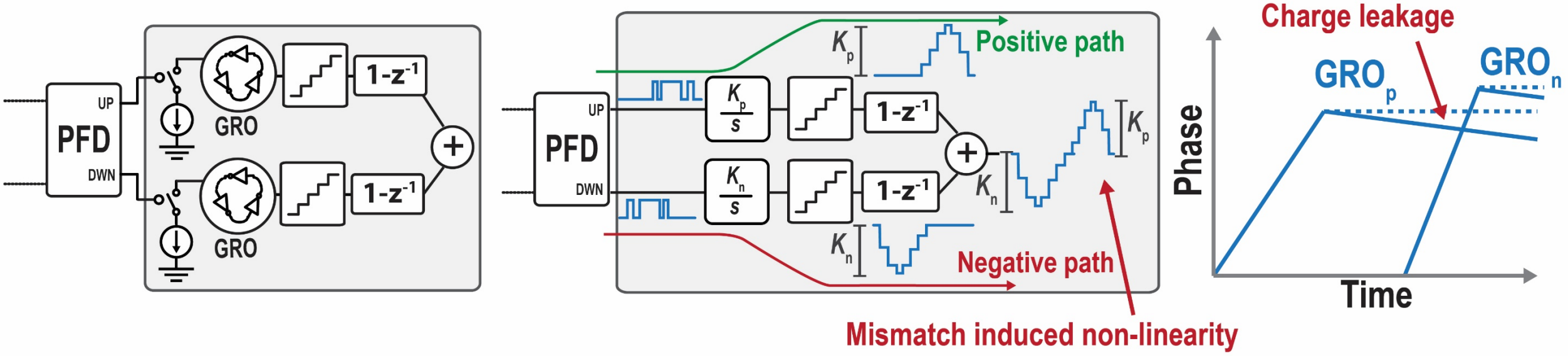



**GRO-based noise-shaped TDC**

→ GRO mismatch induces non-linearity

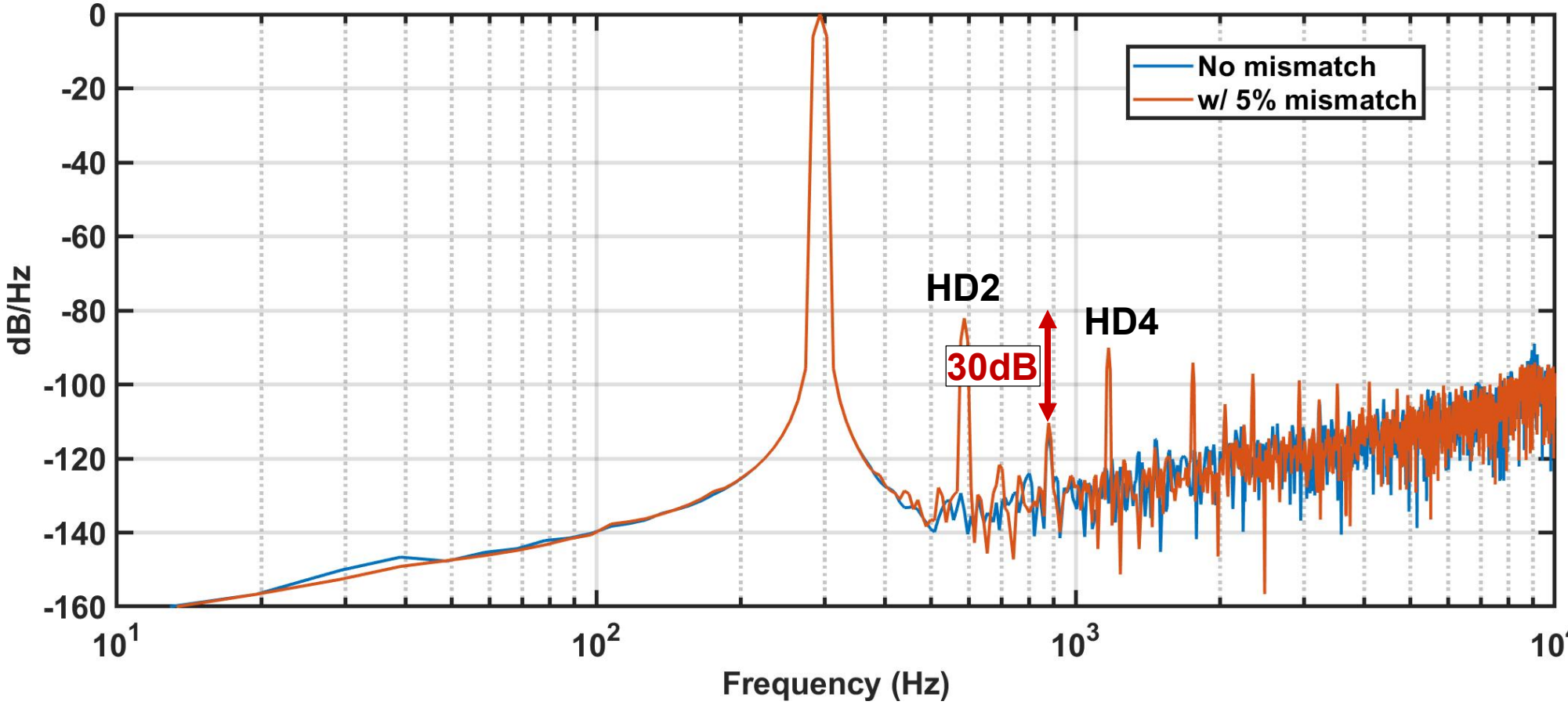
→ GRO requires long hold time

# Issues with GRO-based quantizer




- Path mismatches causes even-order harmonics
- Long hold time leads to charge leakage

# ADC spectrum with GRO mismatch




**Typical mismatch $\sigma = 5\%$ degrade SFDR by > 30 dB**

# Issues with GRO-based quantizer

## Two issues due to GRO-based quantization:

1. Mismatches cause SFDR degradation
2. Inactive GRO require to hold charge for long period of time

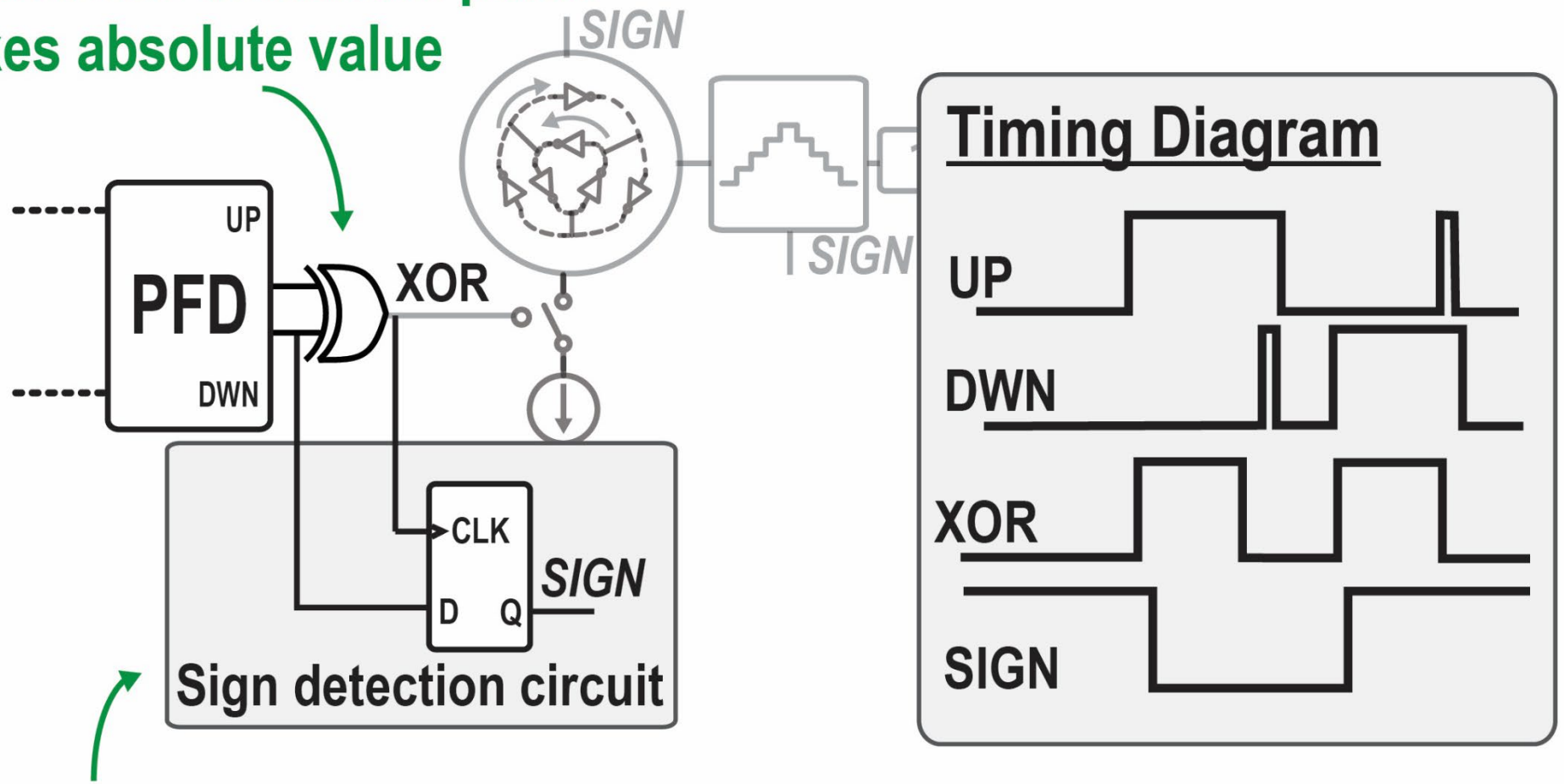
## Two innovations to solve these issues:

1. Sign feed-forwarding from the PFD enabling path merging
2. Gated-inverted ring-oscillator (GIRO) improving the matching

# PFD Sign Detection

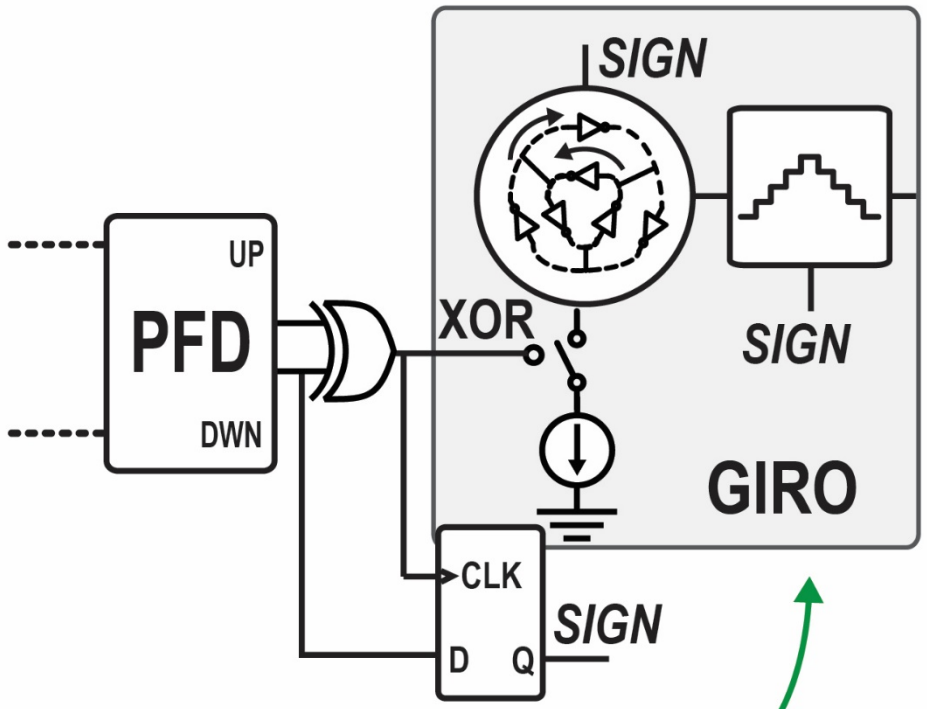
Eliminates deadband pulse

Takes absolute value

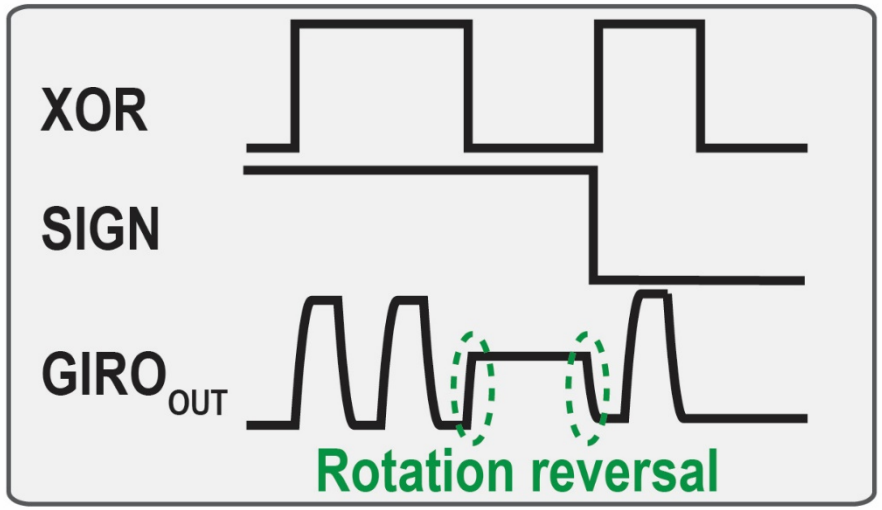



Detects and feedforwards the signal polarity

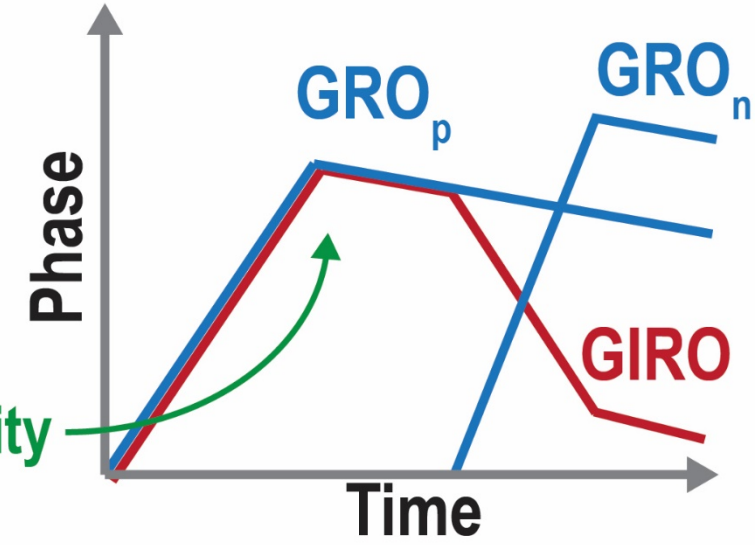
# GIRO-based quantizer



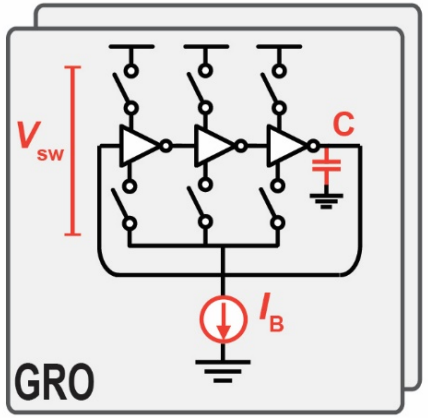

Pseudo-differential path merged




GIRO active on both polarity

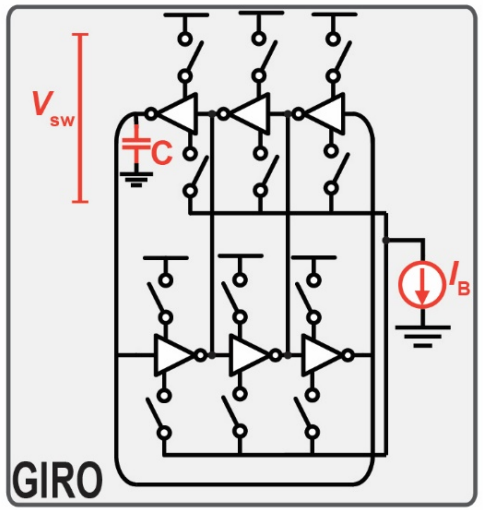


# Quantizer mismatch comparison




Typical path mismatch σ ~ 5%

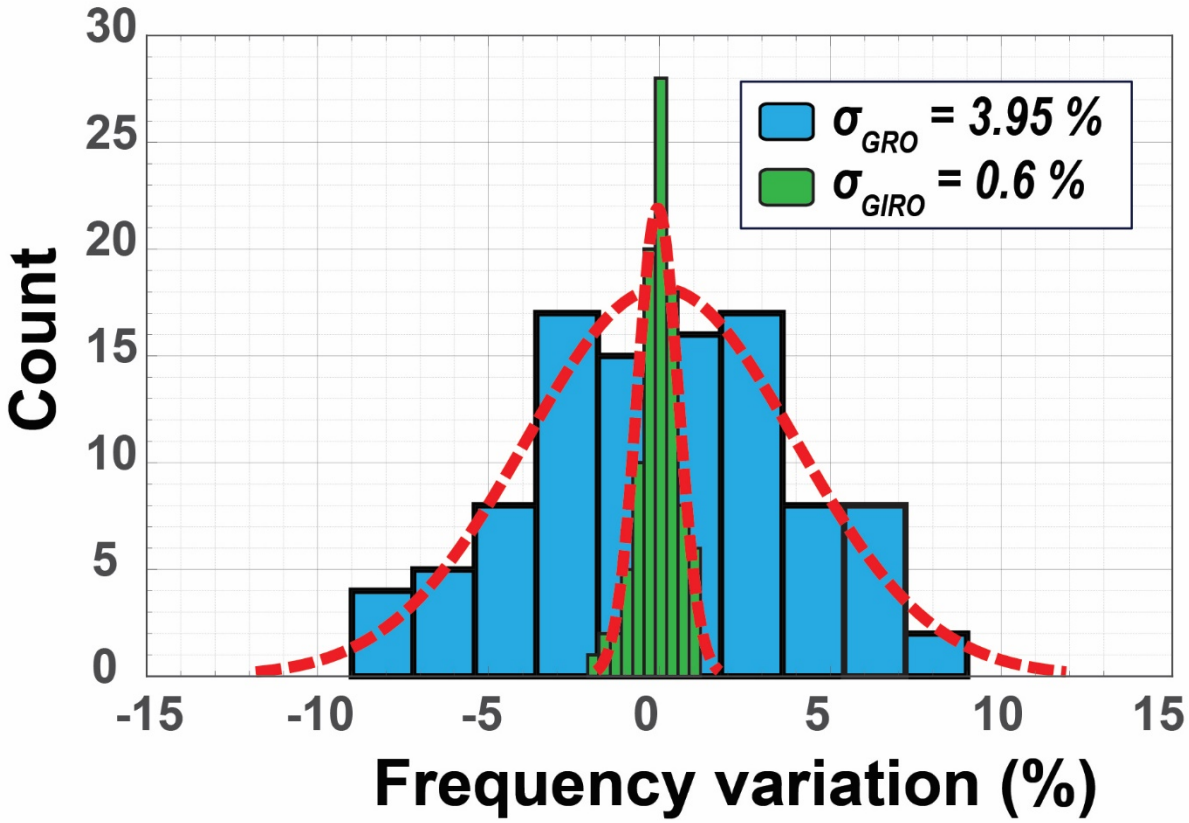
- Inactive path required to hold state for long period (ms)
- Path matching affected by $I_B$, $C$, $V_{sw}$
- Minimum layout distance 10s $\mu$m



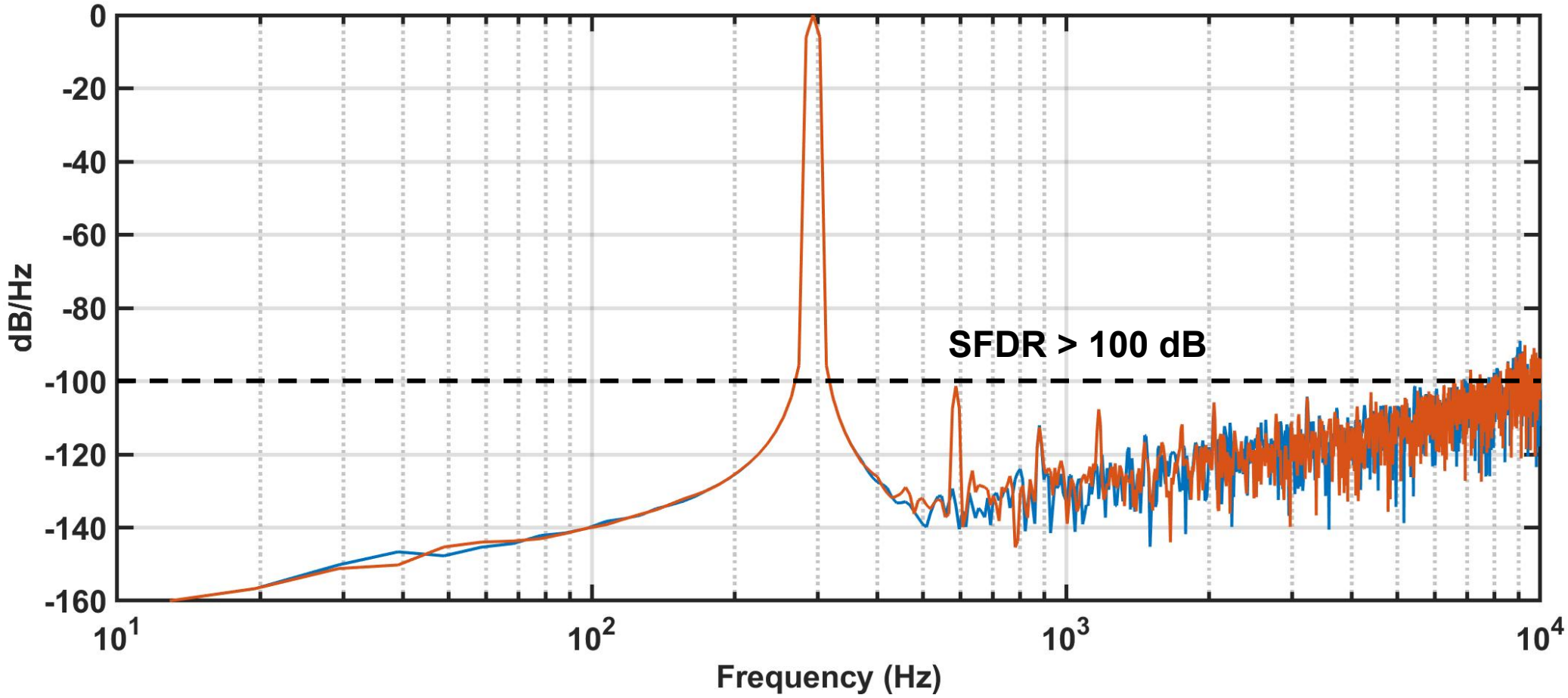

Typical path mismatch σ ~ 0.5%

+ Always active
+ Path matching only affected by $V_{sw}$
+ Adjacent layout

$V_{sw}$ : Voltage swing
$I_B$ : Bias current
C : Node capacitance

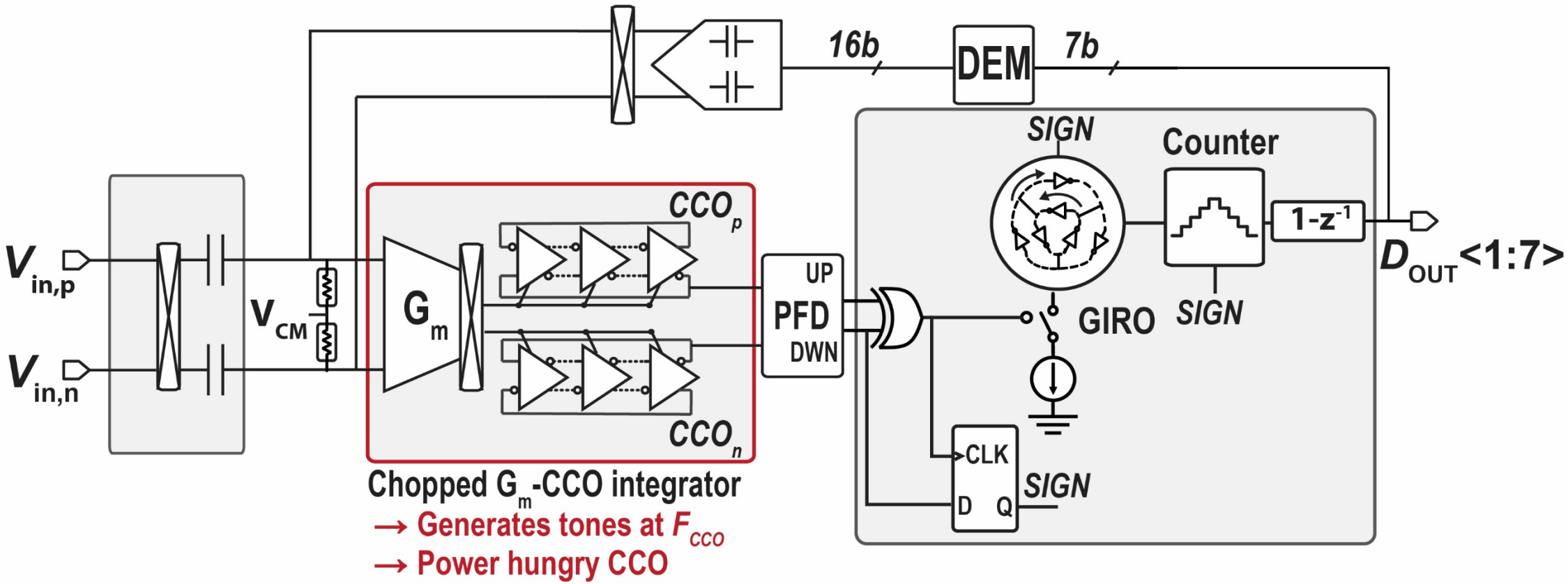


# ADC spectrum with GIRO mismatch

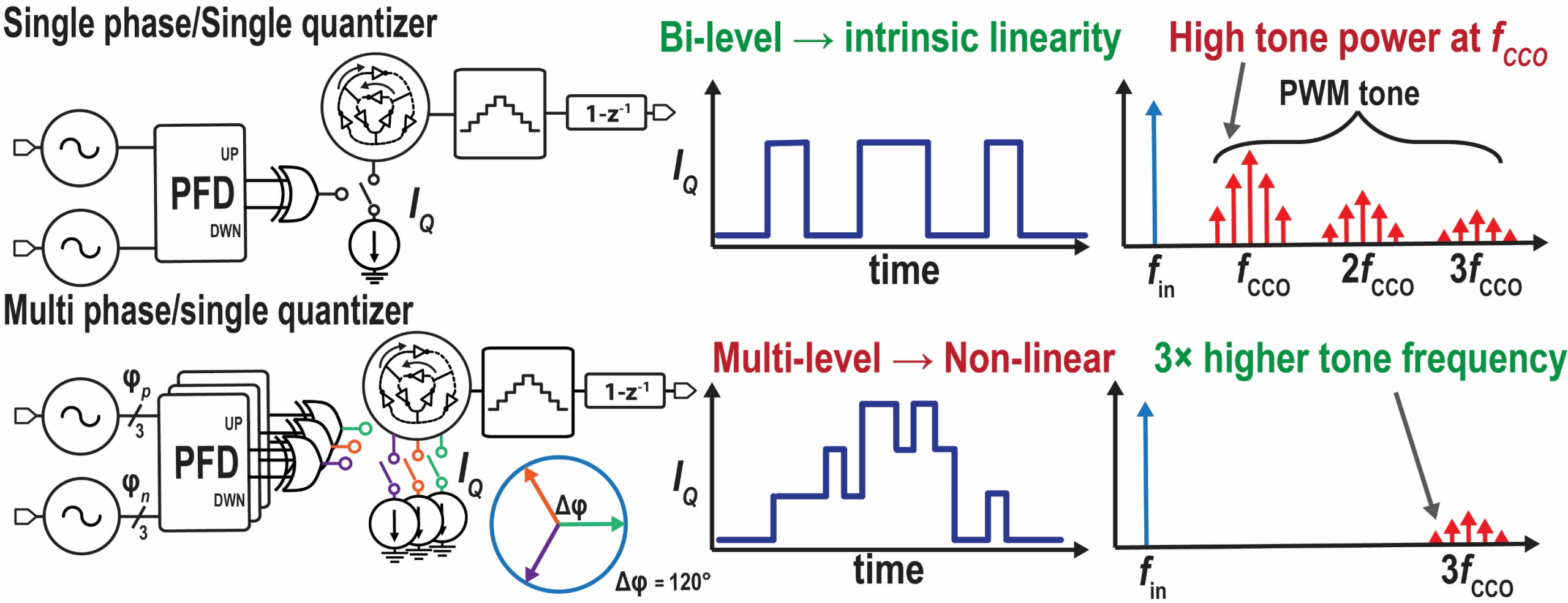



**Typical mismatch $\sigma = 0.5\%$ degrades SFDR by <10 dB**

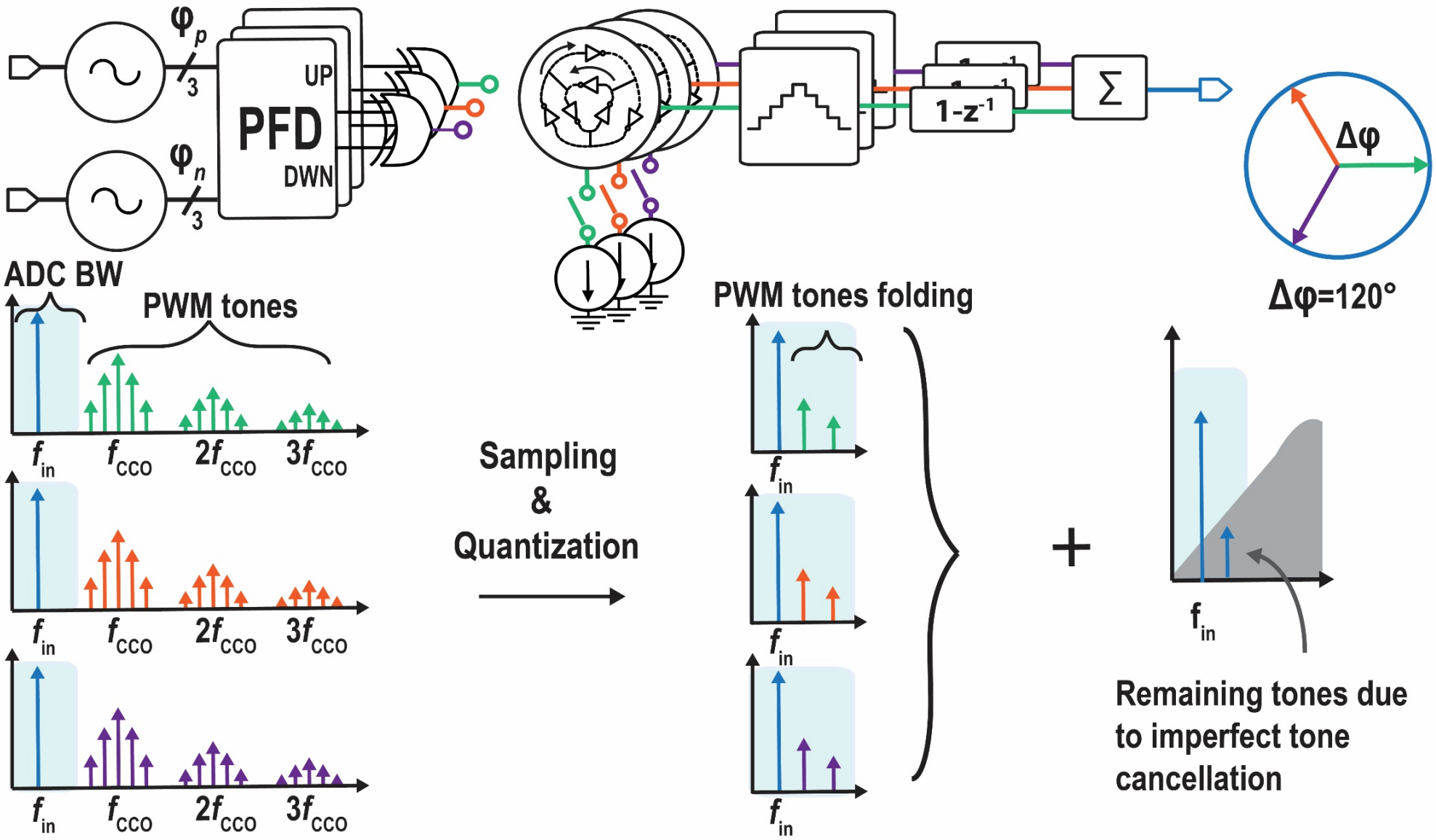
# Issue #2: PWM Encoding



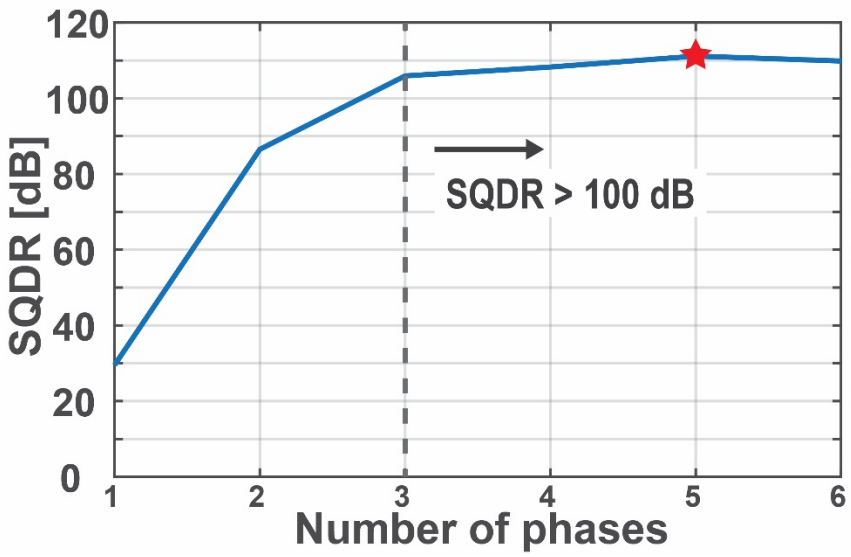
# PWM quantizer architectures

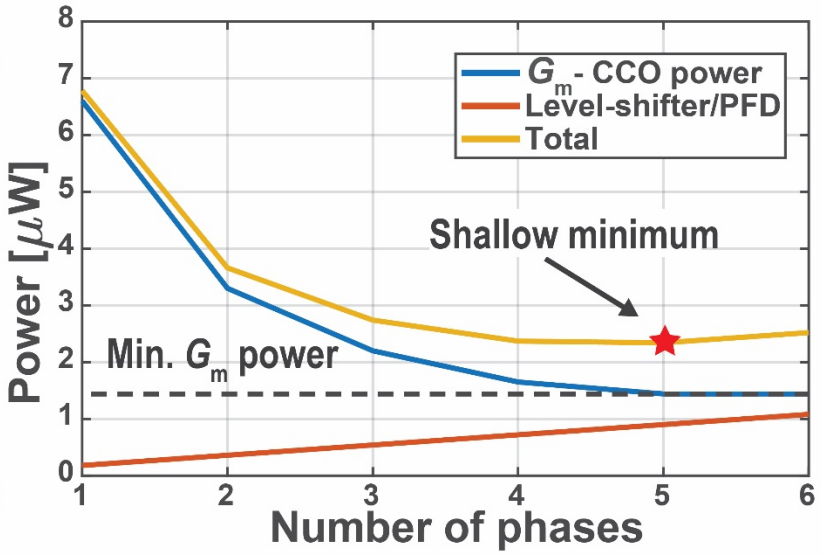


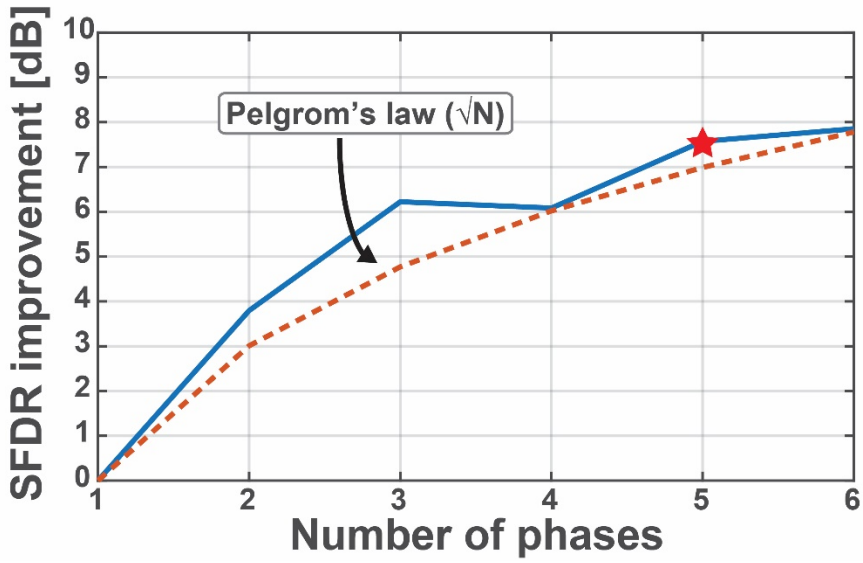
# Multi-Phase/Multi Quantizers



# Number of Phases Tradeoff

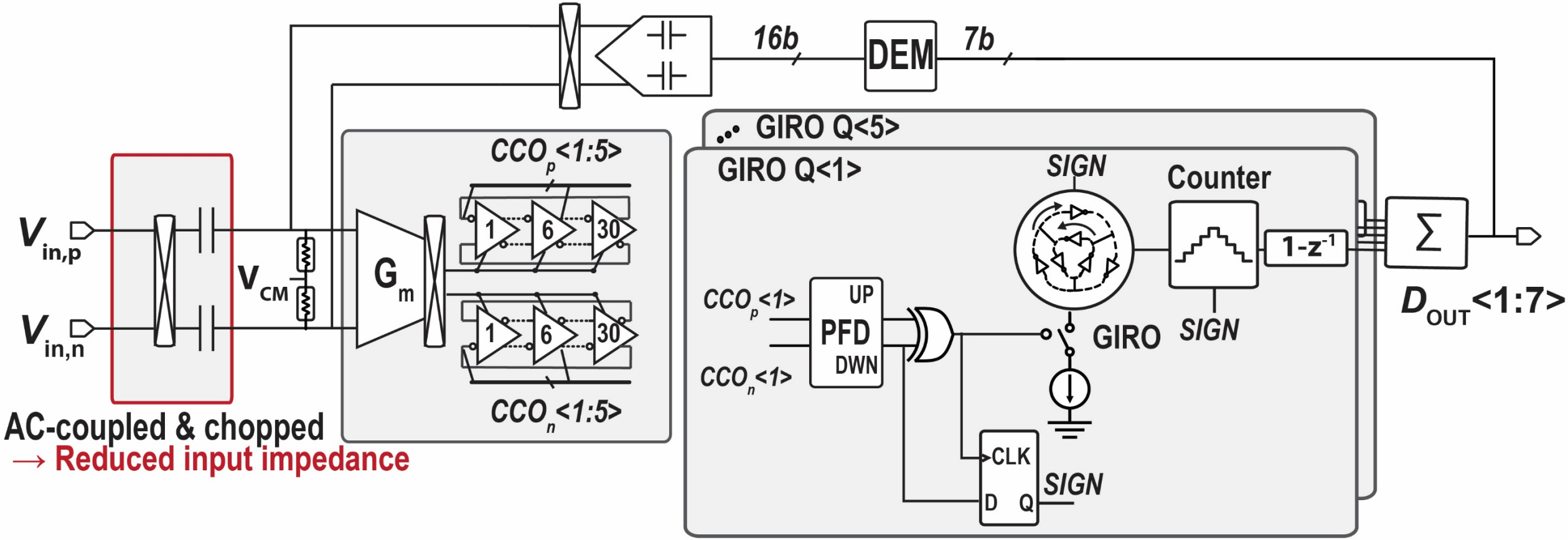


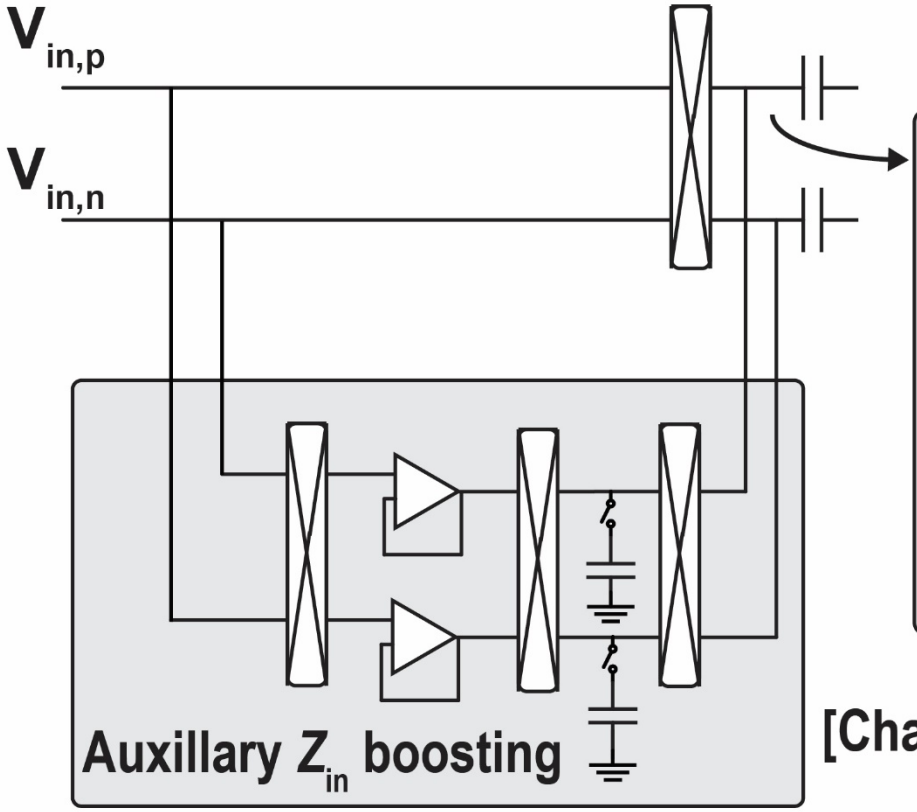



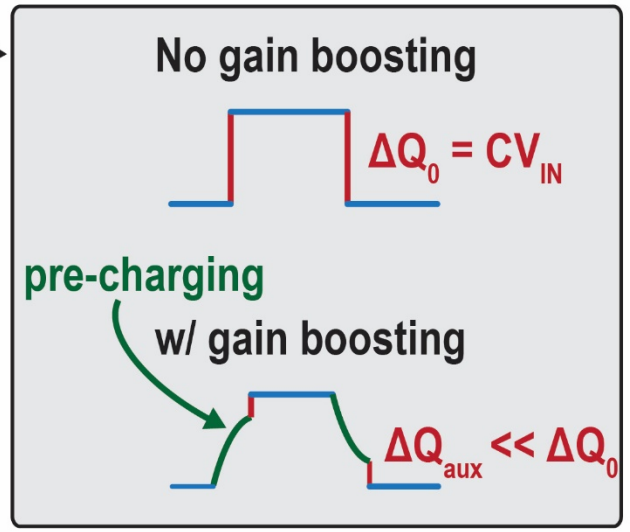

**5 phases selected from this analysis**

# Issue #3: Low Input-Impedance

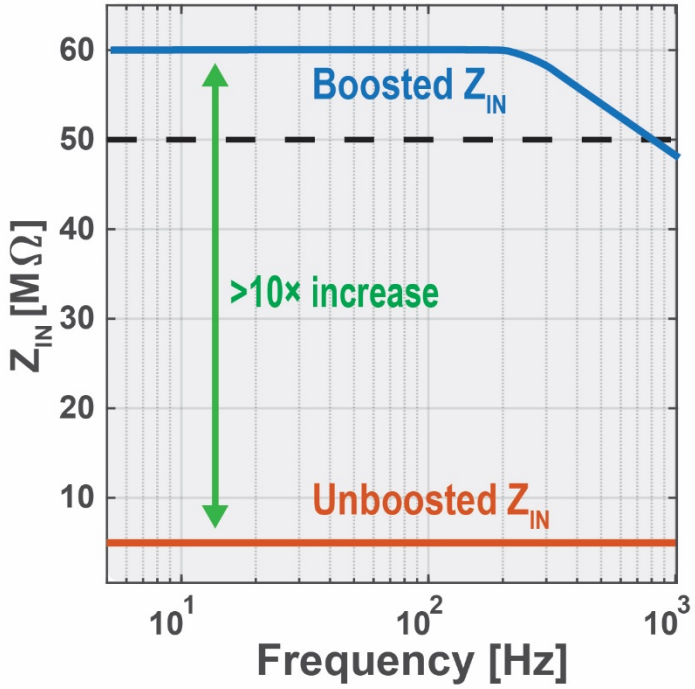


# Input-Impedance Boosting



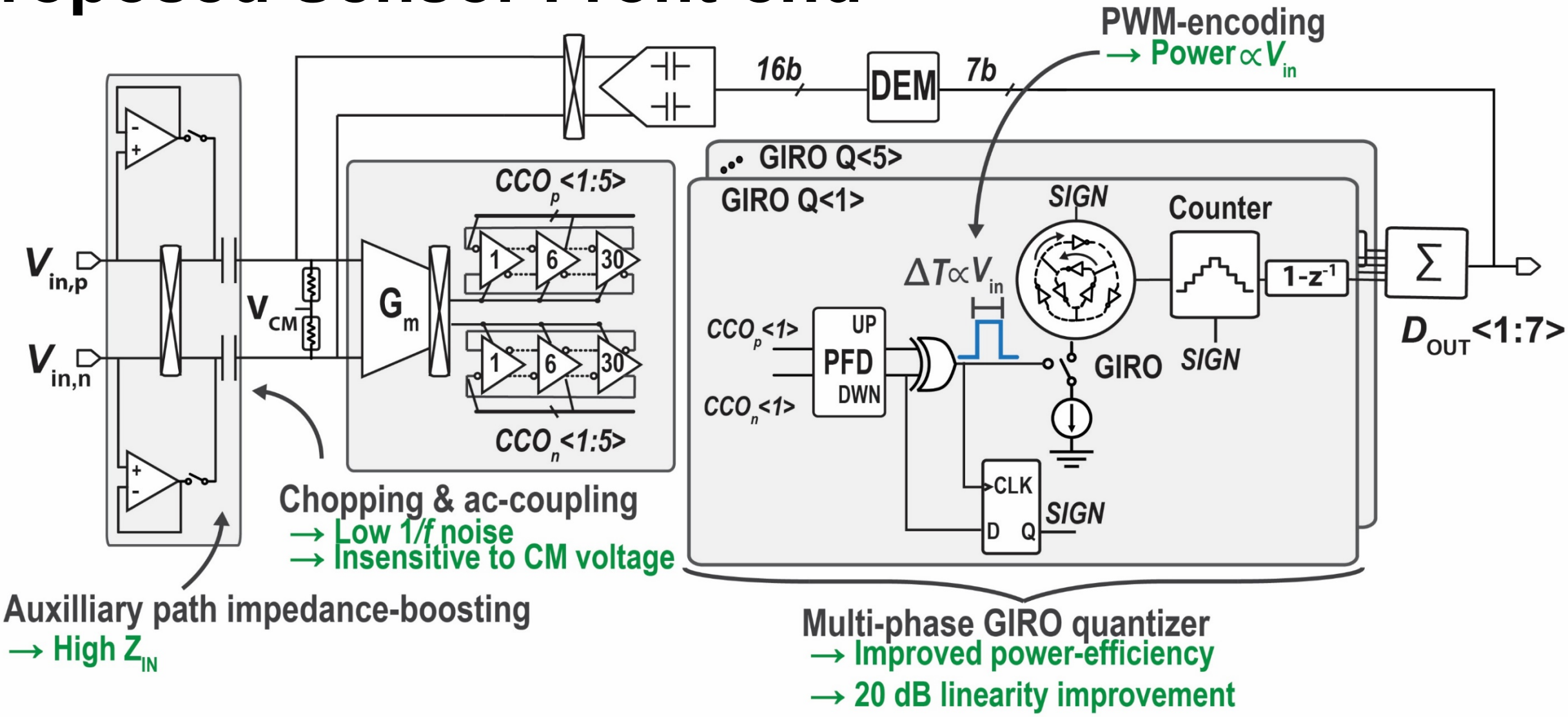

[Chandrakumar JSSC '18]




$$Z_{IN} = \frac{1}{2f_{chop}C_{in}}$$

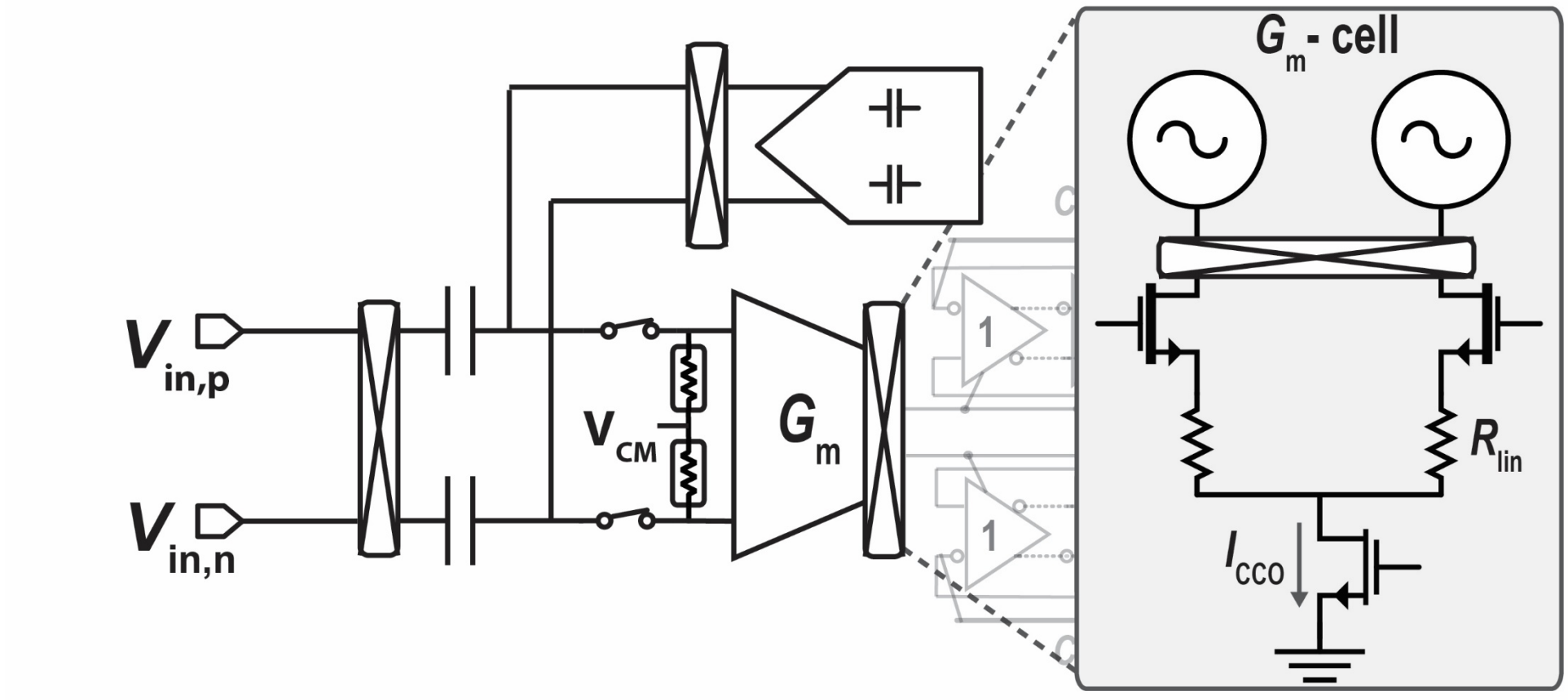
**Concept used in CCIAs to boost the input impedance**

# Proposed Sensor Front-end



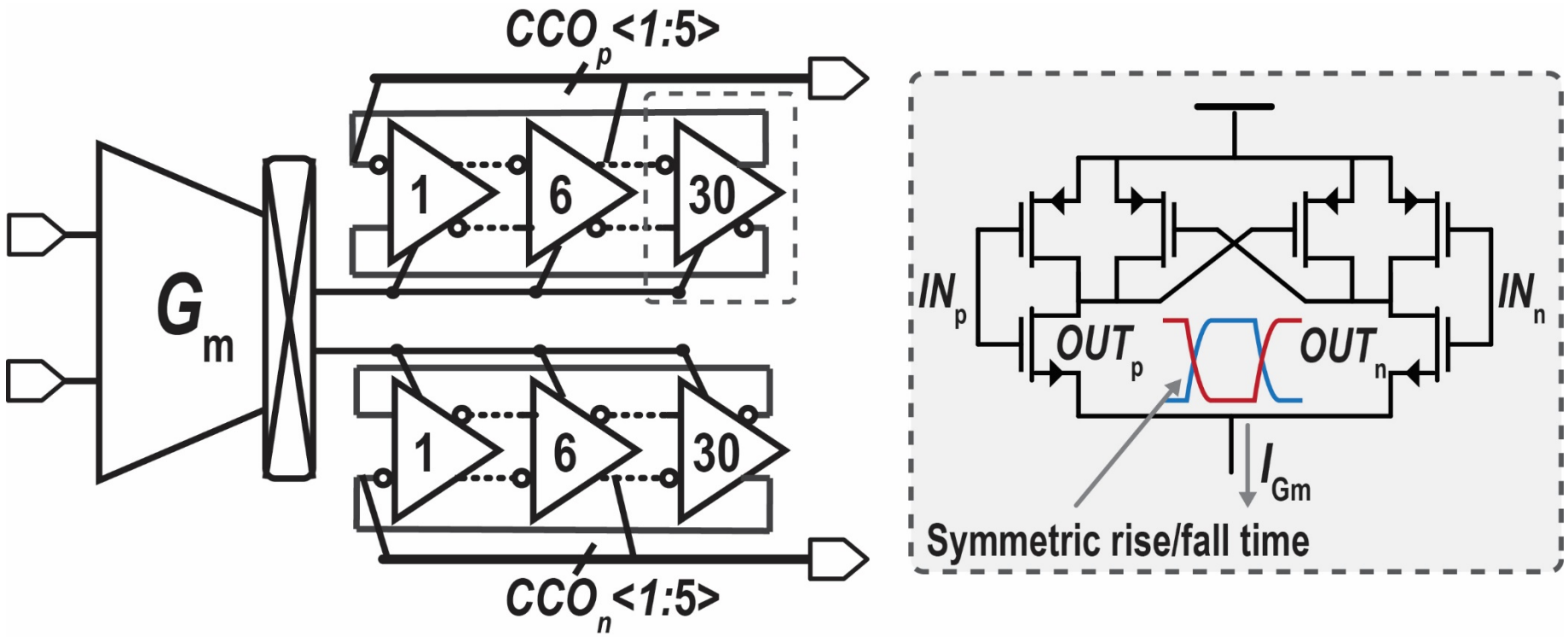
# Circuit implementation

# $G_m$-cell design



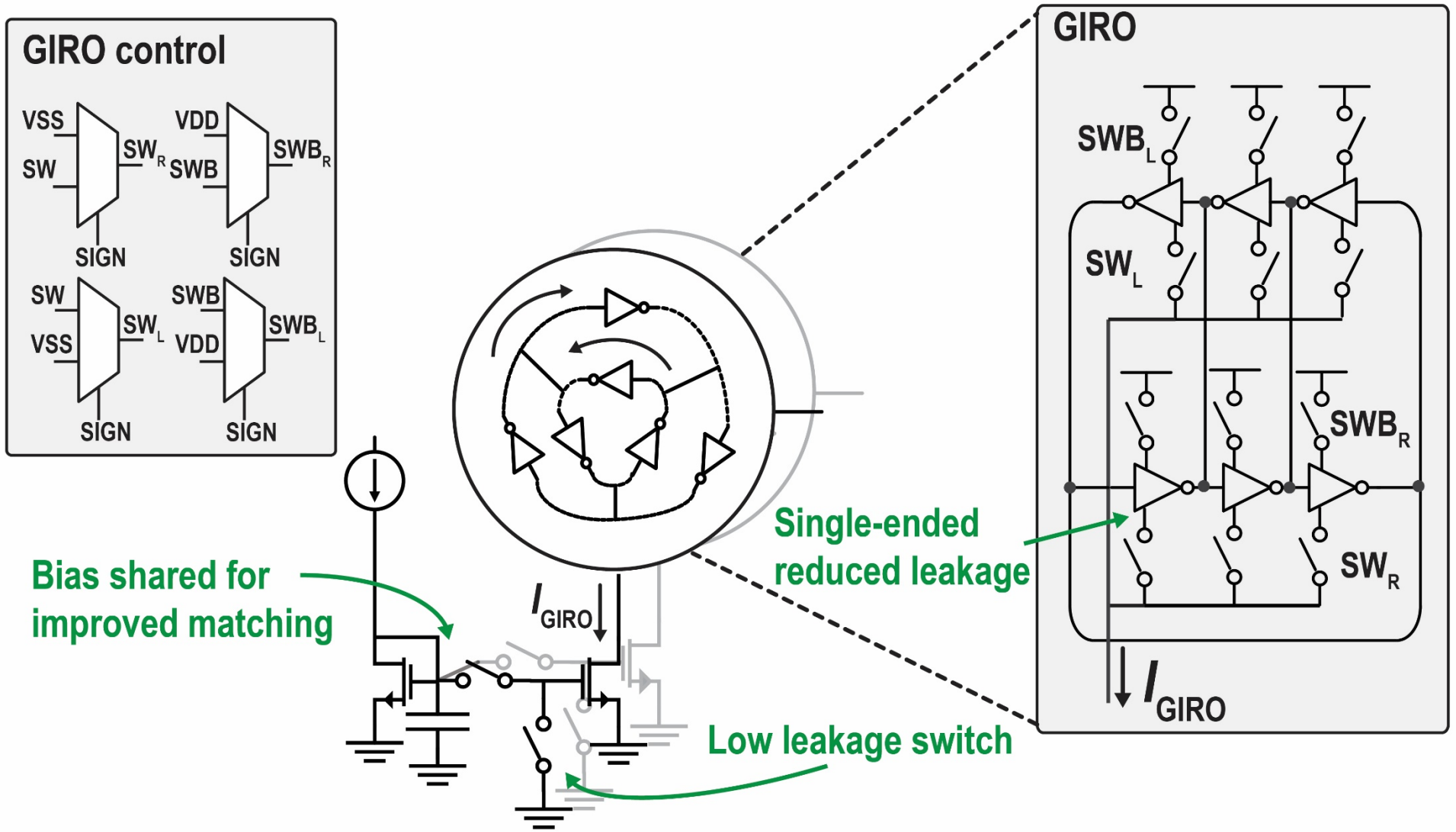

- Source degenerated $G_m$-cell for linearity
- Thick-gate device to avoid common-mode drift

# CCO Design



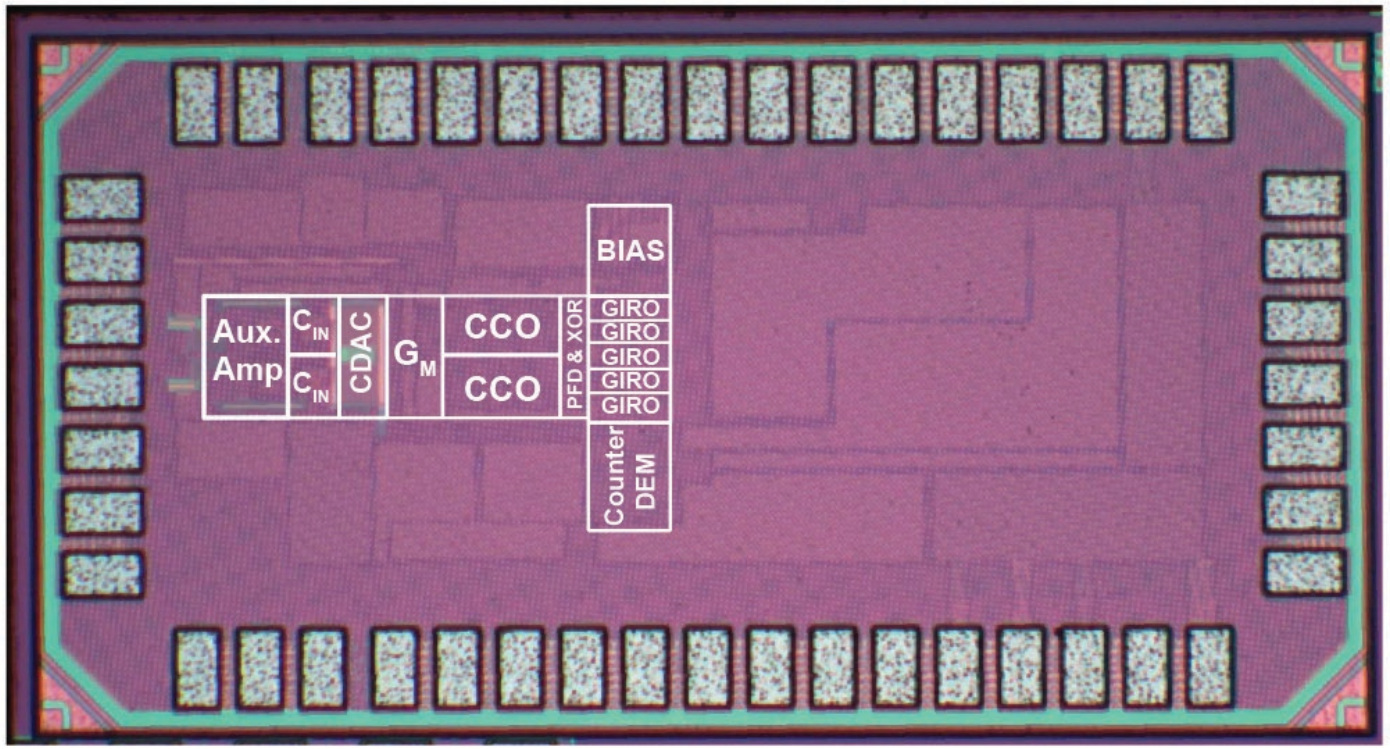

- **Differential stages with PMOS cross-coupling**
- **30 stages tapped every 6 nodes**
  - Equidistant phase-tapping around $2\pi$

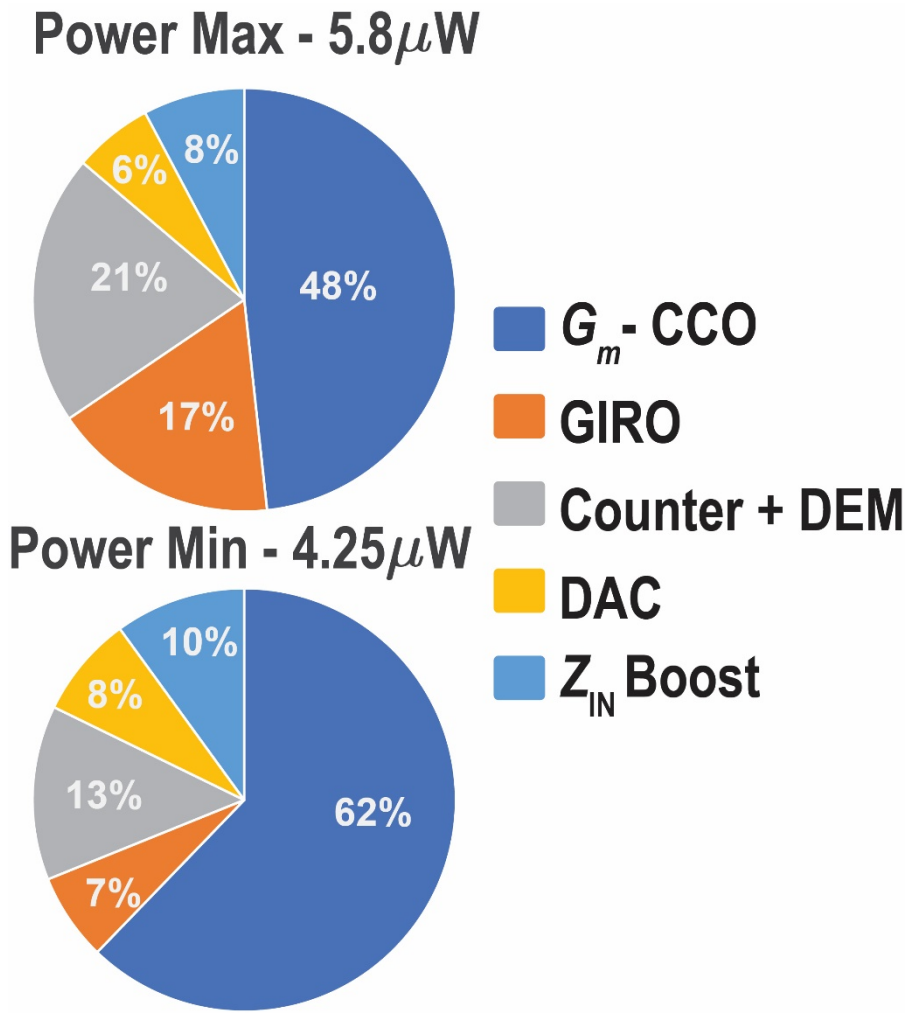
# GIRO Design



# Measurement Results

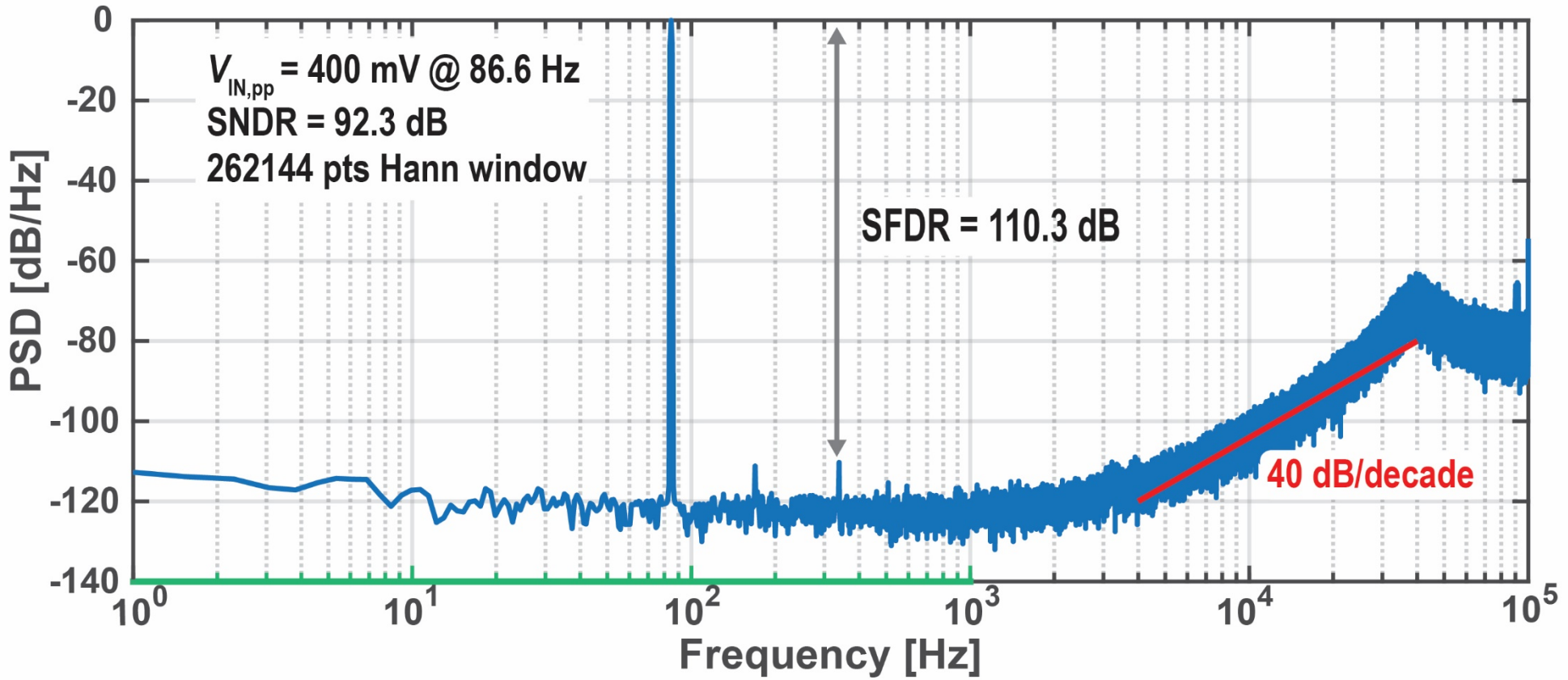
# Die Micrograph & Power breakdown



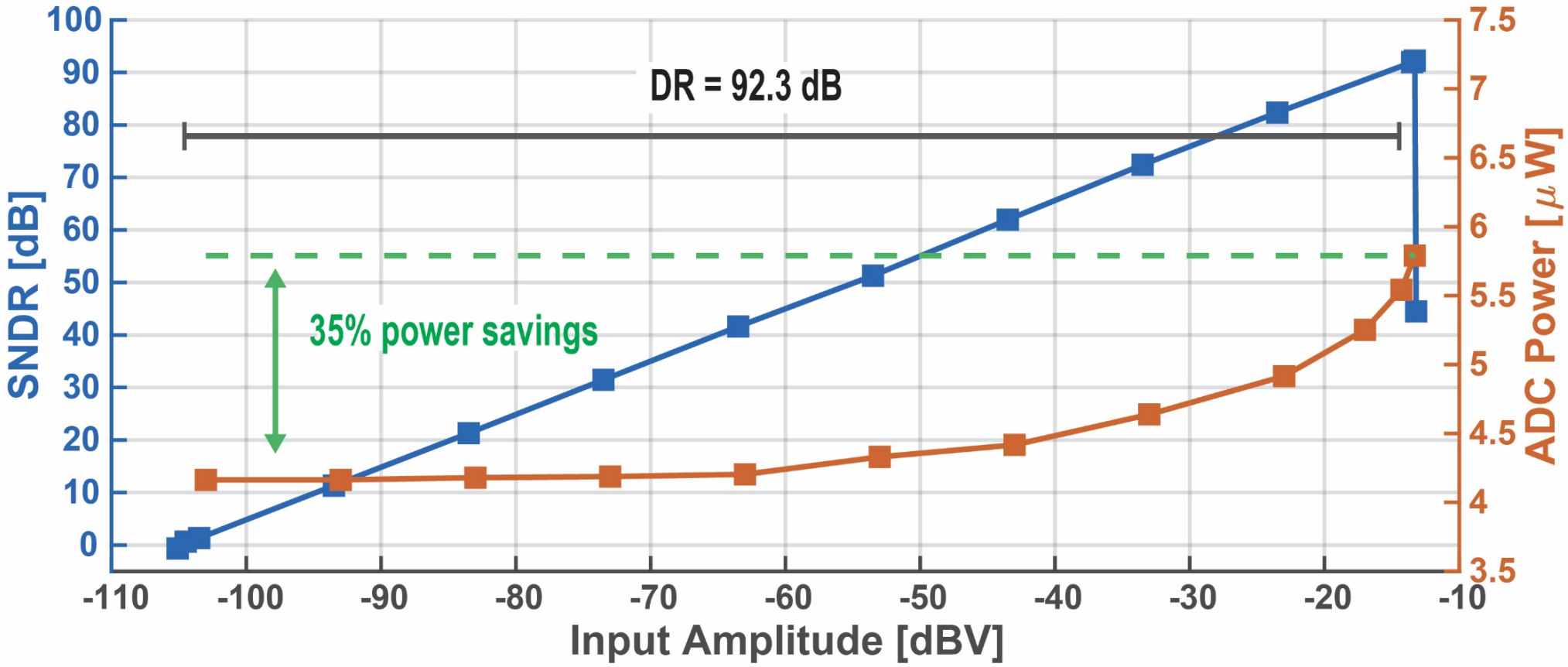




## Chip designed in TSMC65 LP with active area 0.075 mm$^2$

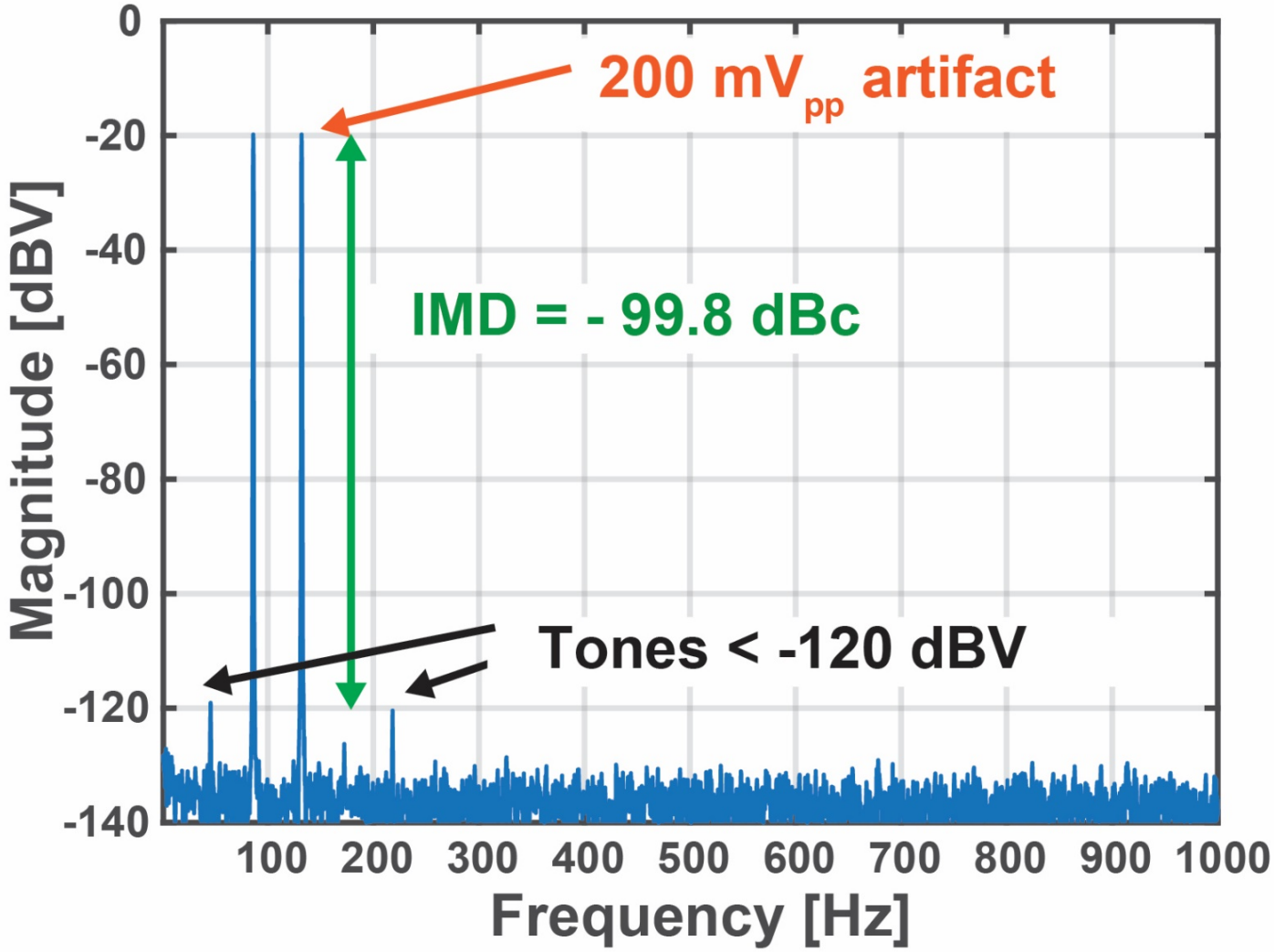
# Measured SNDR



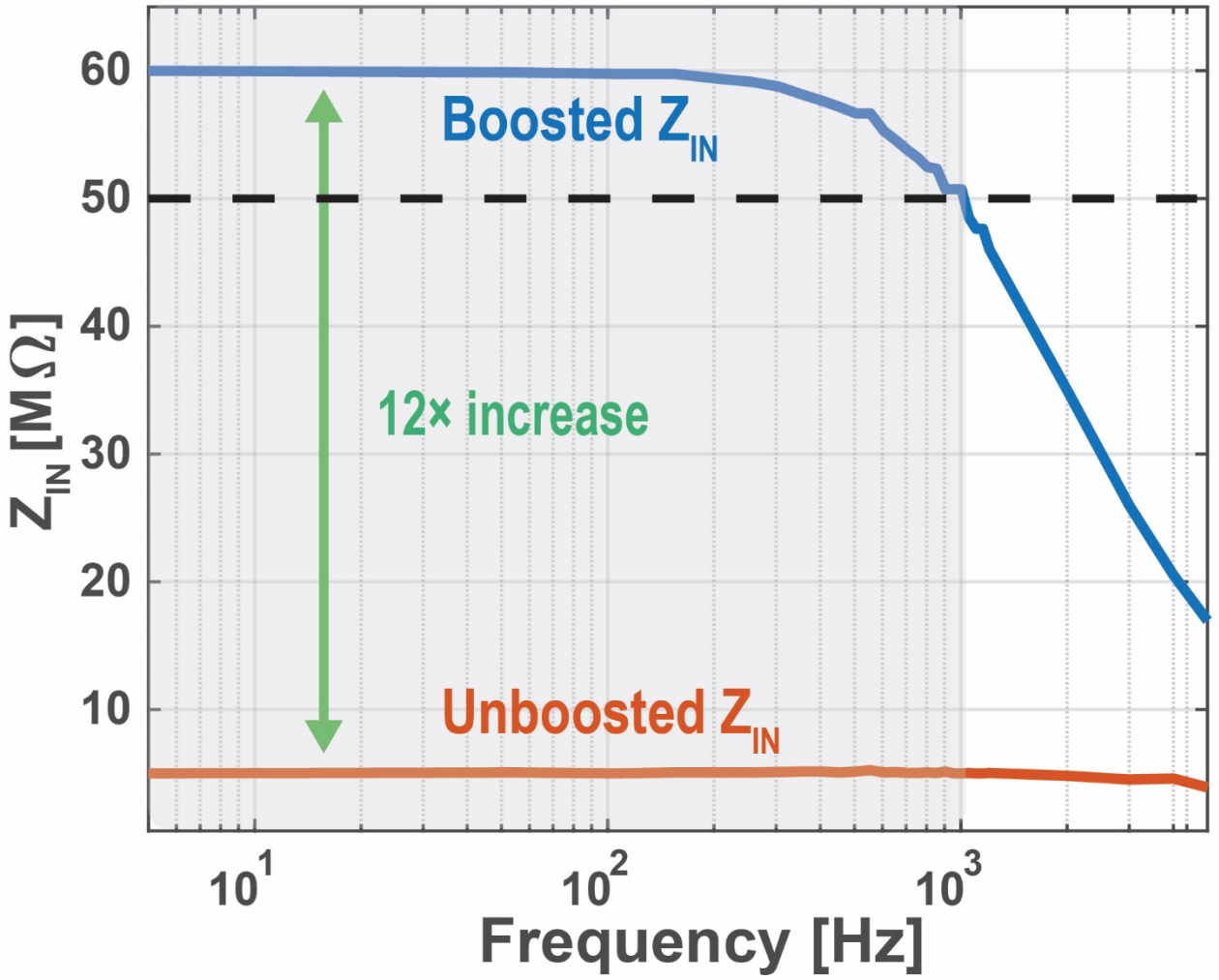
# Measured DR and Power Scaling



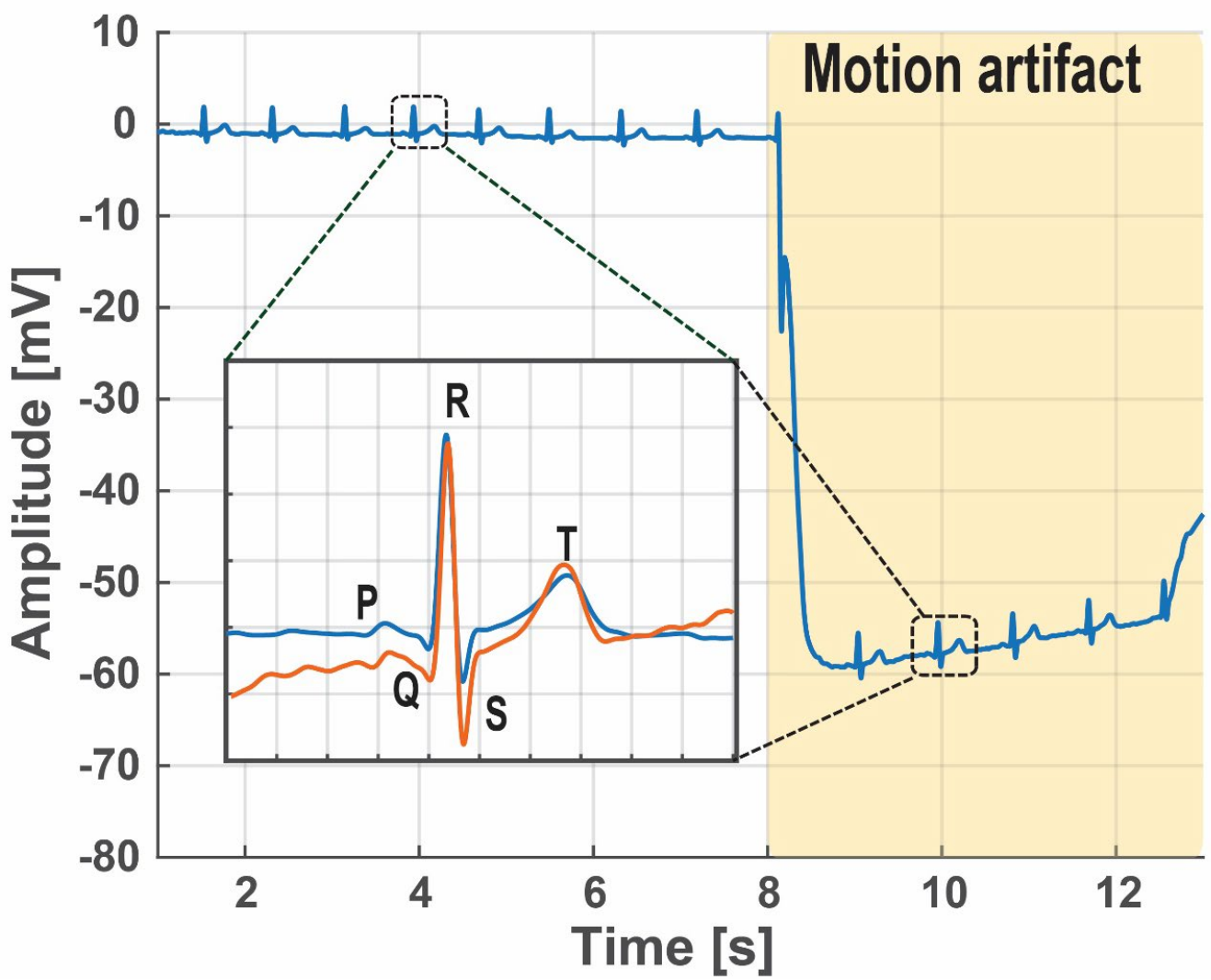
# Measured Two-tone Linearity



# Measured Input-Impedance

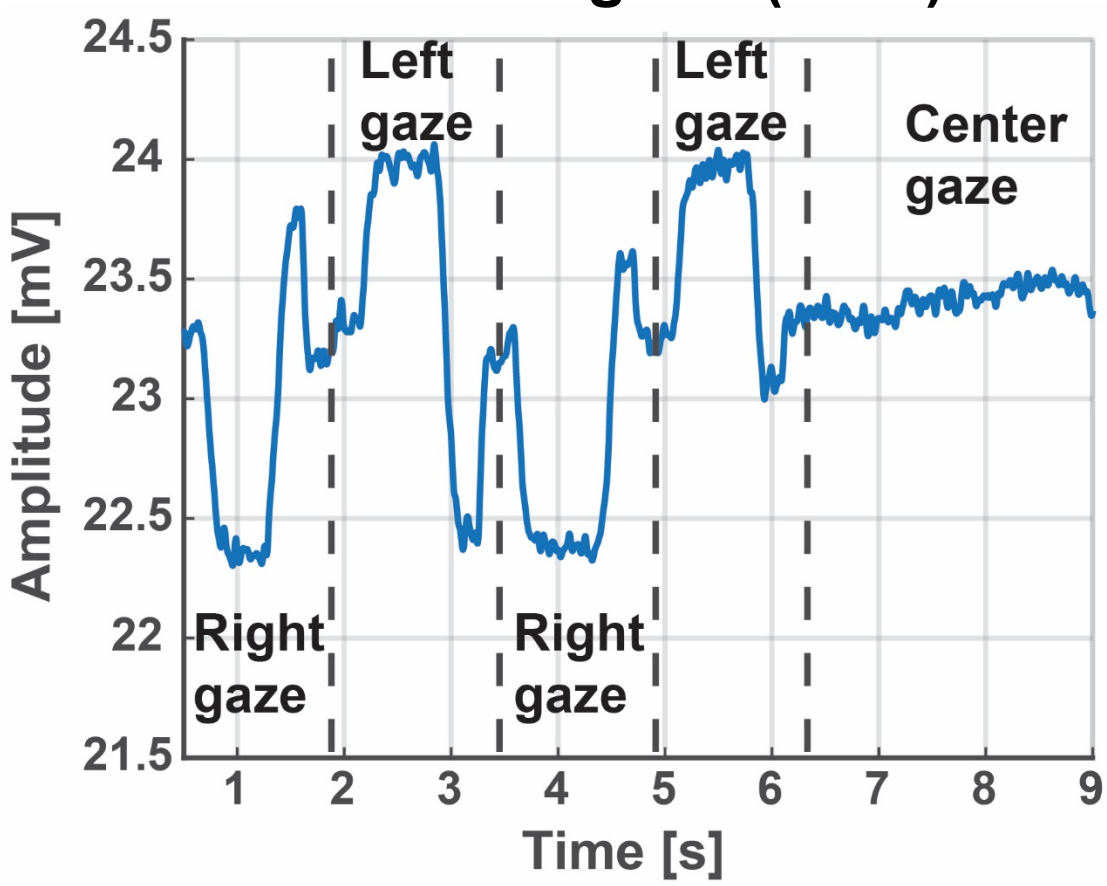


# Measured ECG with Motion Artifacts

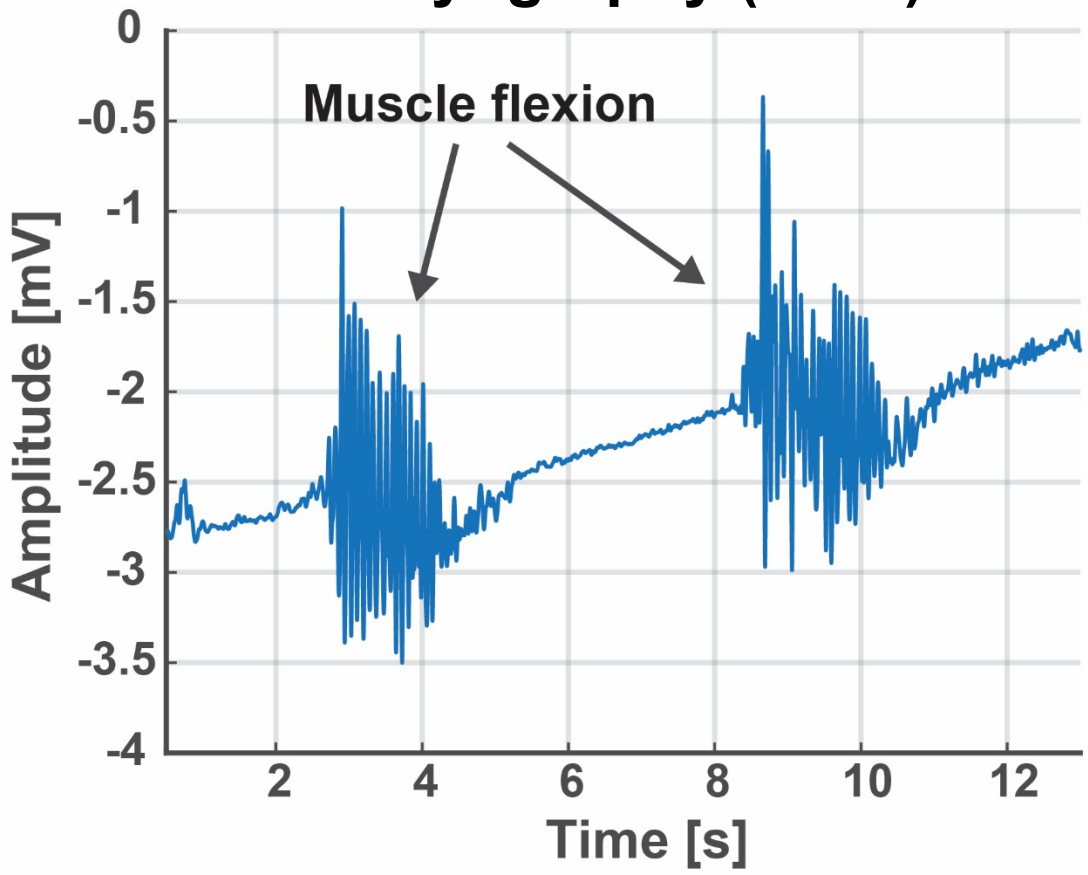


# Measured EOG and EMG

## Electro-oculogram (EOG)




## Electromyography (EMG)



# Performance Summary

| | J.Huang VLSI 2020 | S.Li CICC 2020 | W.Jiang JSSC 2017 | C.Lee ISSCC 2020 | J-S Bang VLSI 2018 | H.Chandrakumar JSSC 2019 | **This work** |
|---|---|---|---|---|---|---|---|
| Integration Domain | Time | Time | Time | Hybrid | Voltage | Voltage | **Time** |
| Topology | 1st -ord. VCO | 1st -ord. VCO | Open-loop VCO | 2nd -ord. Gm-C/VCO | 3rd -ord. CTΔΣ | CCIA + 3rd -ord. CTΔΣ | **2nd -ord. VCO** |
| Technology [nm] | 65 | 40 | 40 | 65 | 180 | 65 | **65** |
| Area [$mm^2$] | 0.08 | 0.025 | 0.135 | 0.078 | 0.5 | 0.113 | **0.075** |
| Supply (A/D) [V] | 1.2/0.7 | 0.8/0.6 | 1.2/0.45 | 1 | 1 | 1.2 | **1.2/0.8** |
| Power [µW] | 3.2 | 4.5 | 7 | 6.5 | 6.5 | 7.3 | **4.25/5.8** |
| Coupling | ac | ac | ac | dc | ac | ac | **ac** |
| Input-range [$mV_{pp}$] | 250 | 100 | 100 | 300 | 360 | 200 | **400** |
| Sampling frequency [kHz] | 32 | 2500 | 3 | 1280 | 12.8 | 400 | **200** |
| BW [kHz] | 0.5 | 10 | 0.2 | 10 | 0.3 | 5 | **1** |
| CMRR [dB] | 98 | 83 | 66 | 76 | 84 | 78 | **89** |
| Input-referred noise [nV/√Hz] | 53 | 36 | 367 | 95 | 265 | 90 | **110** |
| SNDR [dB] | 88.1 | 78.5 | 75.2 dB | 80.4 | 84.3 | 78 | **92.3** |
| DR [dB] | 94.2 | 79 | 77.4 dB | 80.4 | 84.3 | 81 | **92.3** |
| SFDR [dB] | 105.1 | 91 | 79 | 92.2 | 104.7 | 81 | **110.3** |
| $Z_{in}$ at DC [MΩ] | 4 | 0.22 | ∞ | ∞ | 39 | 1500 | **60** |
| $Z_{in}$ at BW [MΩ] | 4 | 0.22 | 8 | 13.3 | 39 | 19.6 | **50** |
| $FoM_{SNDR}$[dB] | 170 | 172 | 149.6 | 172.3 | 160.9 | 166.4 | **174.7** |

# Performance Summary

| | J.Huang VLSI 2020 | S.Li CICC 2020 | W.Jiang JSSC 2017 | C.Lee ISSCC 2020 | J-S Bang VLSI 2018 | H.Chandrakumar JSSC 2019 | **This work** |
|---|---|---|---|---|---|---|---|
| Integration Domain | Time | Time | Time | Hybrid | Voltage | Voltage | **Time** |
| Topology | 1st -ord. VCO | 1st -ord. VCO | Open-loop VCO | 2nd -ord. Gm-C/VCO | 3rd -ord. CTΔΣ | CCIA + 3rd -ord. CTΔΣ | **2nd -ord. VCO** |
| Technology [nm] | 65 | 40 | 40 | 65 | 180 | 65 | **65** |
| Area [$mm^2$] | 0.08 | 0.025 | 0.135 | 0.078 | 0.5 | 0.113 | **0.075** |
| Supply (A/D) [V] | 1.2/0.7 | 0.8/0.6 | 1.2/0.45 | 1 | 1 | 1.2 | **1.2/0.8** |
| Power [µW] | 3.2 | 4.5 | 7 | 6.5 | 6.5 | 7.3 | **4.25/5.8** |
| Coupling | ac | ac | ac | dc | ac | ac | **ac** |
| Input-range [$mV_{pp}$] | 250 | 100 | 100 | 300 | 360 | 200 | **400** |
| Sampling frequency [kHz] | 32 | 2500 | 3 | 1280 | 12.8 | 400 | **200** |
| BW [kHz] | 0.5 | 10 | 0.2 | 10 | 0.3 | 5 | **1** |
| CMRR [dB] | 98 | 83 | 66 | 76 | 84 | 78 | **89** |
| Input-referred noise [$nV/\sqrt{Hz}$] | 53 | 36 | 367 | 95 | 265 | 90 | **110** |
| SNDR [dB] | 88.1 | 78.5 | 75.2 dB | 80.4 | 84.3 | 78 | **92.3** |
| DR [dB] | 94.2 | 79 | 77.4 dB | 80.4 | 84.3 | 81 | **92.3** |
| SFDR [dB] | 105.1 | 91 | 79 | 92.2 | 104.7 | 81 | **110.3** |
| $Z_{in}$ at DC [MΩ] | 4 | 0.22 | ∞ | ∞ | 39 | 1500 | **60** |
| $Z_{in}$ at BW [MΩ] | 4 | 0.22 | 8 | 13.3 | 39 | 19.6 | **50** |
| $FoM_{SNDR}$[dB] | 170 | 172 | 149.6 | 172.3 | 160.9 | 166.4 | **174.7** |

# Performance Summary

| | J.Huang VLSI 2020 | S.Li CICC 2020 | W.Jiang JSSC 2017 | C.Lee ISSCC 2020 | J-S Bang VLSI 2018 | H.Chandrakumar JSSC 2019 | **This work** |
|---|---|---|---|---|---|---|---|
| Integration Domain | Time | Time | Time | Hybrid | Voltage | Voltage | **Time** |
| Topology | 1st -ord. VCO | 1st -ord. VCO | Open-loop VCO | 2nd -ord. Gm-C/VCO | 3rd -ord. CTΔΣ | CCIA + 3rd -ord. CTΔΣ | **2nd -ord. VCO** |
| Technology [nm] | 65 | 40 | 40 | 65 | 180 | 65 | **65** |
| Area [$mm^2$] | 0.08 | 0.025 | 0.135 | 0.078 | 0.5 | 0.113 | **0.075** |
| Supply (A/D) [V] | 1.2/0.7 | 0.8/0.6 | 1.2/0.45 | 1 | 1 | 1.2 | **1.2/0.8** |
| Power [µW] | 3.2 | 4.5 | 7 | 6.5 | 6.5 | 7.3 | **4.25/5.8** |
| Coupling | ac | ac | ac | dc | ac | ac | **ac** |
| Input-range [$mV_{pp}$] | 250 | 100 | 100 | 300 | 360 | 200 | **400** |
| Sampling frequency [kHz] | 32 | 2500 | 3 | 1280 | 12.8 | 400 | **200** |
| BW [kHz] | 0.5 | 10 | 0.2 | 10 | 0.3 | 5 | **1** |
| CMRR [dB] | 98 | 83 | 66 | 76 | 84 | 78 | **89** |
| Input-referred noise [nV/√Hz] | 53 | 36 | 367 | 95 | 265 | 90 | **110** |
| SNDR [dB] | 88.1 | 78.5 | 75.2 dB | 80.4 | 84.3 | 78 | **92.3** |
| DR [dB] | 94.2 | 79 | 77.4 dB | 80.4 | 84.3 | 81 | **92.3** |
| SFDR [dB] | 105.1 | 91 | 79 | 92.2 | 104.7 | 81 | **110.3** |
| $Z_{in}$ at DC [MΩ] | 4 | 0.22 | ∞ | ∞ | 39 | 1500 | **60** |
| $Z_{in}$ at BW [MΩ] | 4 | 0.22 | 8 | 13.3 | 39 | 19.6 | **50** |
| $FoM_{SNDR}$[dB] | 170 | 172 | 149.6 | 172.3 | 160.9 | 166.4 | **174.7** |

# Conclusion

**We reported a 2nd-order VCO-based ExG front-end with high dynamic range and low power for motion artifact tolerance using a new GIRO quantizer with sign feedforward.**

**Key achievements:**

- 2nd-order VCO-only ADC
- Wide input-range (**400 $mV_{pp}$**) and dynamic range (**92.3 dB**)
- Dynamic power consumption w/ input amplitude
- High input-impedance across the bandwidth of interest (>**50 MΩ**)
- State-of-the-art linearity (**110.3 dB**) by using a GIRO-based quantizer
- State-of-the-art FoM (**174.7 dB**) using a power-efficient multiphase quantizer