A 400 MHz 4.5 nW –63.8 dBm Sensitivity Wake-up Receiver Employing an Active Pseudo-Balun Envelope Detector

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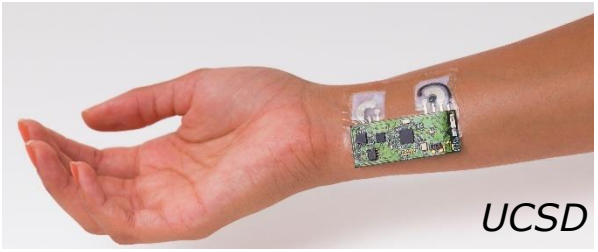
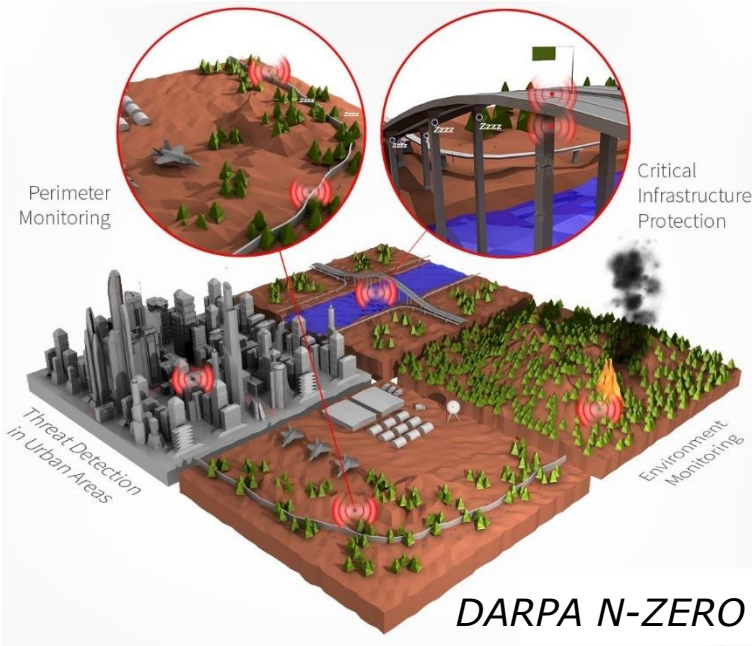
UCSD

Motivation

Wearables/Medical

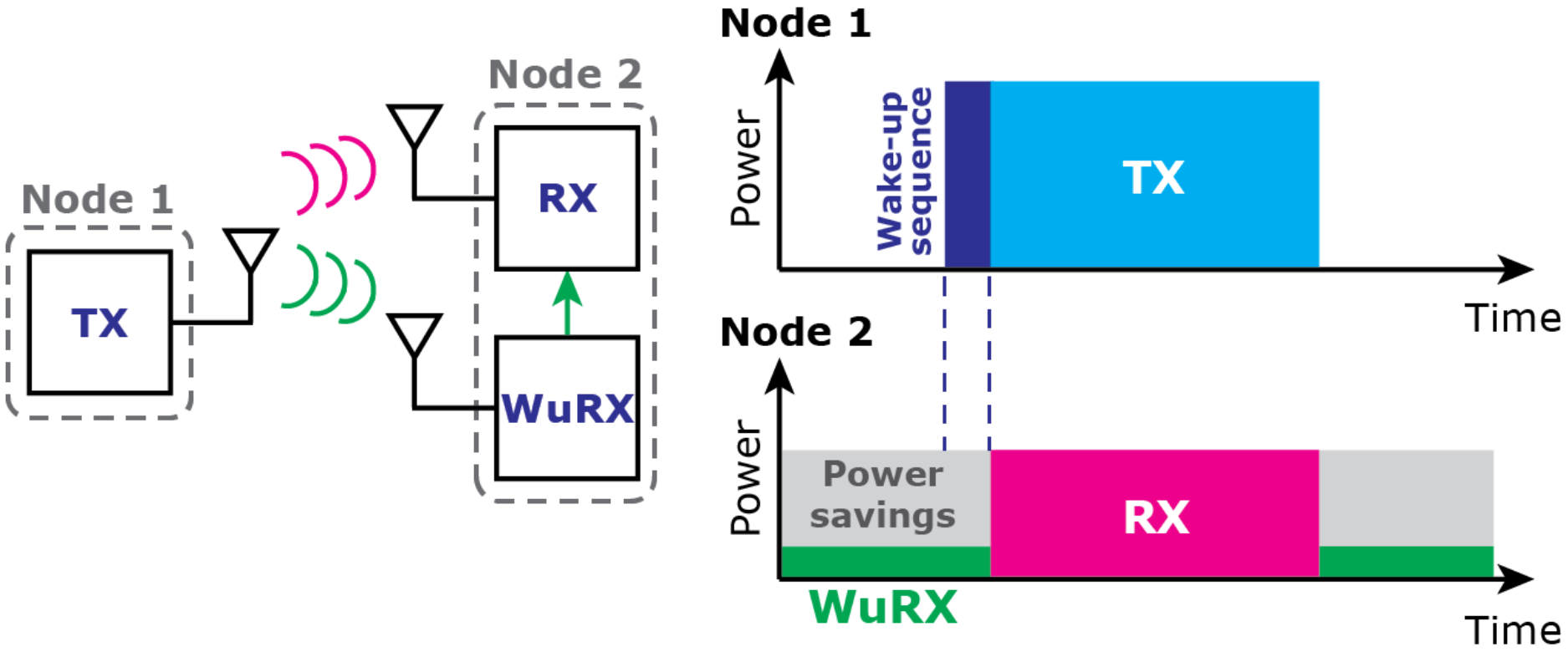


Unattended ground sensors



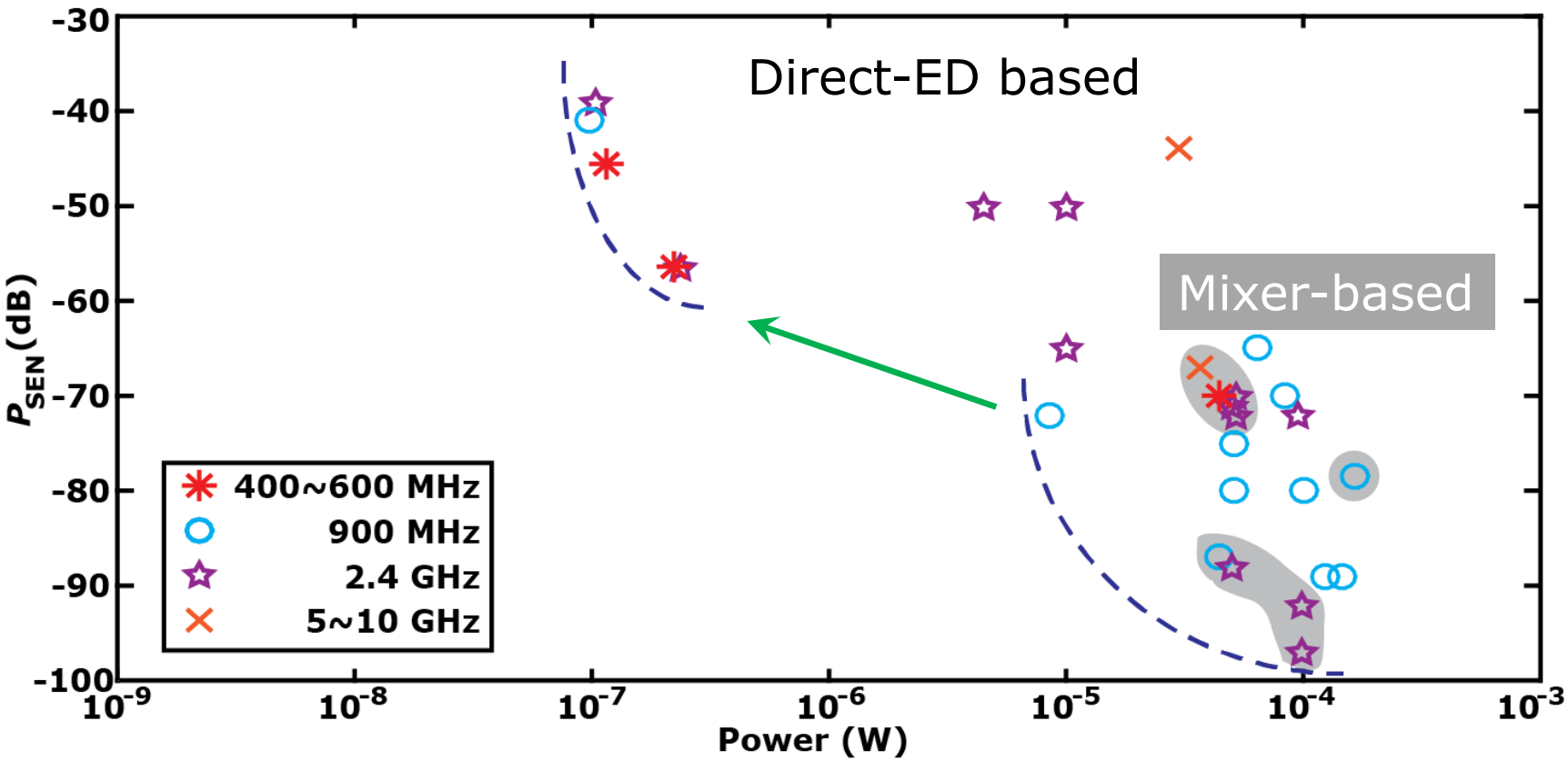
- The age of Internet of Everything (IoE)
  - 500 billion connected devices before 2030 [*Cisco, 2014*]
- Event-driven applications focuses on lifetime and range
  - Low power and high sensitivity are the main targets

Wake-up receiver (WuRX)



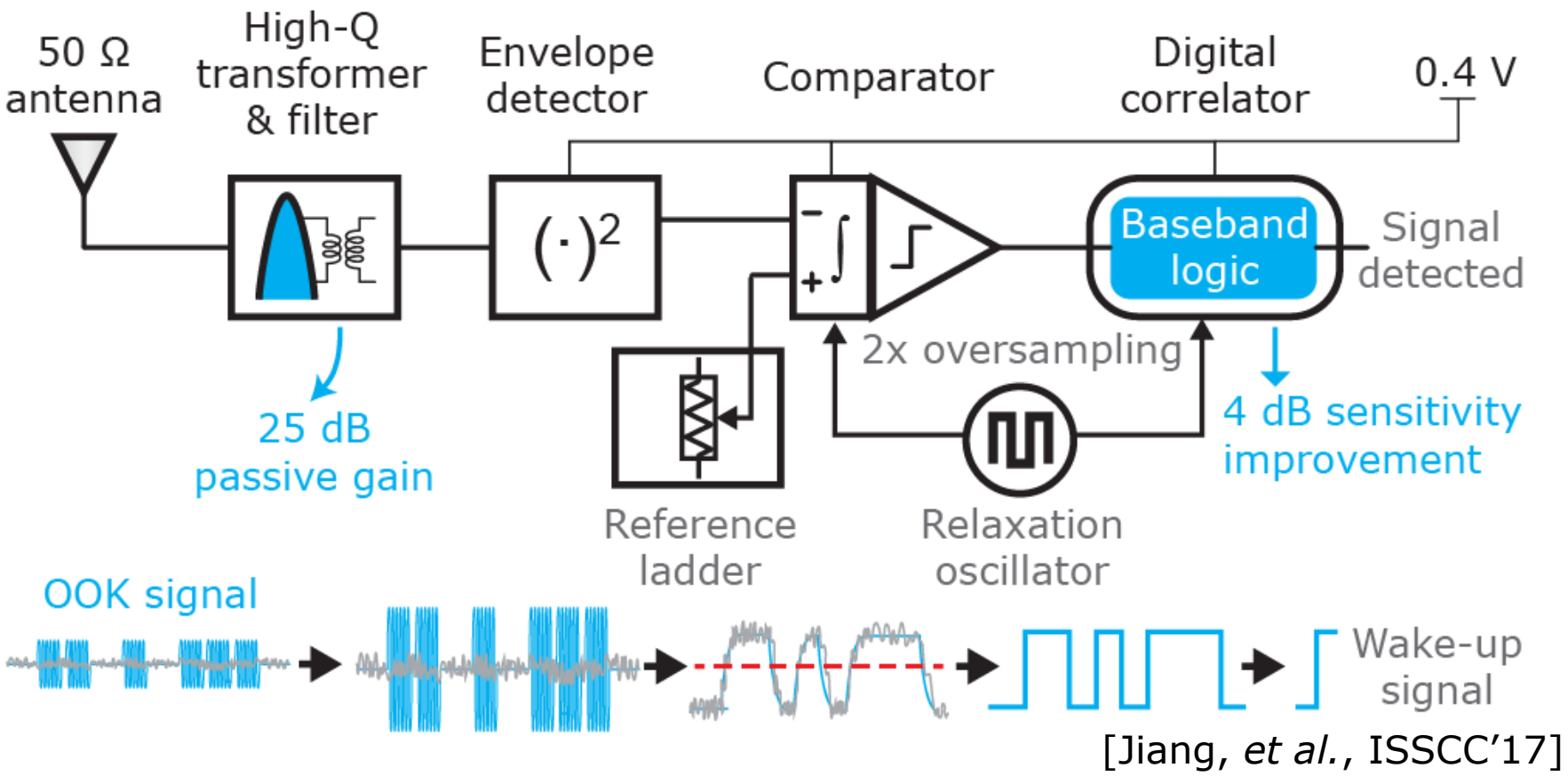
- For infrequent event-driven networks:
  - Always-ON WuRX extends system lifetime
  - WuRX sensitivity should be comparable with main RX

State-of-the-art WuRX comparison



Prior-art sub-μW WuRX compromises sensitivity for low power consumption

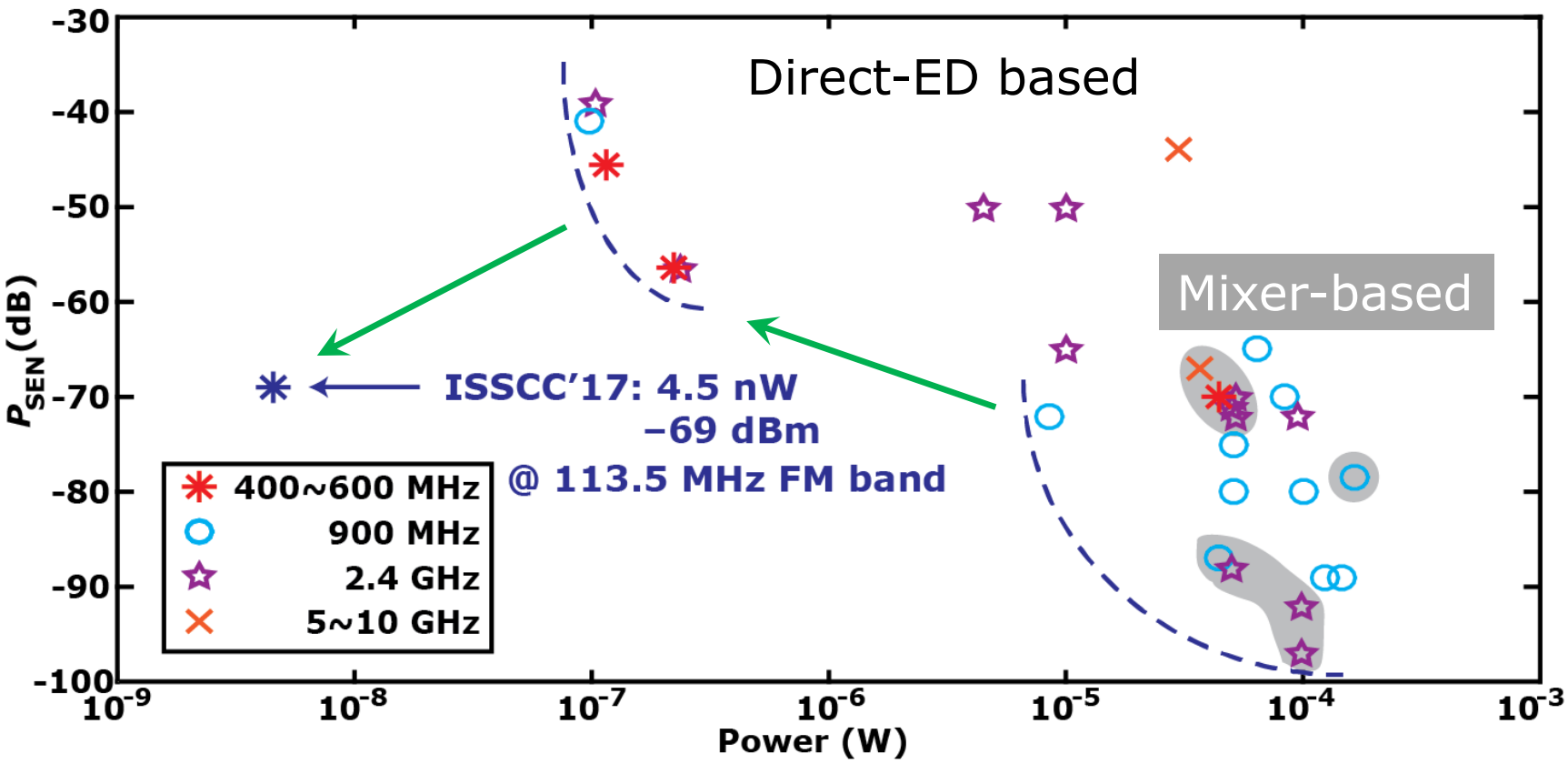
State-of-the-art nW WuRX



[Jiang, *et al.*, ISSCC'17]

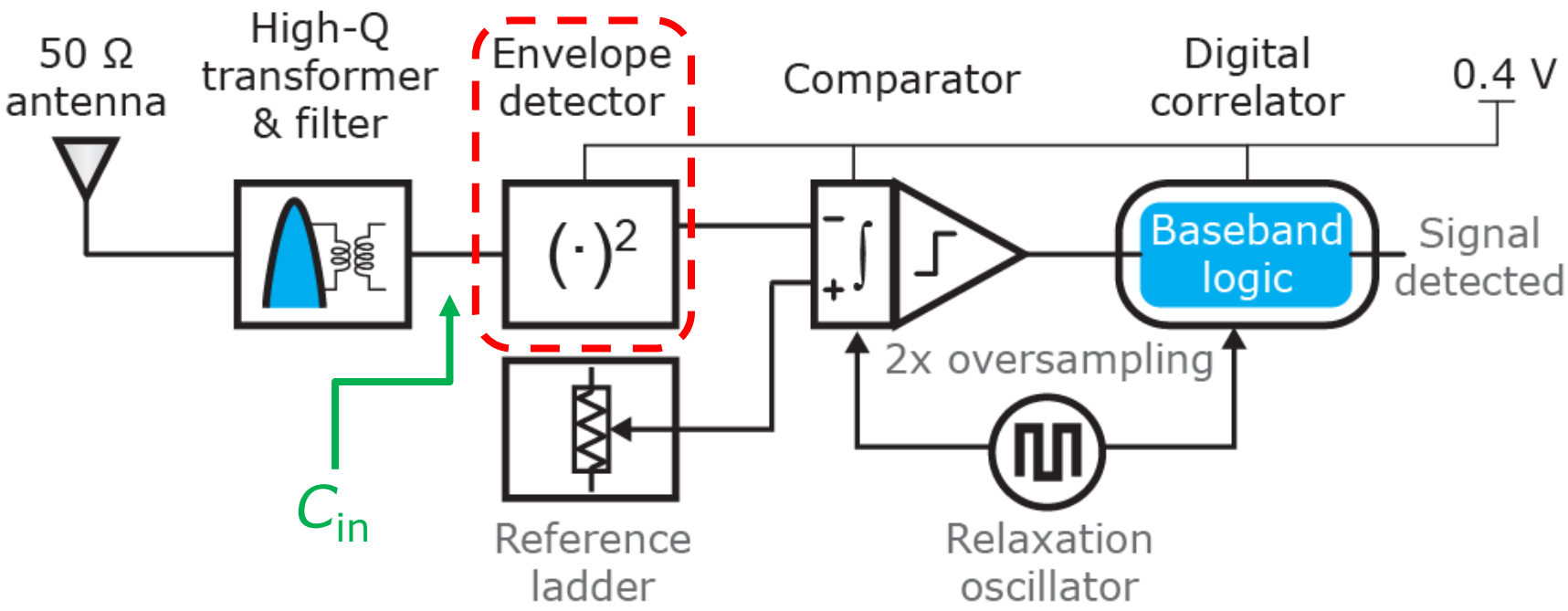
- Direct envelope detection architecture
- 25 dB passive gain enabled by high R_{in} ED

State-of-the-art WuRX comparison



Q1: Could we use the same approach at a higher frequency?

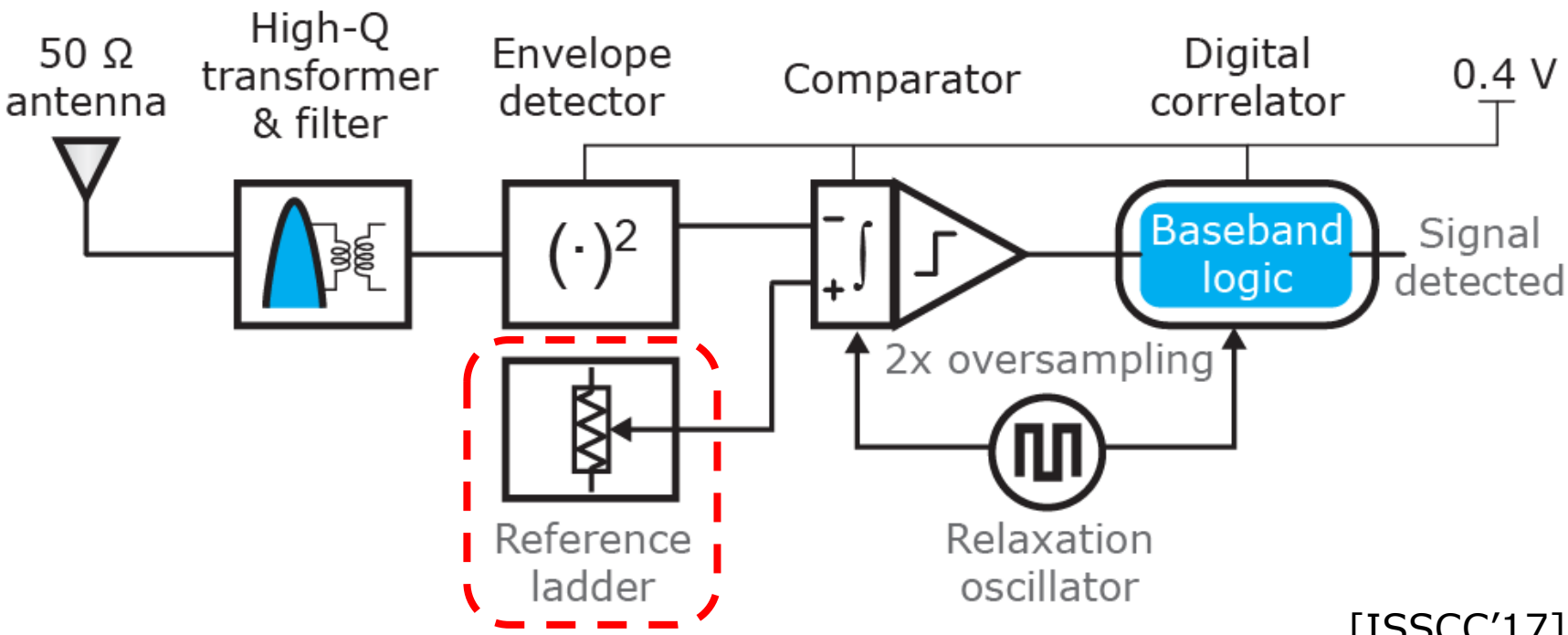
Problem 1: high input capacitance ED



[ISSCC'17]

High C_{in} ED limits carrier frequency and passive gain

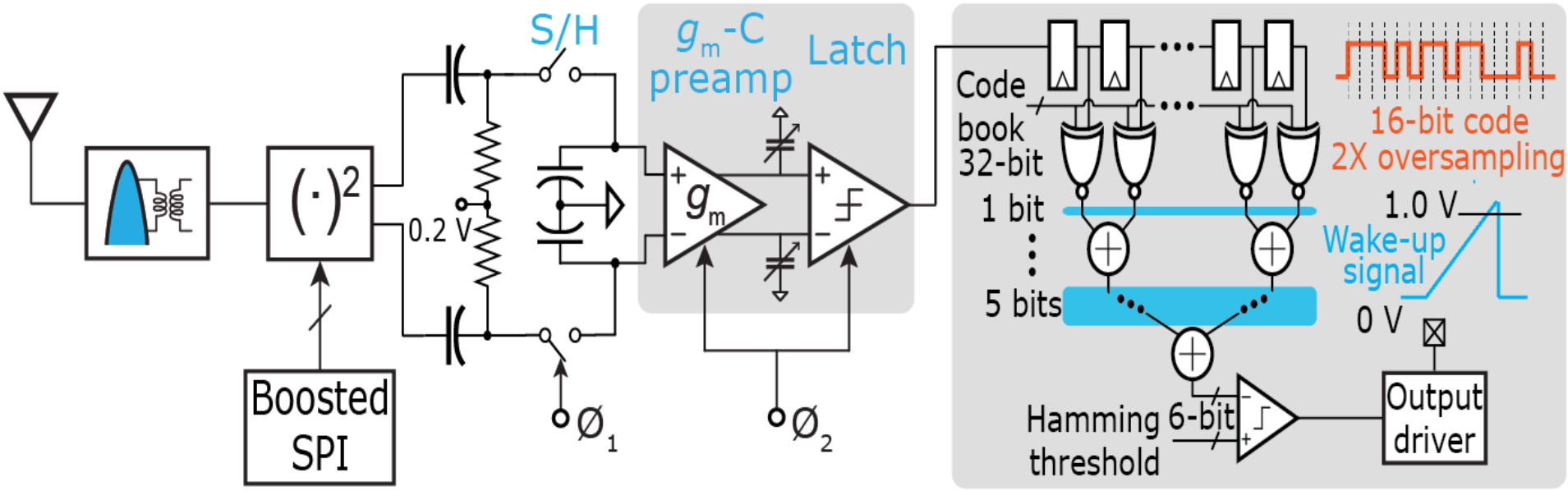
Problem 2: single-ended output ED



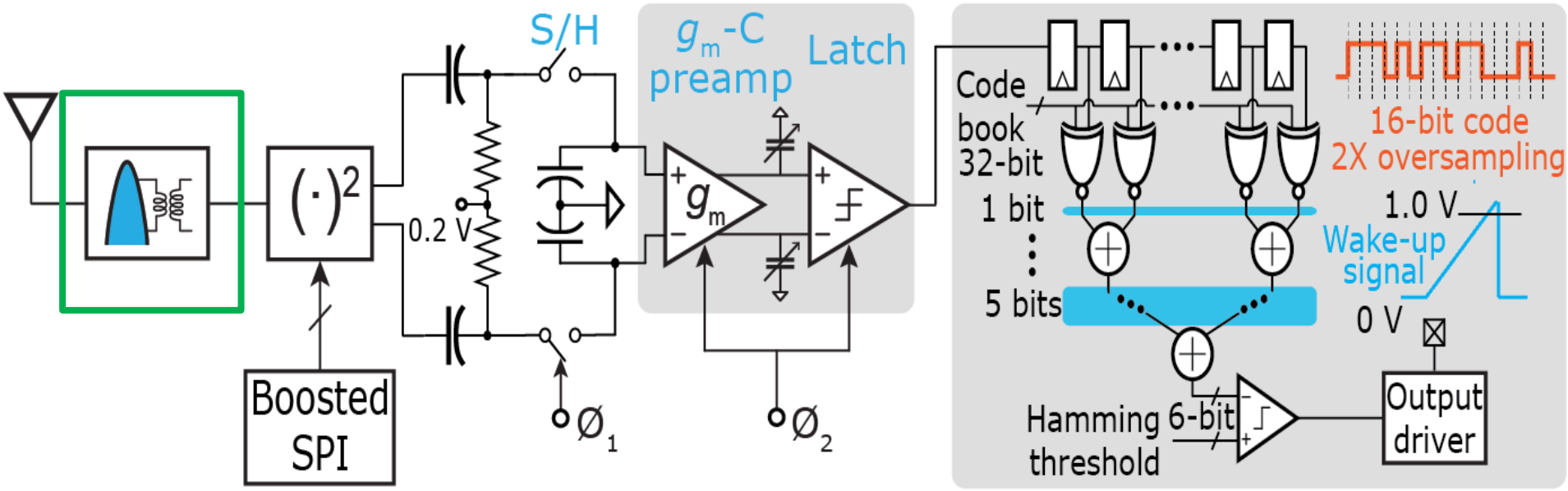
[ISSCC'17]

- Needs extra reference circuit for comparator
  - Extra tuning required for DC variation from PVT
  - Reference circuit is an additional noise source
- Q2: Could we eliminate the reference circuit?

Proposed WuRX architecture

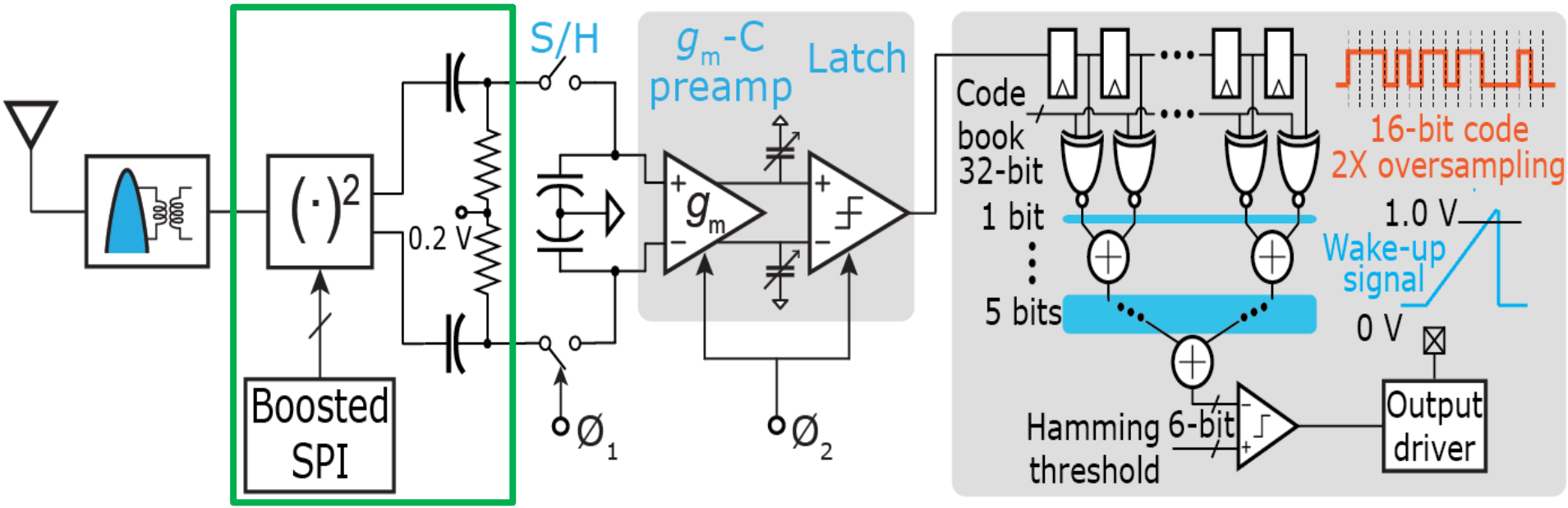


Proposed WuRX architecture



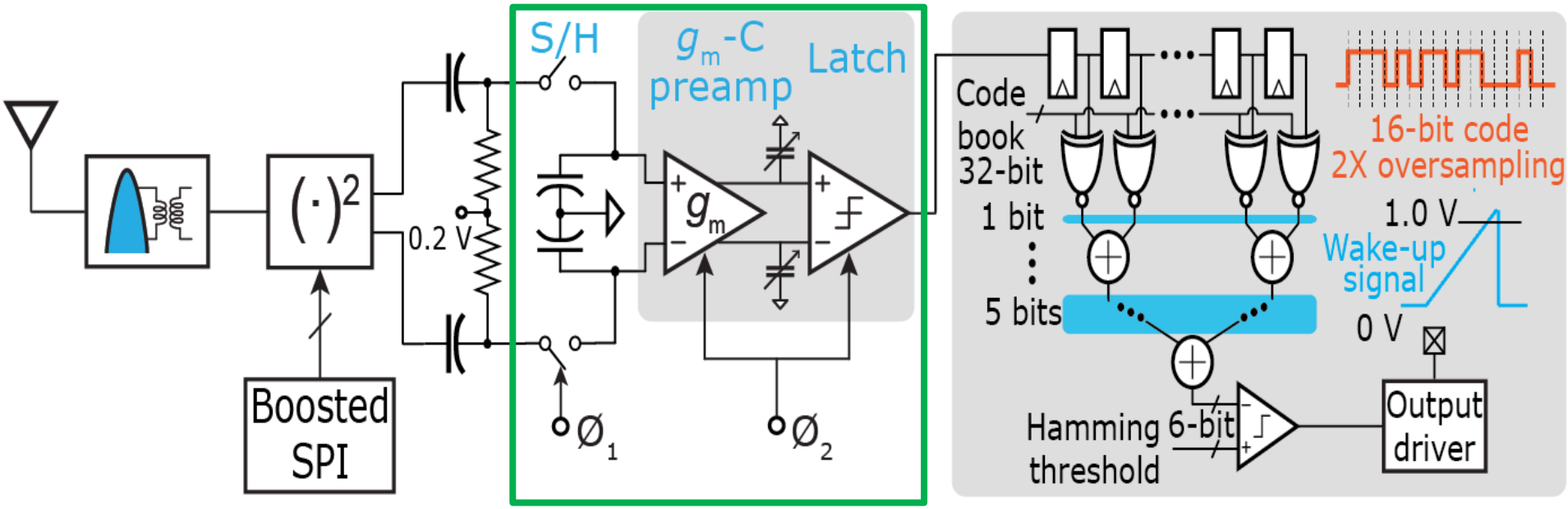
- Transformer filter
  - 18.5 dB passive gain @ 402~405 MHz MICS band

Proposed WuRX architecture



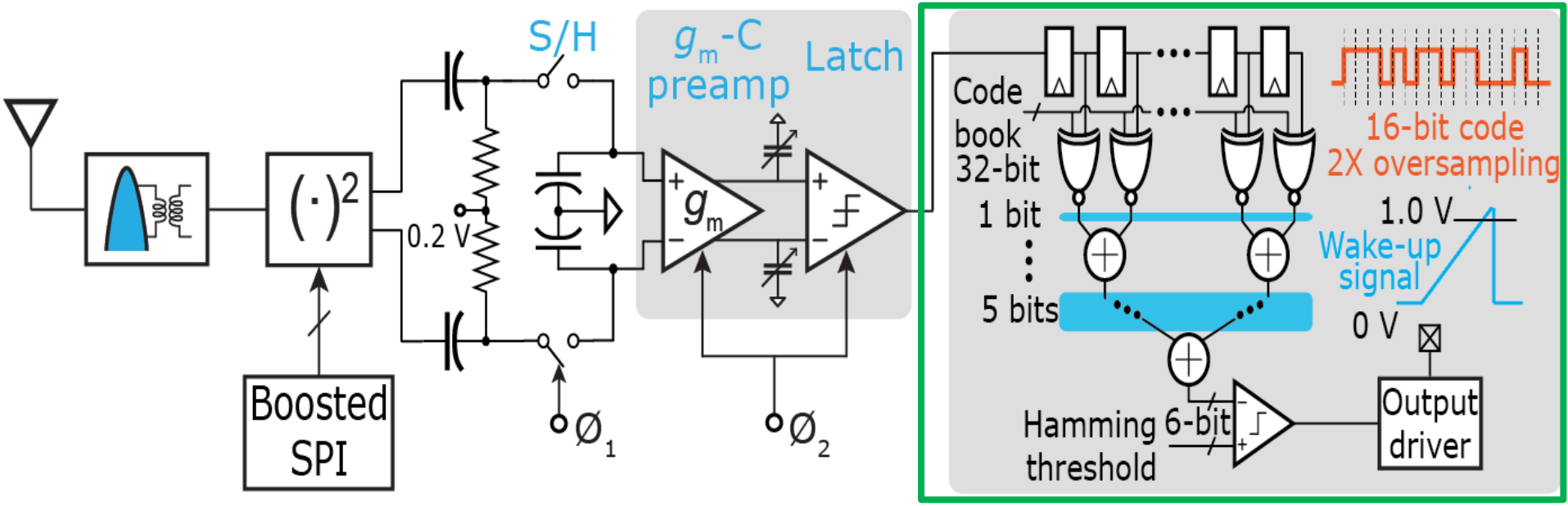
- Active pseudo-balun CG DTMOS envelope detector
  - Single-ended input to pseudo-differential output
  - Boosted SPI for super cut-off switches

Proposed WuRX architecture



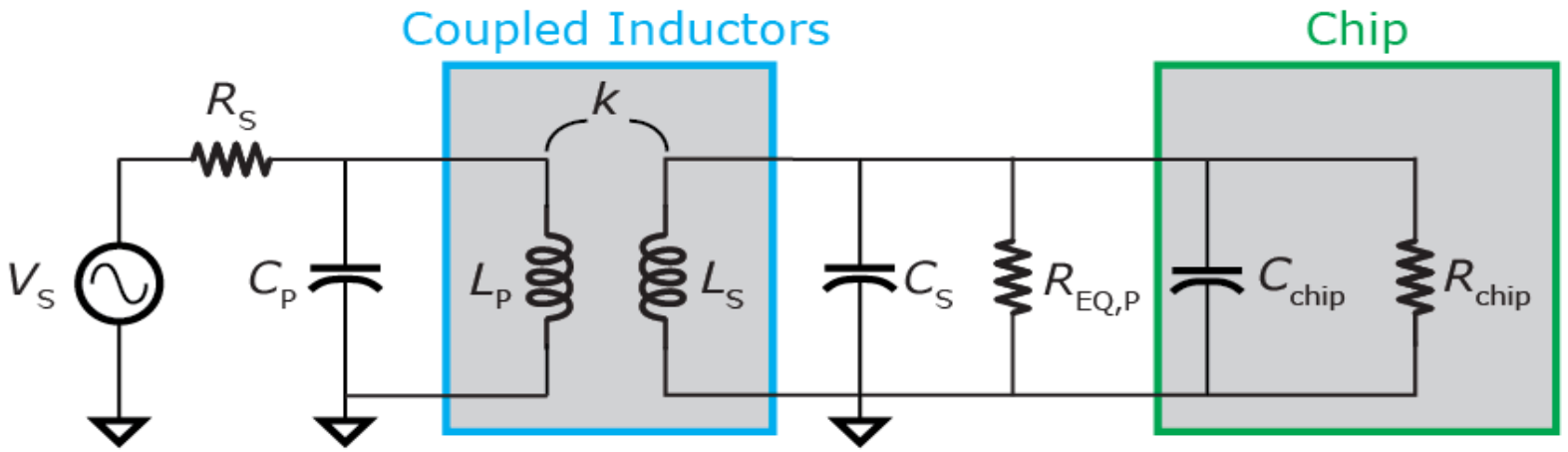
- S/H stage and 2-stage comparator
  - S/H stage solves asymmetric comparator kickback at $\emptyset_2$

Proposed WuRX architecture

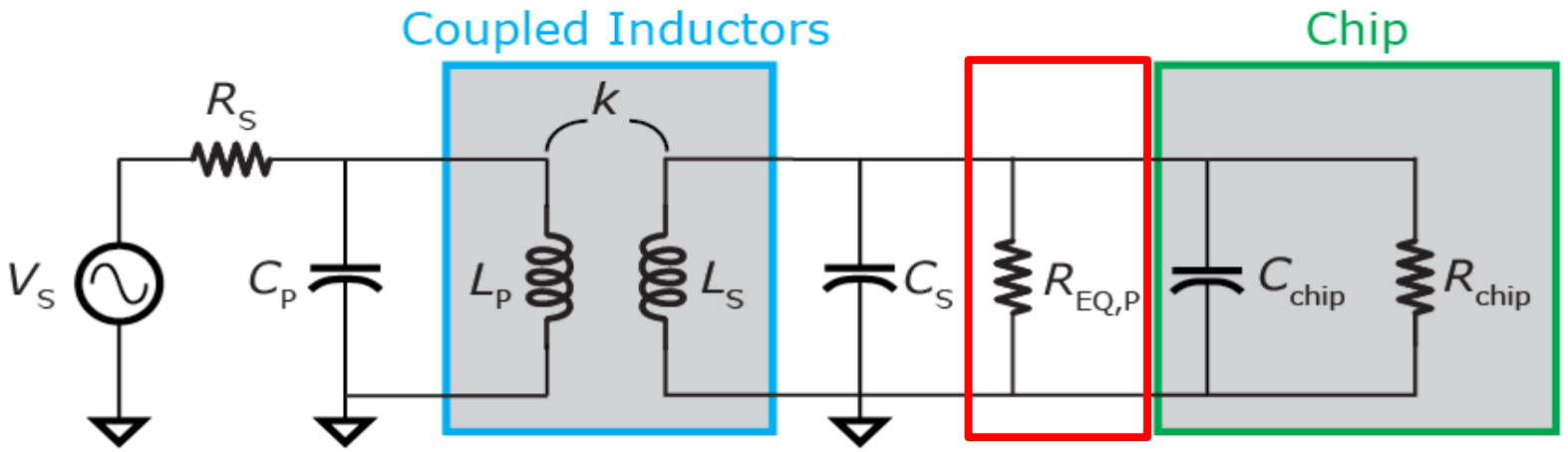


- Digital correlator
  - 2× oversampling overcomes clock asynchronization
  - 4 dB coding gain

Maximizing passive voltage gain



Maximizing passive voltage gain

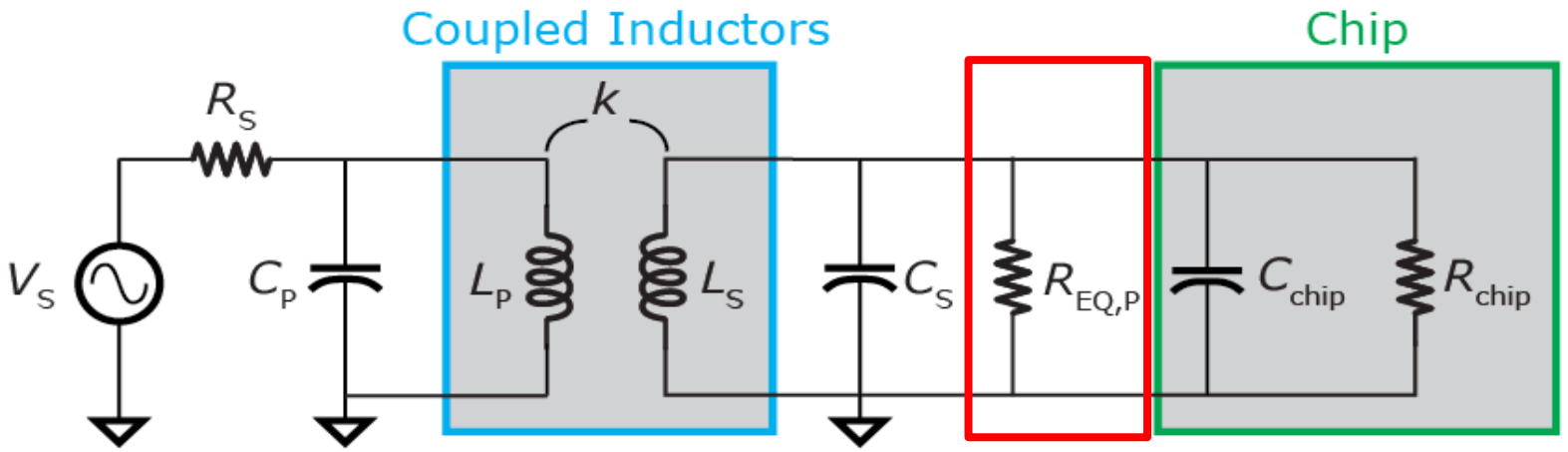


Equivalent parallel resistance of L_S

- $A_V \approx \sqrt{R_{EQ,P} || R_{chip} / R_S}$ → Requires high-Q passives and a large chip input impedance

E.g.: Assuming $R_{chip} \to \infty$, 25 dB gain from 50 Ω requires $R_{EQ,P}$=16 kΩ

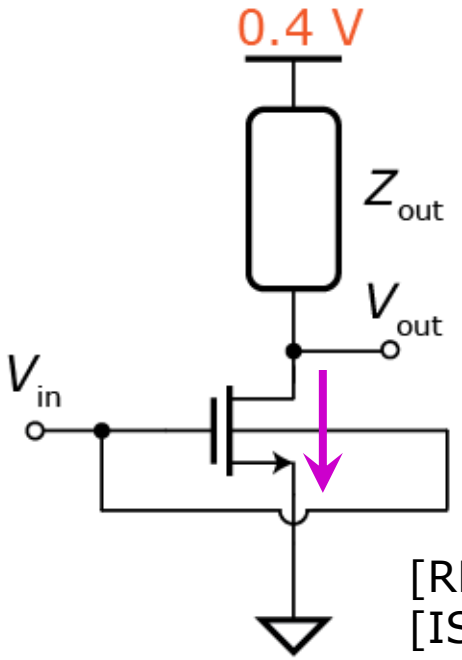
Maximizing passive voltage gain



Equivalent parallel resistance of L_S

- $R_{EQ,P} = {}^{Q}/_{\omega_{RF}(C_S+C_{chip})}$ ➡ $A_V \propto \sqrt{\frac{1}{f_{RF}(C_S+C_{chip})}}$
  - **Objective:** under given f_{RF}, minimize $(C_S + C_{chip})$ to maximize L_S and therefore passive voltage gain

Active envelope detector: prior-art



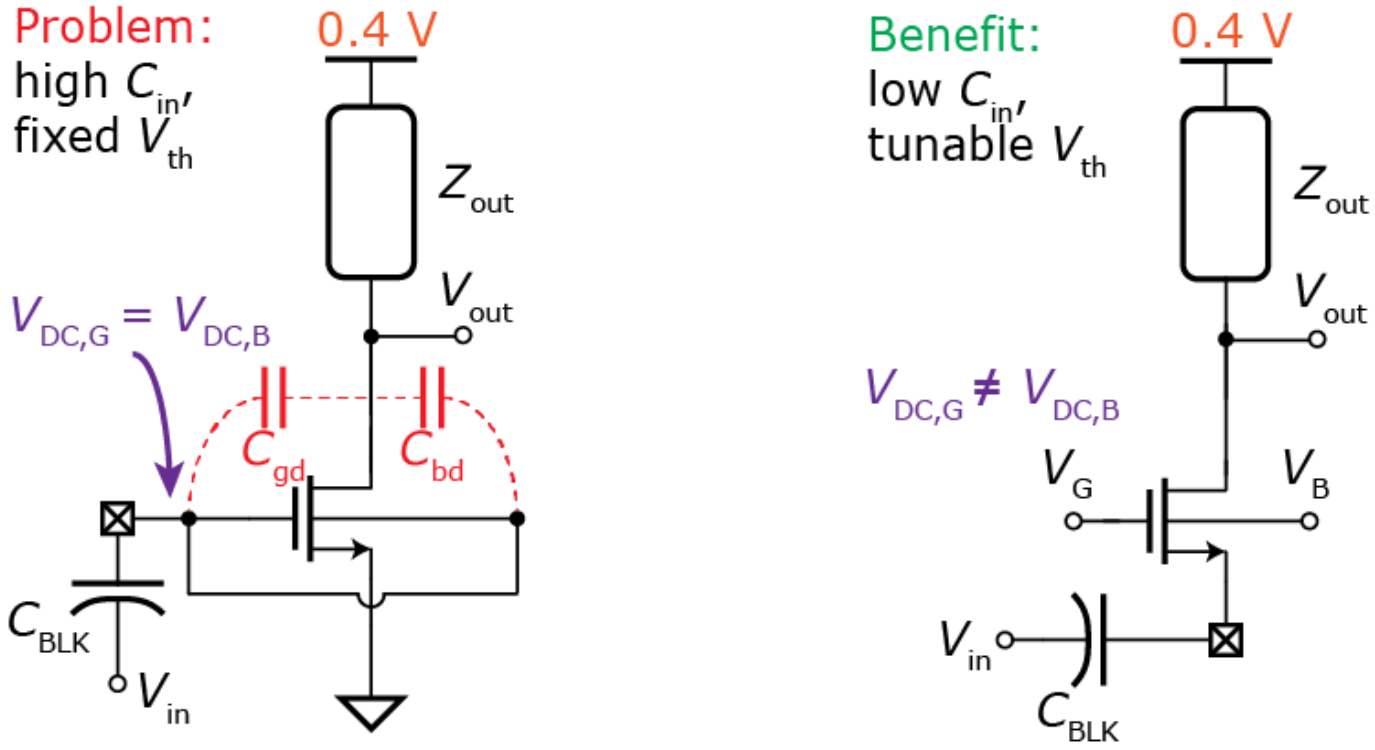
[RFIC'12]
[ISSCC'17]

$$i_{DS} = \mu C_{ox} \frac{W}{L} (n-1) \emptyset_t^2 e^{\frac{v_{GS}-V_{th}}{n\emptyset_t}}$$

$$g_{m2} = \frac{1}{2} \cdot \frac{\partial^2 i_{DS}}{\partial v_{GS}^2} = \frac{I_{DS}}{2(n\emptyset_t)^2}$$

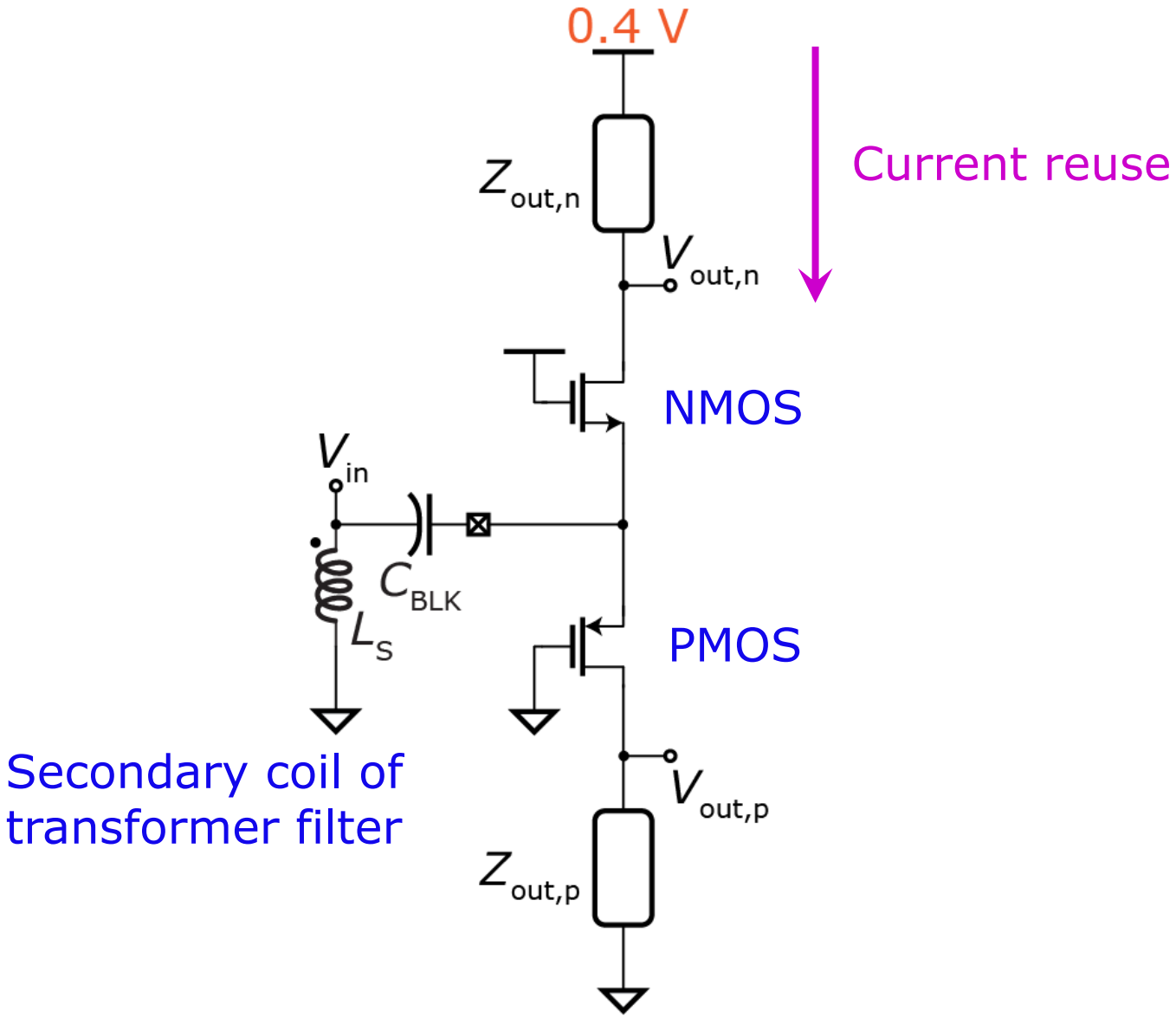
- ☑ High R_{in} supports high transformer passive gain
- ☑ Subthreshold biasing for large 2nd order non-linearity
- ☑ DTMOS configuration provides 16% more g_{m2}
- ☒ High C_{in} limits frequency and achievable passive gain

Common Source vs. Common Gate ED

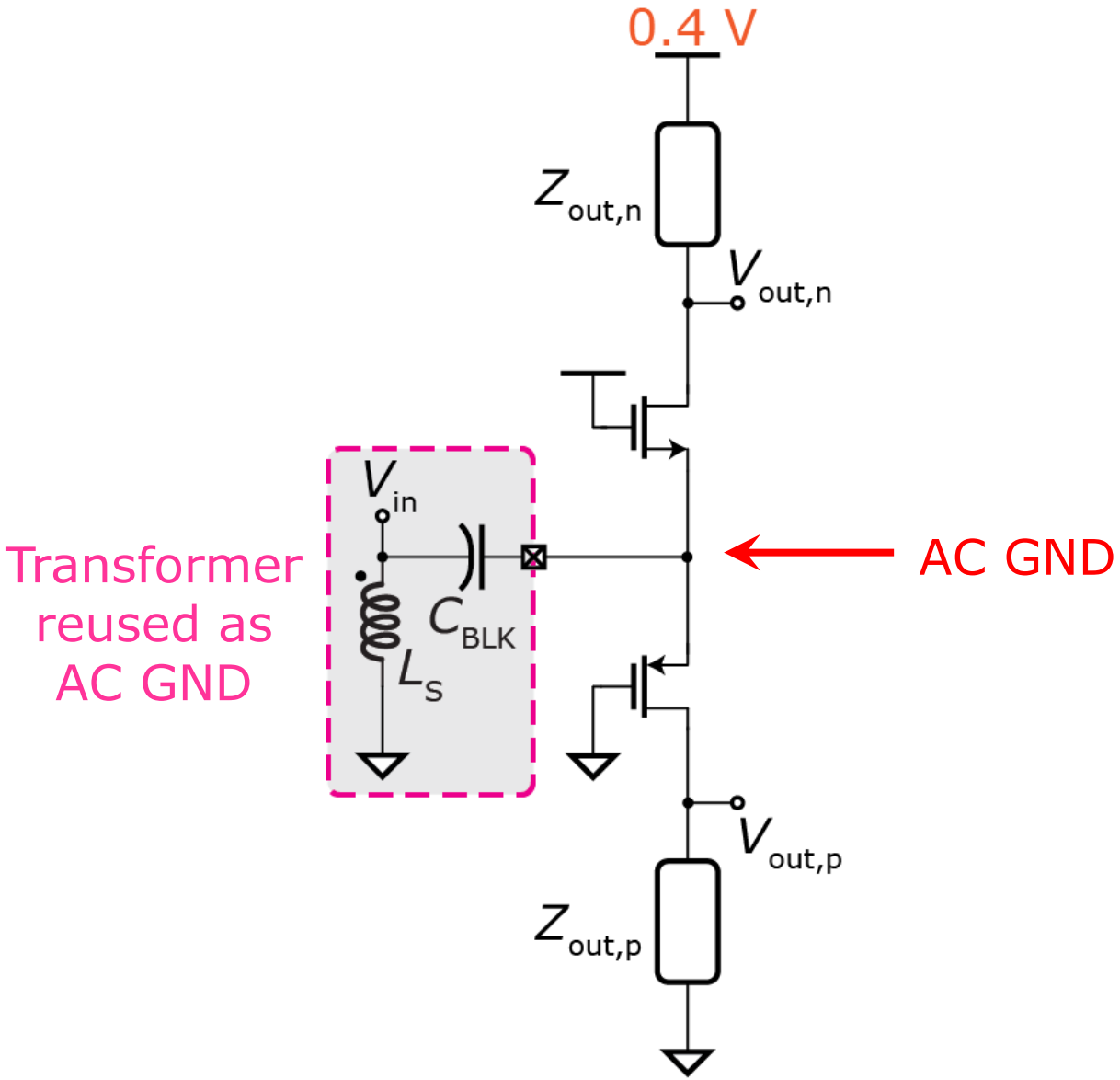


- Common gate input eliminates C_{gd} and C_{bd}
  - Saves 47.5% C_{in} based on simulation
- Extra freedom on bulk bias voltage and V_{th} is tunable
  - DTMOS advantage retained (16% extra g_{m2})

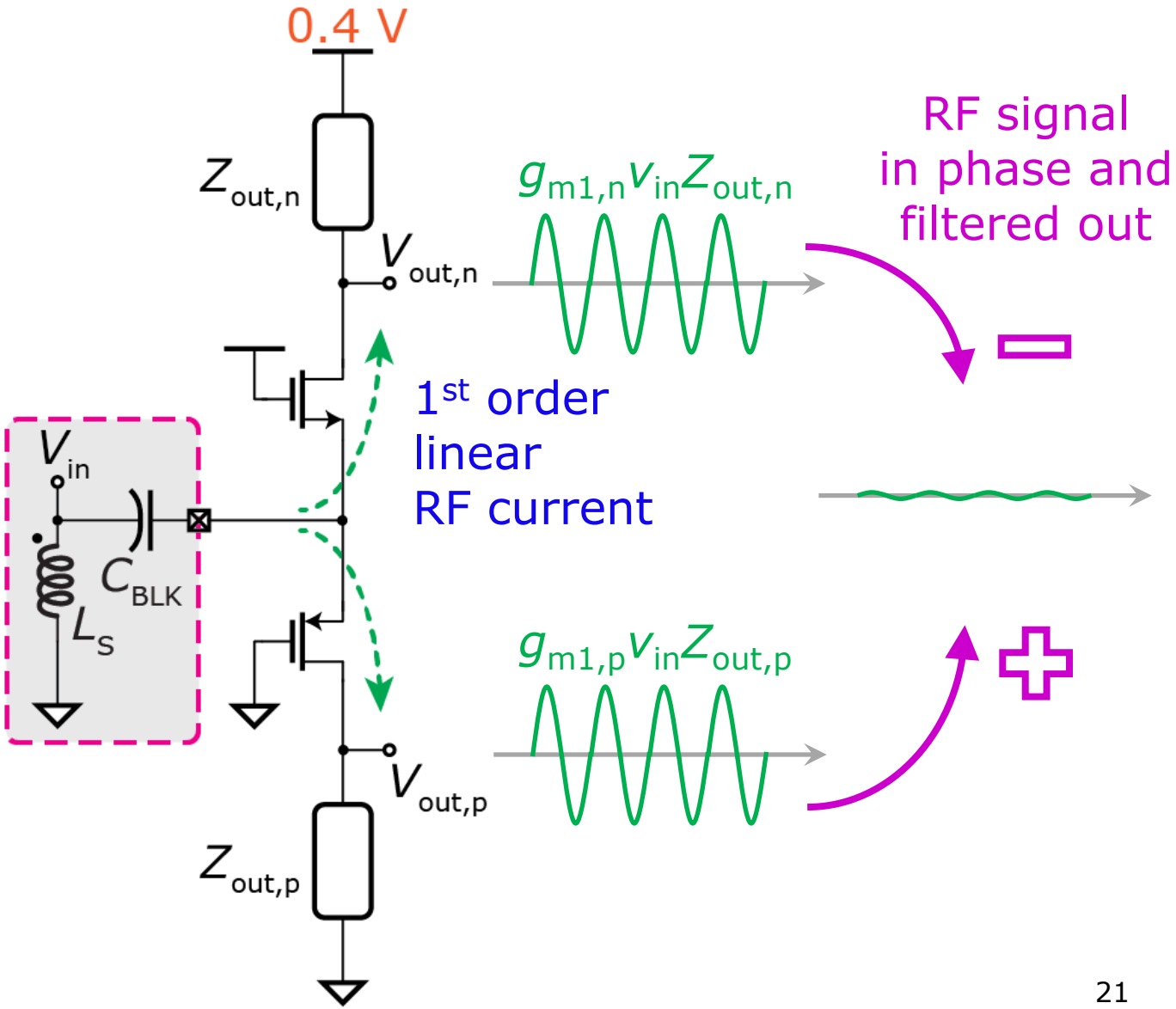
Active pseudo-balun CG ED



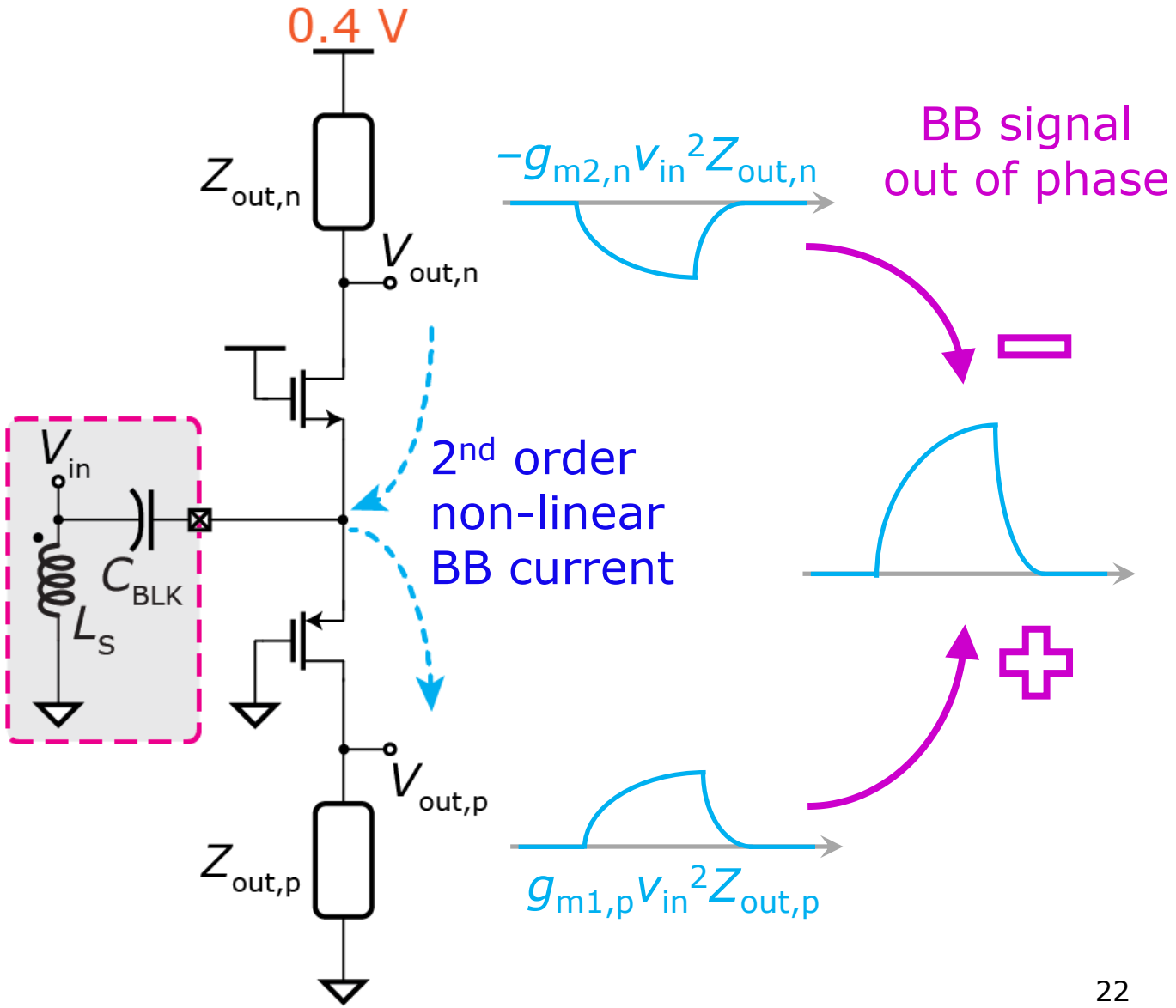
Active pseudo-balun CG ED



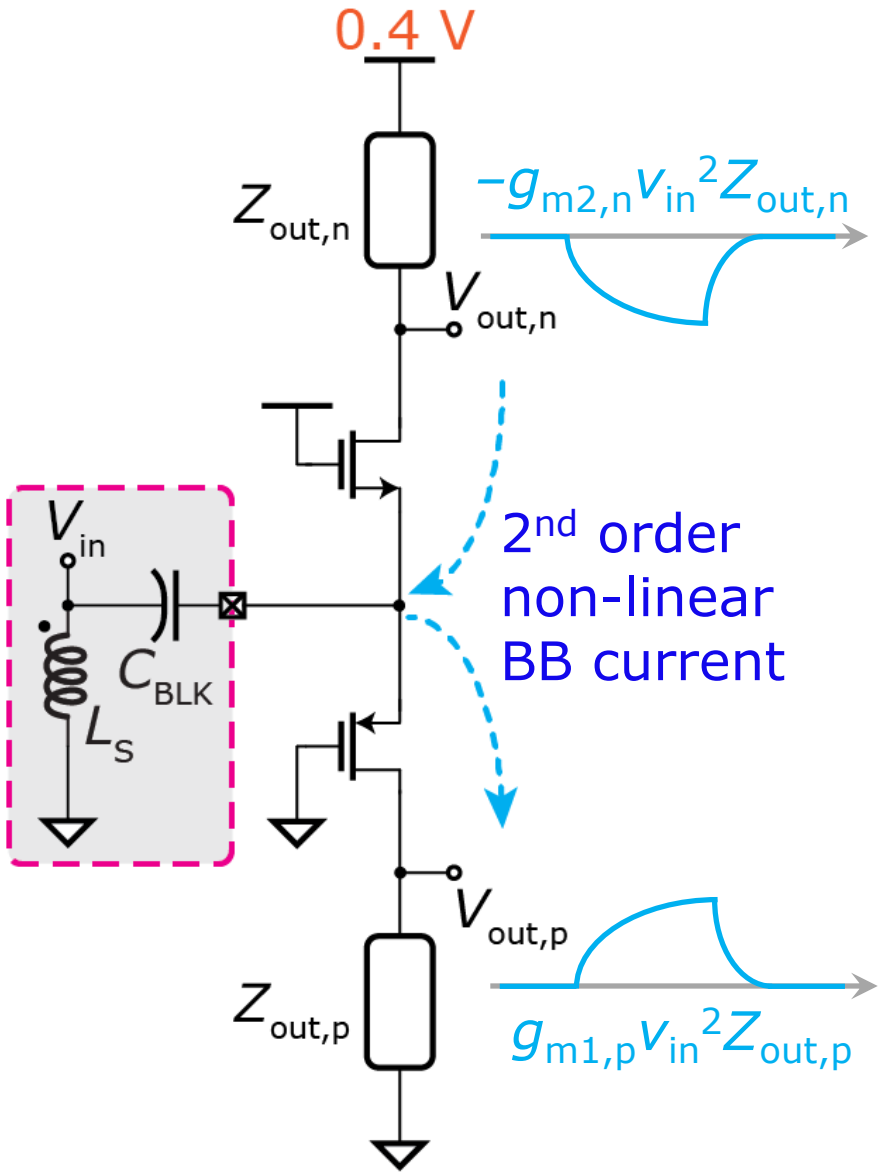
Active pseudo-balun CG ED



Active pseudo-balun CG ED



Active pseudo-balun CG ED



2× signal voltage
2× noise power

⬇

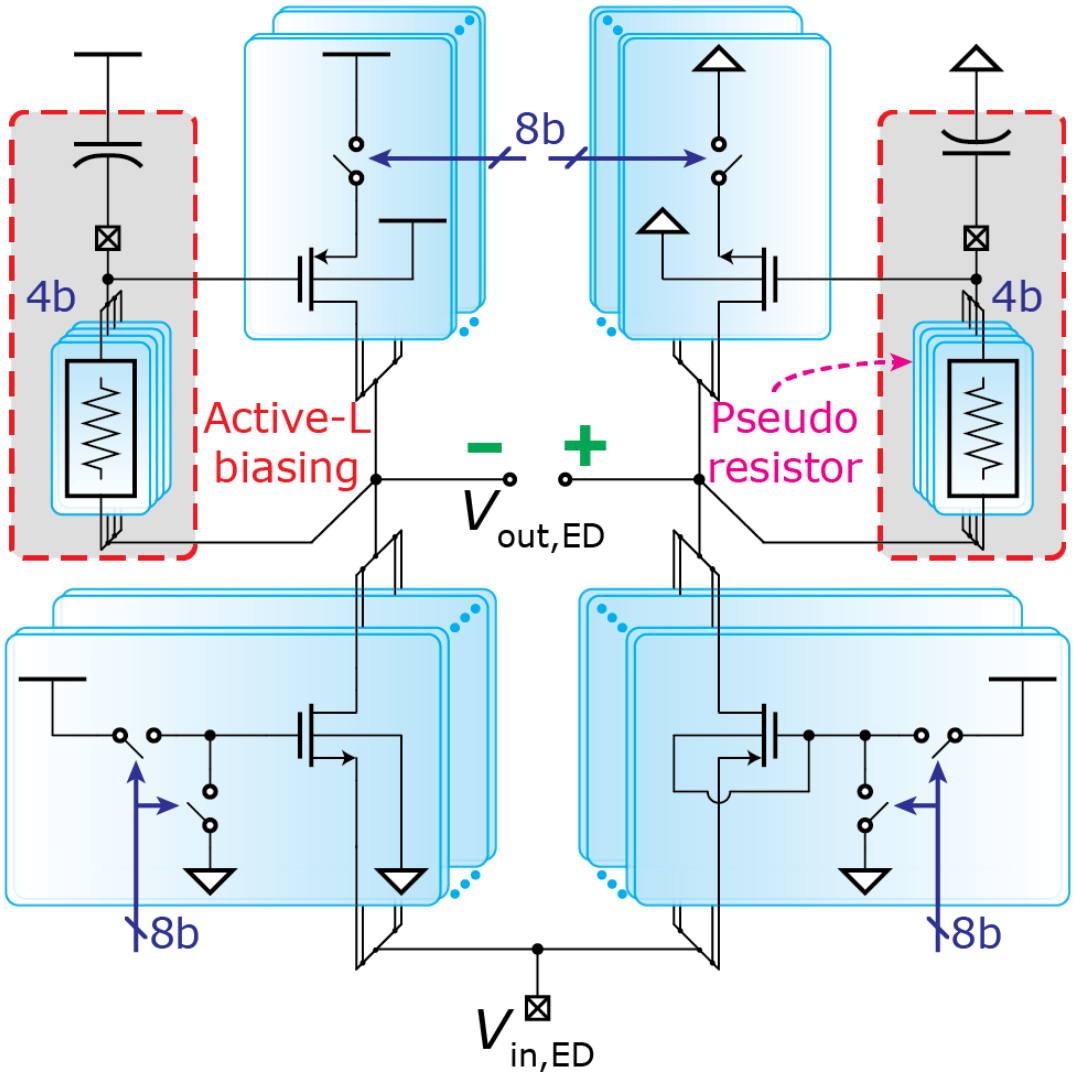
1.5 dB sensitivity improvement

Pseudo-differential output

⬇

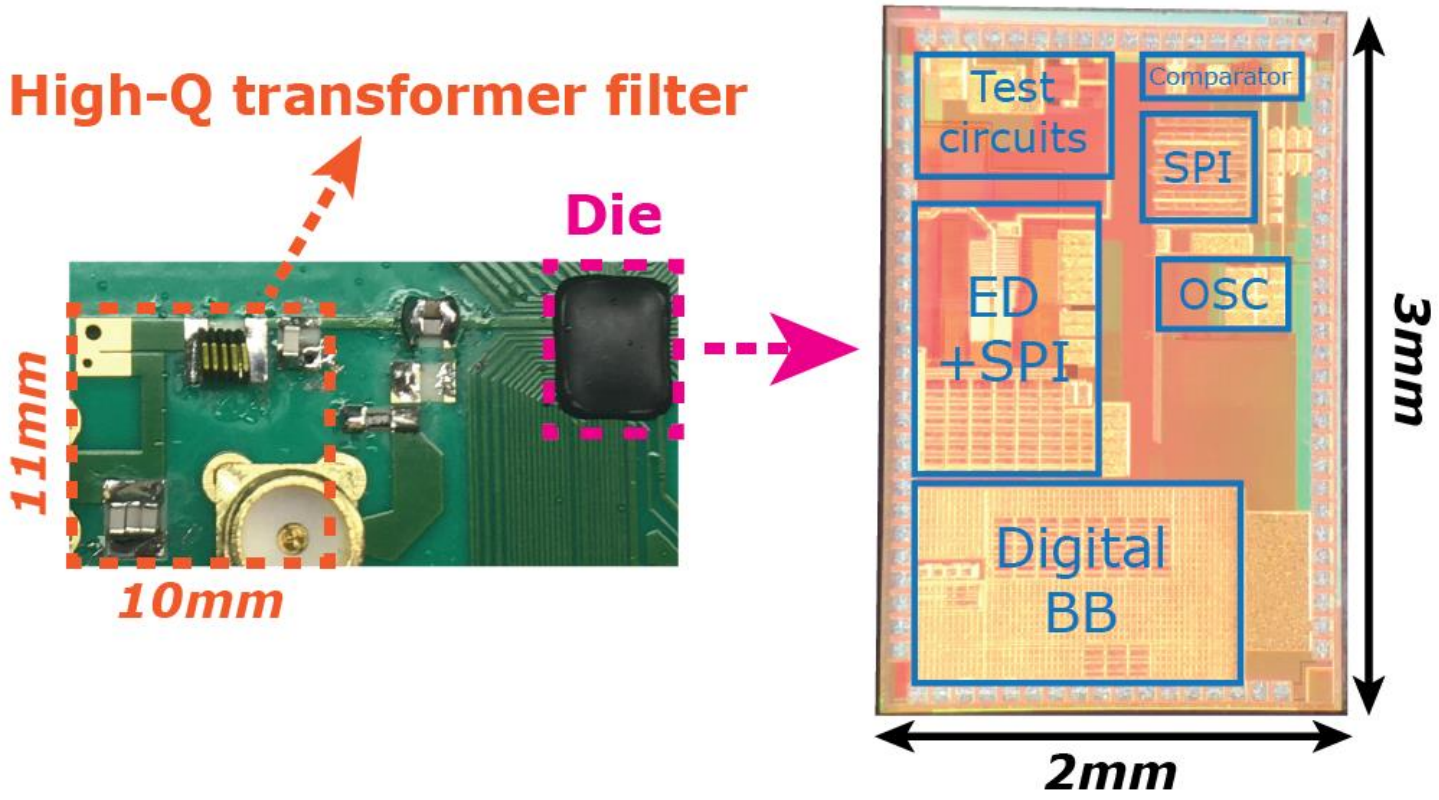
Reference circuit eliminated

Proposed pseudo-balun ED schematic



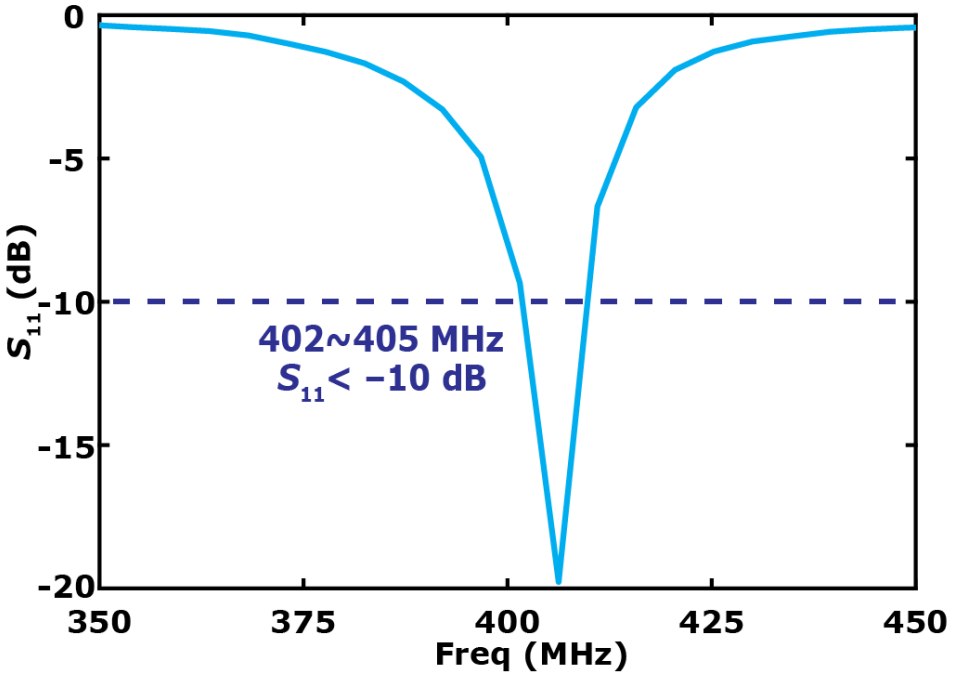
- Active-inductor biasing as output load
  - High R_{out} and thus high conversion gain
- Binary-weighted tuning cells for PVT
- Larger transistors to further reduce *1/f* noise
  - Less C_{in} penalty compared to CS input
- 1.8 nW; k_{ED}=301.2(1/V)

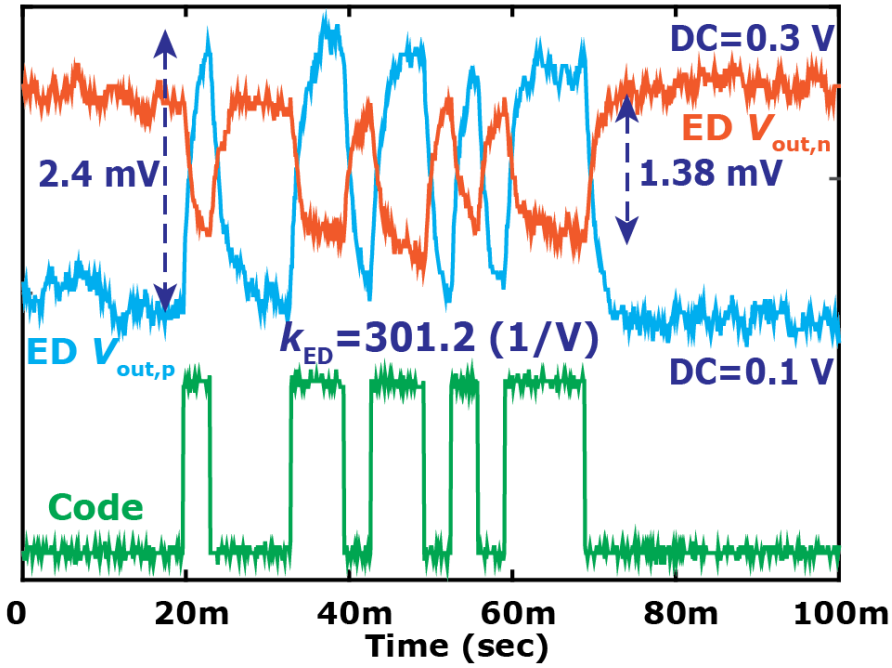
Board and die photo



- GF 180 nm CMOS SOI process
- RO4003 substrate

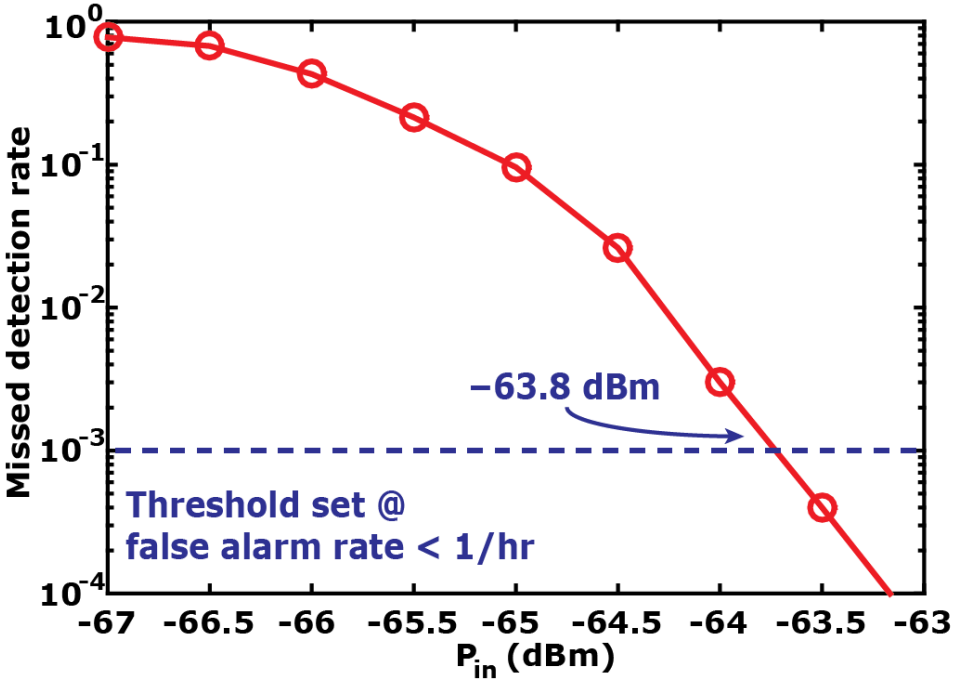
Measurement results

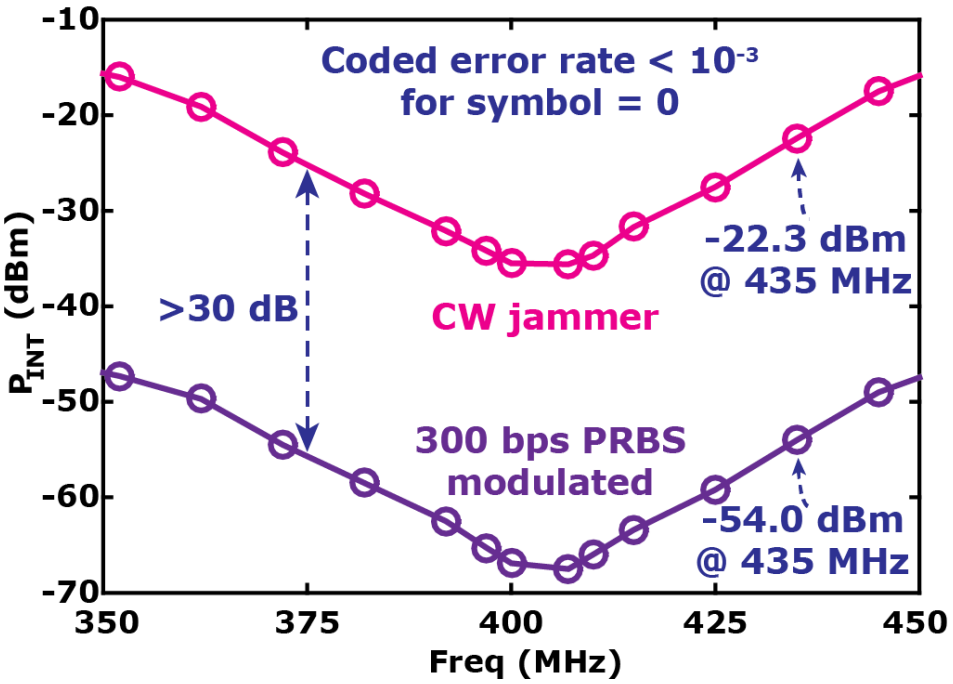




- Input S_{11} well matched across MICS band
- ED pseudo-differential output waveforms

Measurement results



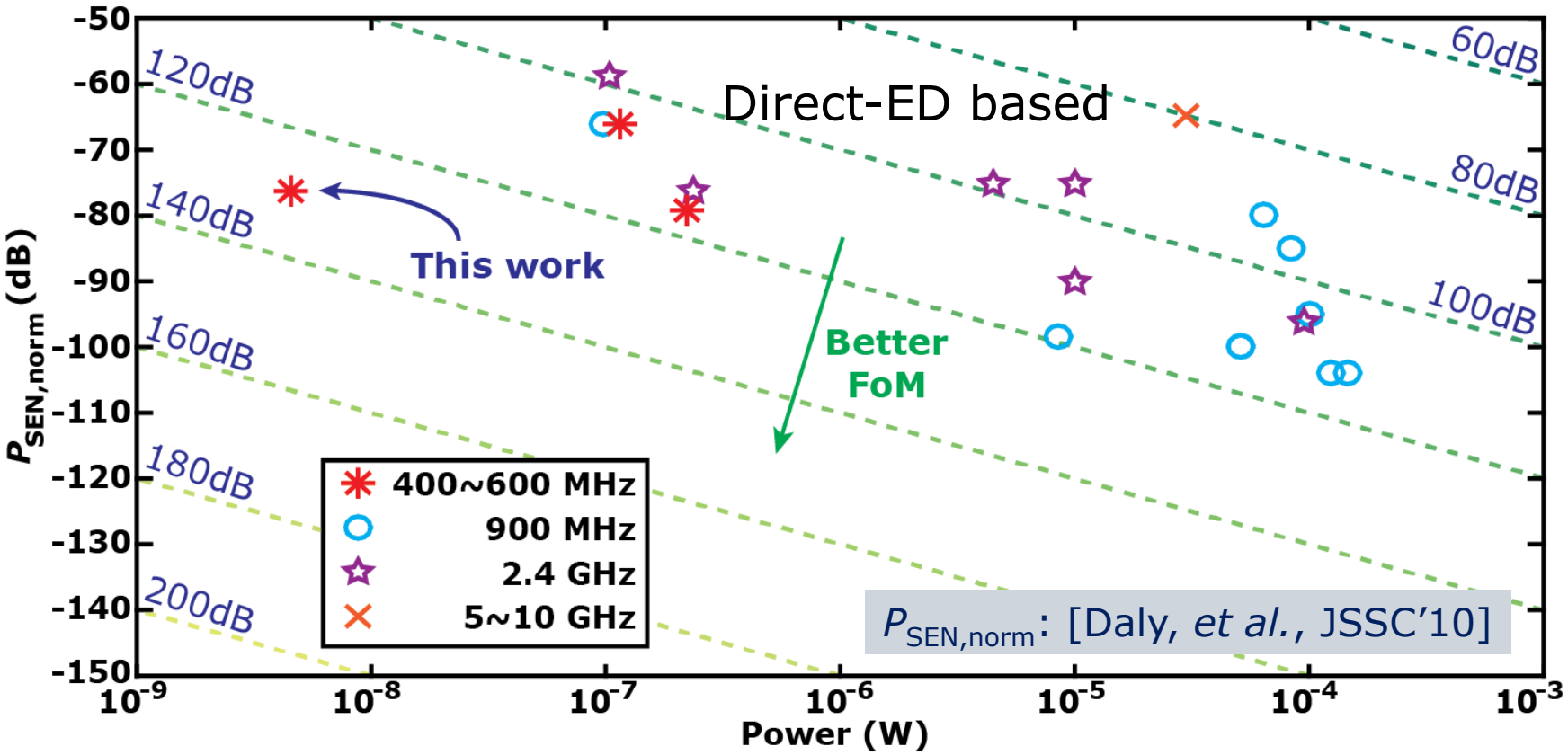


- –63.8 dBm sensitivity for MDR≤10^{-3}
- >–20 dBm CW and >–50 dBm PRBS jammers could be tolerated @ 50 MHz offset w/o false alarm

Comparison to the state-of-the-art

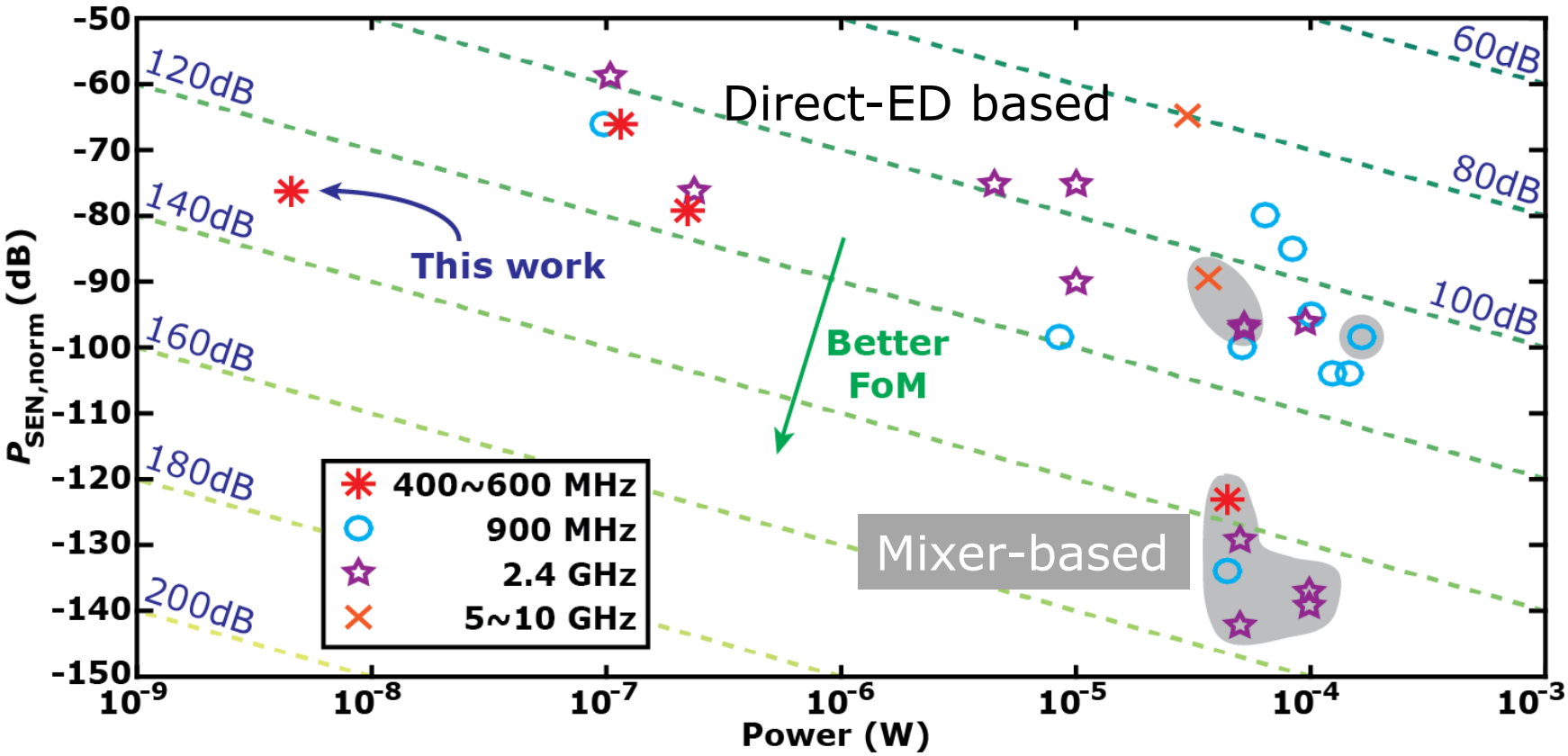
	RFIC'12	ISSCC'16	ISSCC'17	CICC'13	**This work**
Technology	130 nm	65 nm	180 nm	130 nm	**180 nm**
Supply	1.2 V	1 / 0.5 V	0.4 V	1.2 / 0.5 V	**0.4 V**
Data Rate	100 kbps	8.192 kbps	0.3 kbps	12.5 kbps	**0.3 kbps**
Passive Gain	12 dB	N/A	25 dB	5 dB	**18.5 dB**
ED Type	Active CS single-ended	Passive Dickson single-ended	Active CS single-ended	Passive Dickson single-ended	**Active CG pseudo-balun**
ED Power	23 nW	0	2.1 nW	0	**1.8 nW**
ED R_{in} @ RF	505.6 Ω	N/A	10 kΩ	76.3 Ω	**30 kΩ**
k_{ED} (1/V)	112.2	N/A	180.8	N/A	**301.2**
k_{ED}/P_{ED} (1/V·nW)	4.9	N/A	86.1	N/A	**167.3**
Comp. Ref.	ED replica	RC LPF	Ref. ladder	N/A	**None**
Carrier Freq.	915 MHz	2.4 GHz	113.5 MHz	403 MHz	**405 MHz**
Sensitivity	–41 dBm	–56.5 dBm	–69 dBm	–45 dBm	**–63.8 dBm**
RX Power	98 nW	236 nW	4.5 nW	116 nW	**4.5 nW**

Comparison to WuRXs (f_{RF}>400 MHz)



- FoM (dB)=$-P_{SEN,norm}-10\log(P_{DC}/1mW)$
- Best FoM among direct-ED based WuRXs

Comparison to WuRXs (f_{RF}>400 MHz)



Some mixer-based WuRXs have better FoM, albeit at much higher DC power

Conclusions

- For event-driven applications with low-average throughput, WuRXs extend system lifetime
  - Design targets: Low power and high sensitivity
- The proposed design breaks the trade-off between sensitivity and carrier frequency by using:
  - Active ED with CG input to reduce input capacitance
  - Current-reuse pseudo-balun ED to improve 1.5 dB sensitivity without a power penalty
- Result:

  A 400 MHz, 4.5 nW, –63.8 dBm sensitivity WuRX

Acknowledgment

- This work is supported by the Defence Advanced Research Projects Agency (DARPA) under contract No. HR0011-15-C-0134

- Mentor Graphics for the use of Analog FastSPICE tool (AFS)