A 4.4µW 2.5kHz-BW 92.1dB-SNDR 3rd-Order VCO-based ADC with Pseudo Virtual Ground Feedforward Linearization

Corentin Pochet and Drew A. Hall

University of California San Diego (UCSD)

Short Bio – Corentin Pochet

B.Sc. & M.Sc. **Université Libre de Bruxelles**

2011 - 2016 Electrical Engineering

Ph.D. **University of California San Diego**

2016 - Now Electrical Engineering, Advisor: Drew Hall

Mixed-signal intern **Qualcomm, San Diego**

Summer 2021

Awards Henri Benedictus BAEF Fellow

Research focus Low-power sensor front-ends and time-based ADCs

ADC for Internet of Things (IoT)

Smart distributed sensors require:

1. Low-power system (<100 μW)
2. High accuracy front-end (SNR>90 dB)
3. Edge processing

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Edge processing → Highly digital systems

- **Best implemented in advanced nodes**
- **Complicates design of the front-end circuit**
  - Lower supplies, lower intrinsic gain, ...

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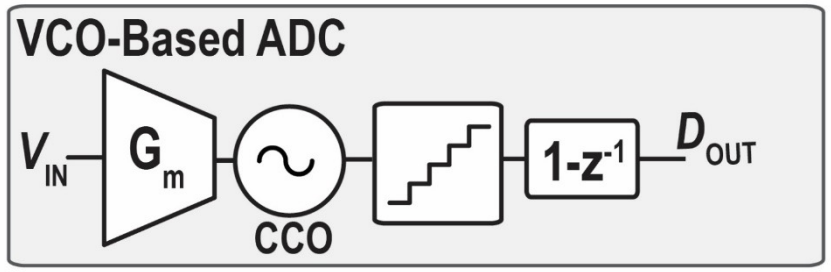
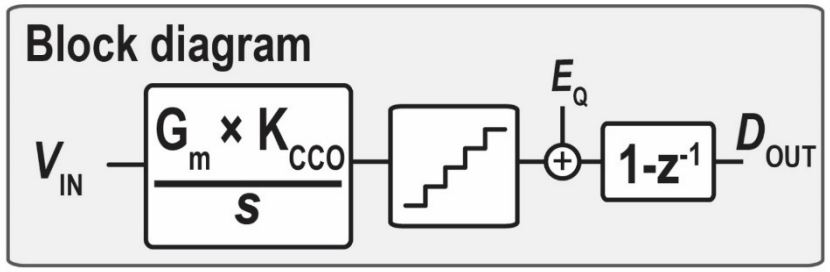
Need innovative architectures for high-precision ADCs

VCO-based ADCs

Pros:

- Continuous-time ΔΣ
- Open-loop noise-shaping
- High scalability with process





$$D_{OUT} = \underbrace{(G_m K_{CCO})}_{G_{ADC}} V_{IN} + E_Q(1-z^{-1})$$

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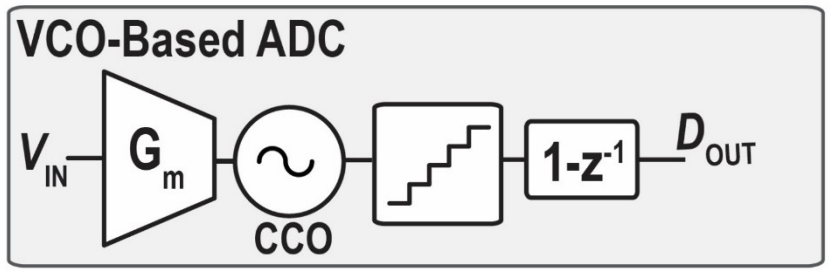

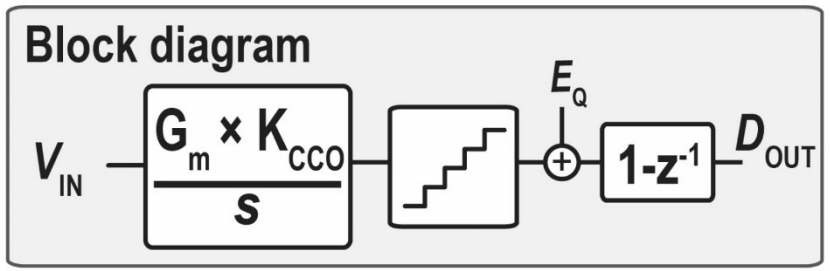

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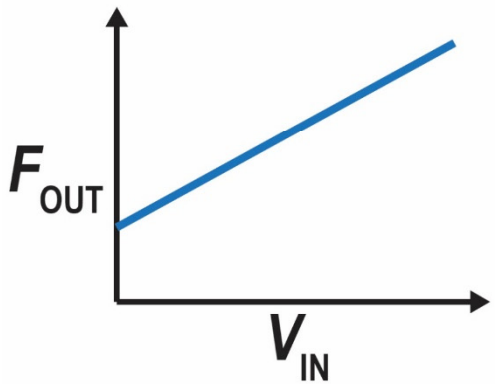
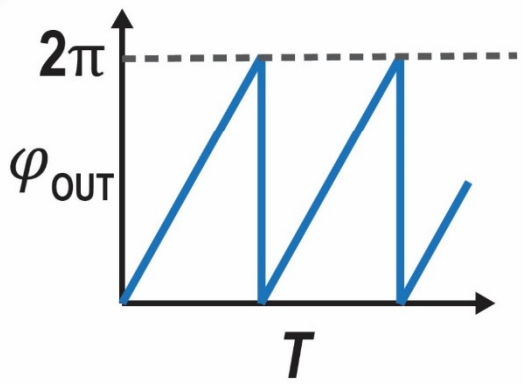
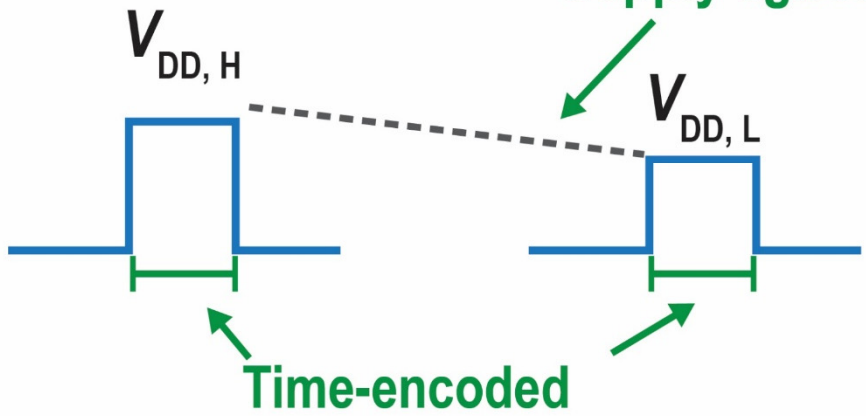
Ideal integrator in phase



$$F_{OUT} = \frac{d\varphi_{OUT}}{dt}$$



Supply agnostic



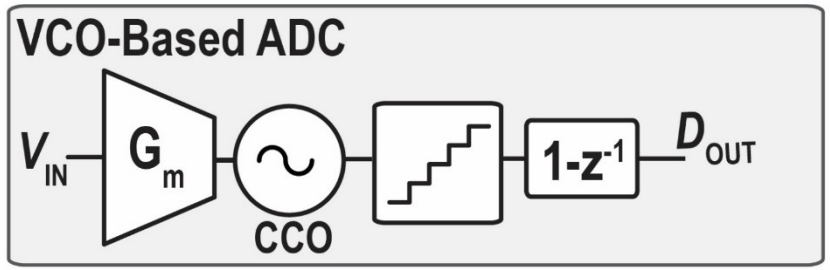
VCO-based ADCs

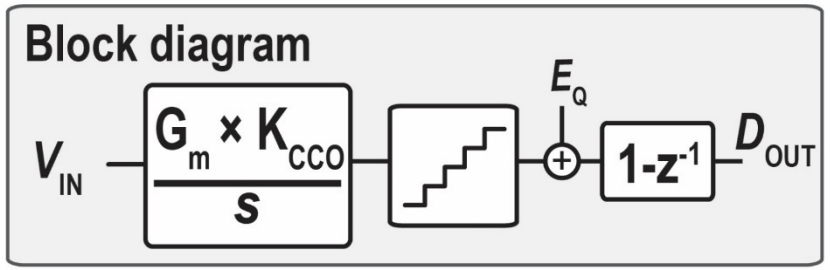
Pros:

- Continuous-time ΔΣ
- Open-loop noise-shaping
- High scalability with process

Cons:

- Very non-linear
- PVT dependent gain
- Limited to 1st-order noise-shaping





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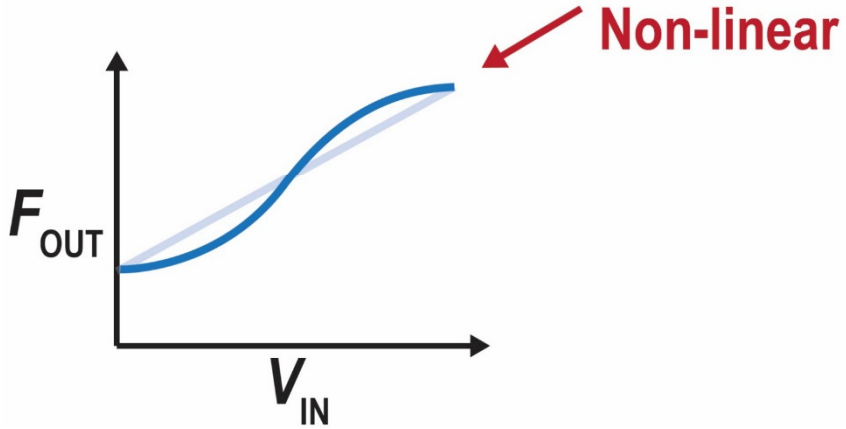

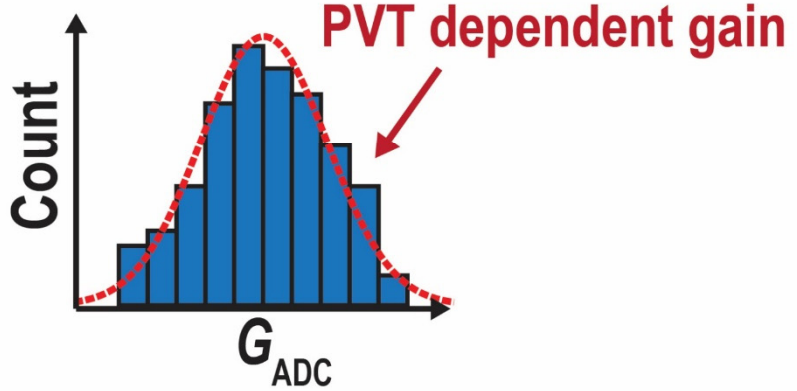

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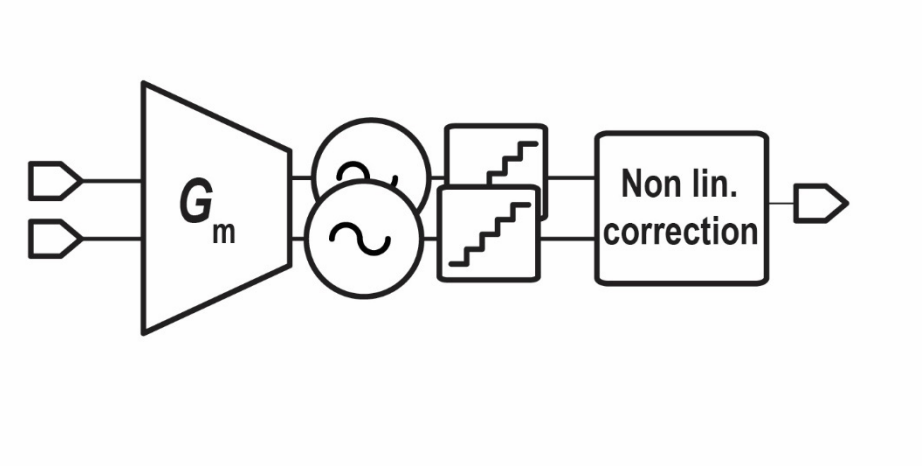
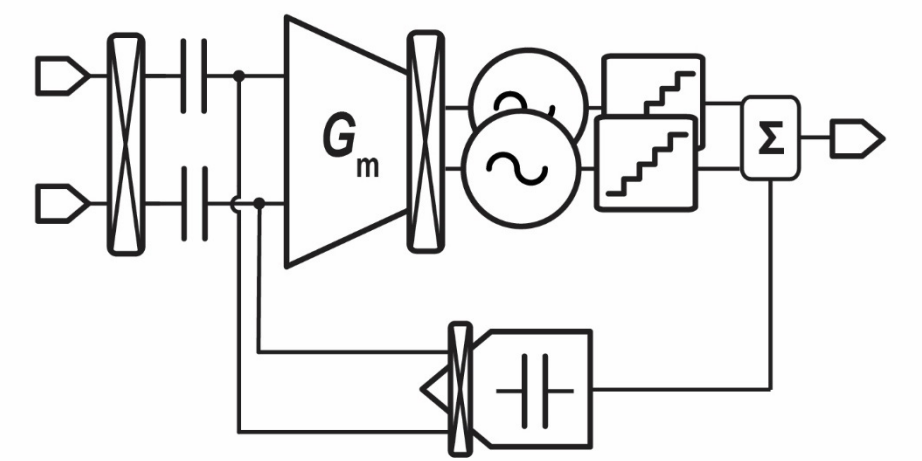
Prior VCO-based ADCs

Open-loop [Jiang *ISSCC '16*]



- ✓ **Highly digital**
- ✗ **Limited input range (<100 mV_{pp})**
- ✗ **Limited to 1st-order noise shaping (NS)**

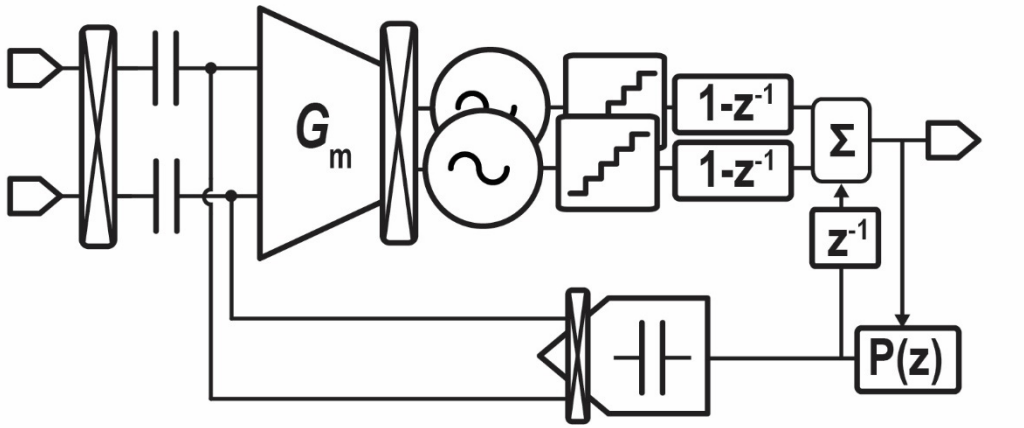
Closed-loop [Li *CICC '19*]



- ✓ **Good linearity**
- ✗ **Limited input range (<500 mV_{pp})**
- ✗ **Limited to 1st-order NS**

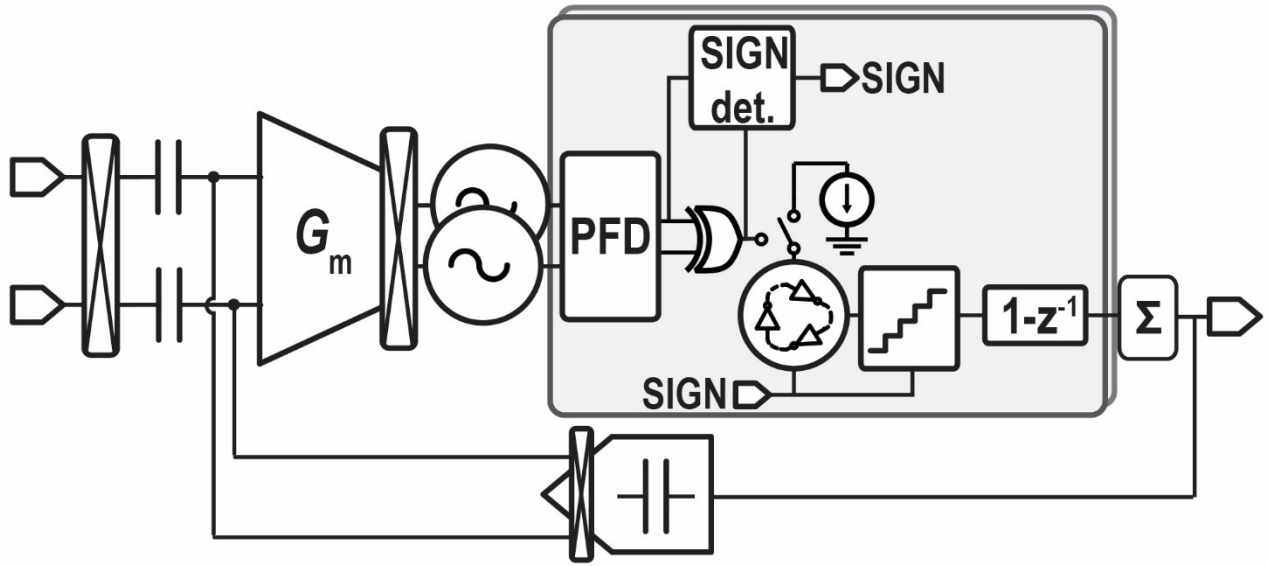
Prior VCO-based ADCs

DPCM-based correction [Huang *ISSCC '21*]



- ✓ Excellent linearity (>120 dB)
- × Large DAC (8b)
- × Limited to 1st-order NS

2nd-ord. VCO-only [Pochet *ISSCC '21*]

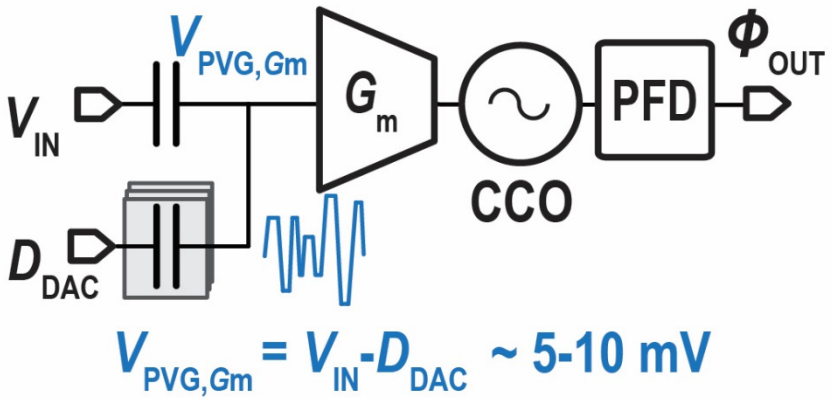


- ✓ Great linearity (>110 dB)
- ✓ 2nd-order NS
- × Sensitive to path mismatch

How to improve VCO-based ADCs?

Prior-art performance primarily limited by:

1. Input swing (< 500 mV_{pp})
2. Noise-shaping (< 2)
3. PVT sensitivity



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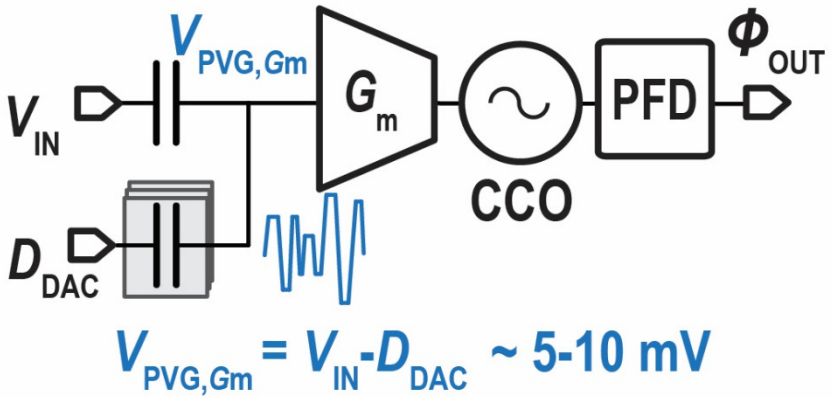

We propose an architecture that:

1. Allows for large input-swing (>1.5 V_{pp})
2. Enables higher order noise-shaping (3)
3. Is reliable across PVT

ADC specs: >90 dB SNDR, 2.5 kHz BW, and 3rd-order NS

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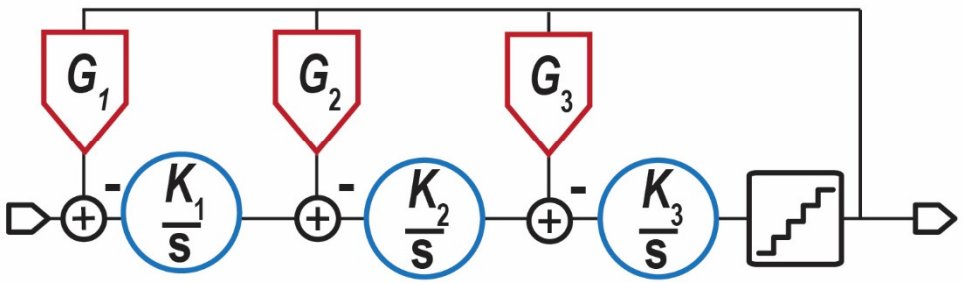
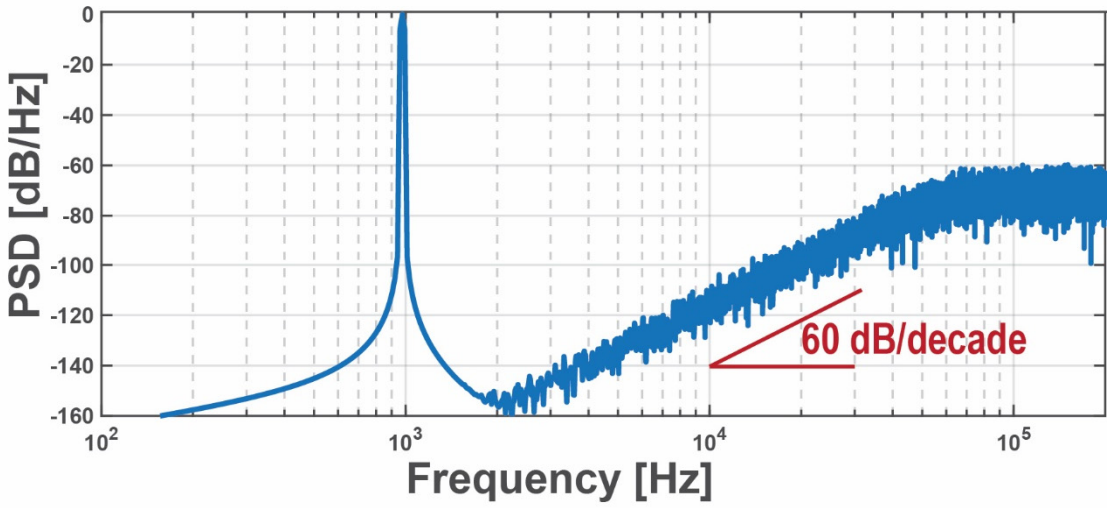
Standard CIFB Architecture

3rd-ord. CIFB architecture:

- ✓ Higher order noise shaping
- ✓ Good anti-aliasing

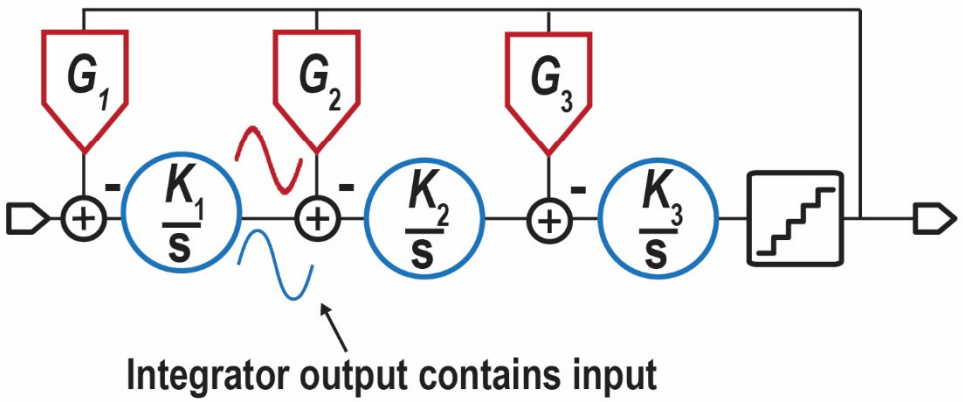


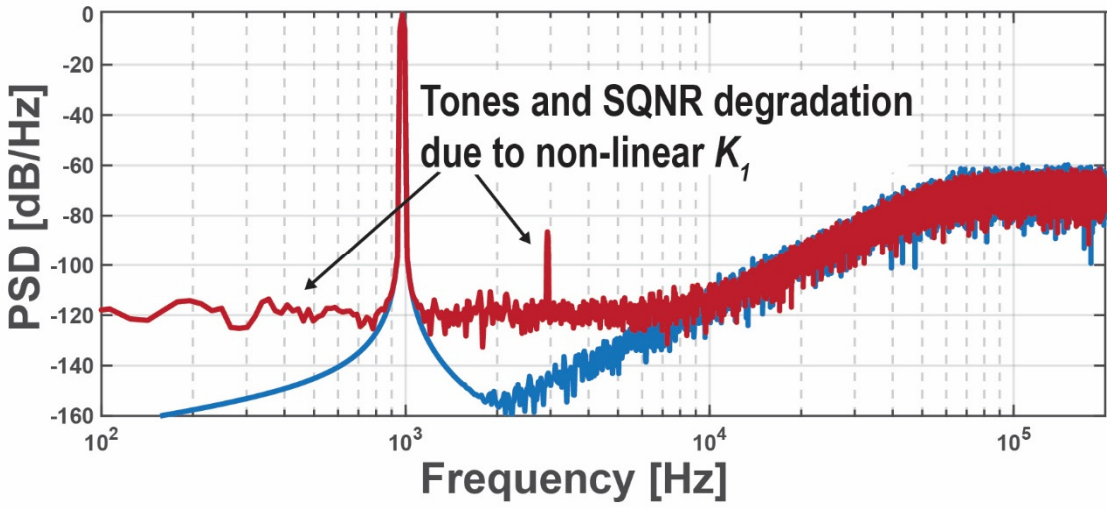


Standard CIFB Architecture

3rd-ord. CIFB architecture:

- ✓ Higher order noise shaping
- ✓ Good anti-aliasing
- ✗ Limited coefficient scaling
- ✗ Tonal integrator output

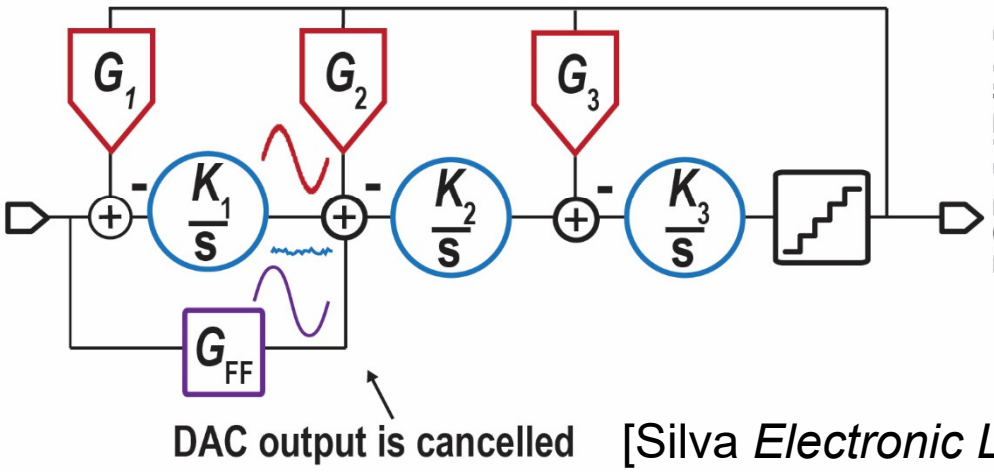


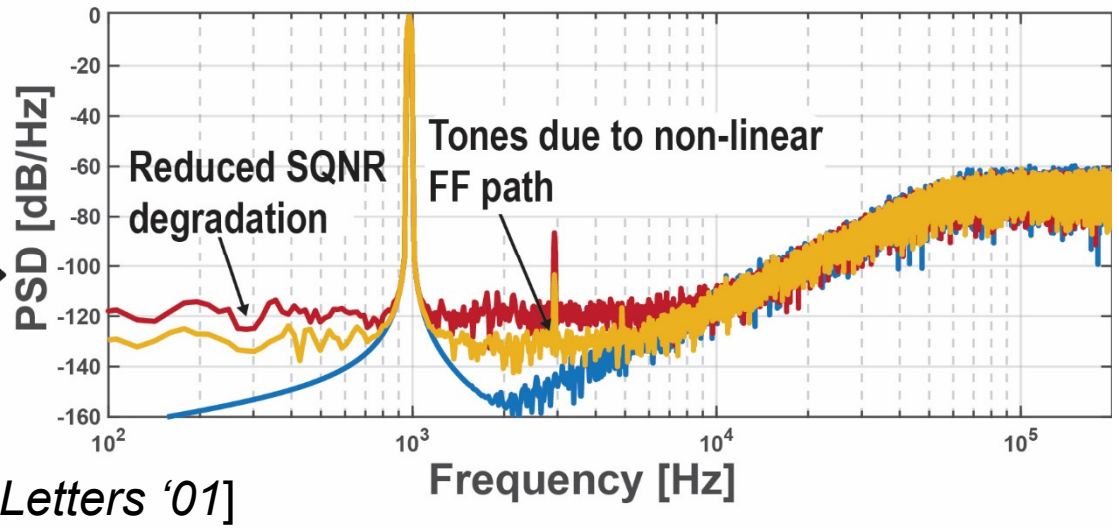


CIFB w/ Input Feedforwarding (FF)

Key idea: FF path cancels DAC output → Integrator is free of input

- ✓ **Reduces SQNR degradation**
- ✓ **Improves coefficient scaling**





[Silva *Electronic Letters '01*]

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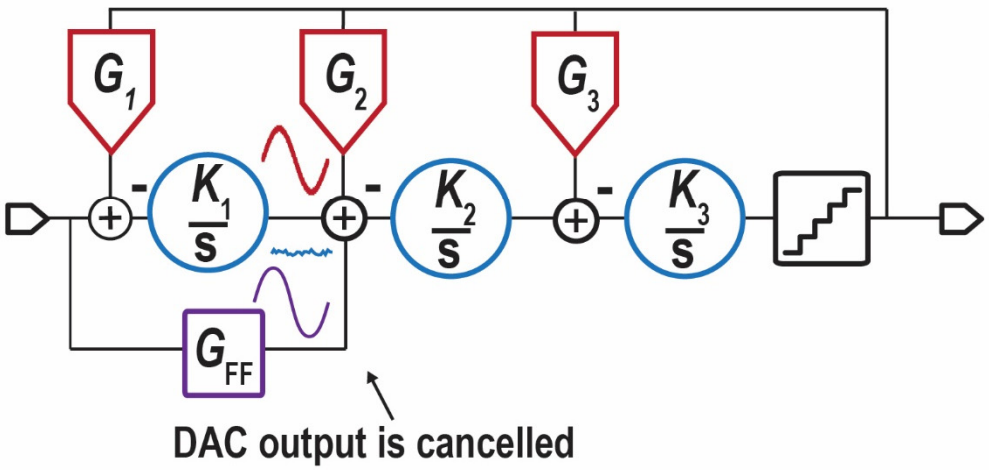
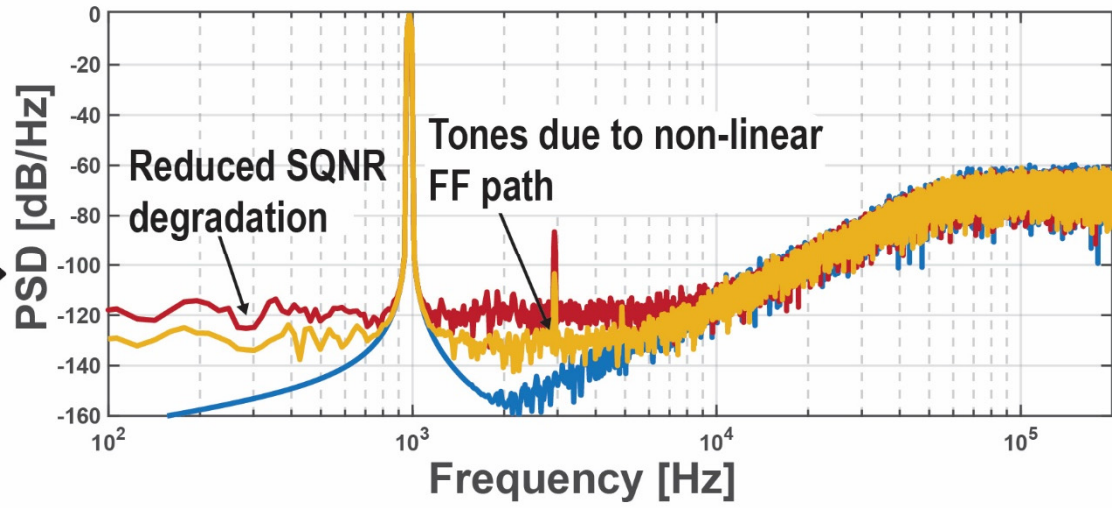
- ✗ **Reduces anti-aliasing**
- ✗ **Stringent FF path linearity**





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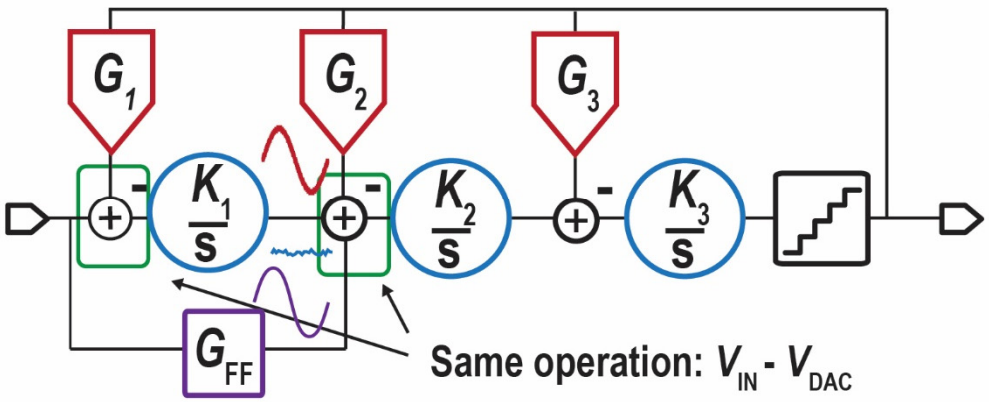
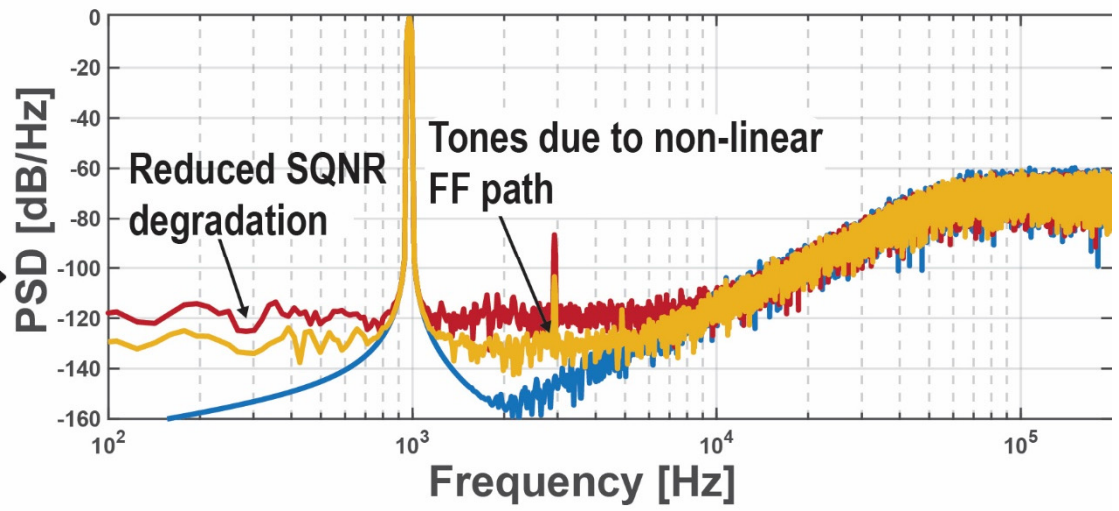
Observation:

Both DAC nodes perform input signal cancellation

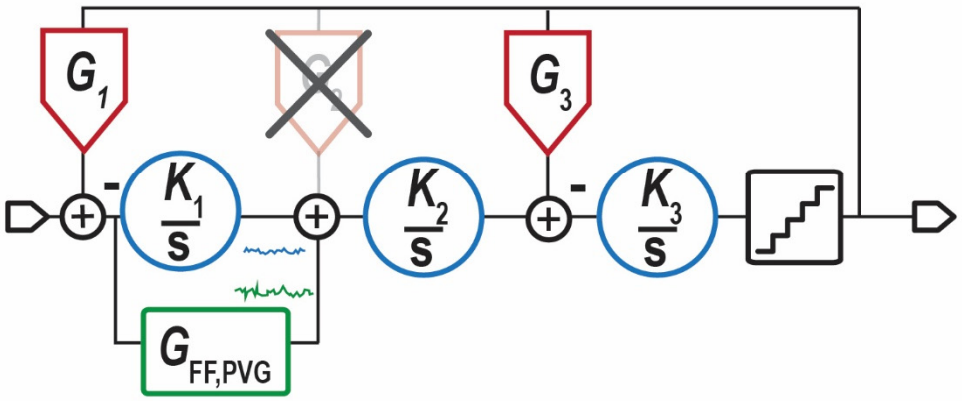


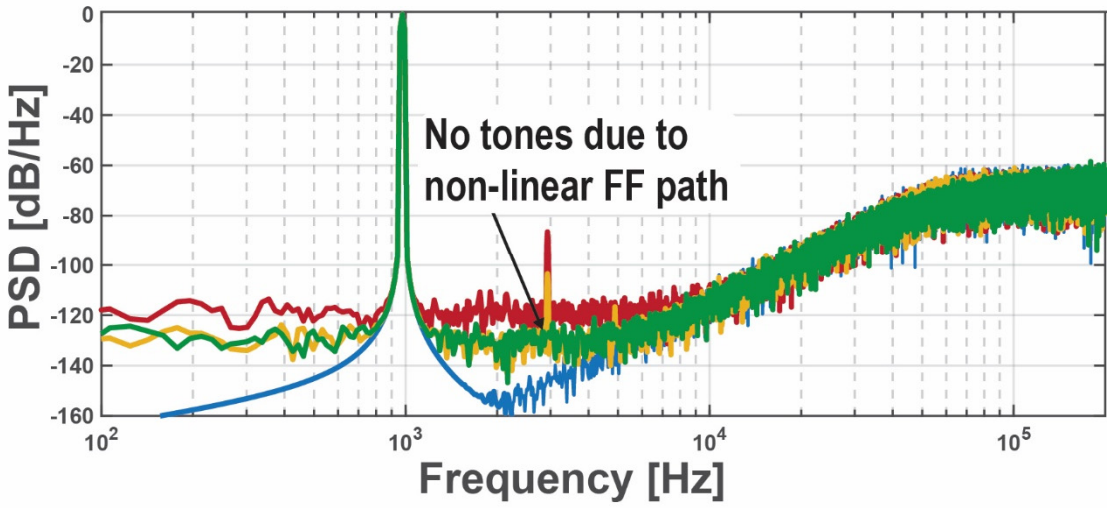


Pseudo Virtual Ground (PVG) FF

Key idea: Feedforward result of input and DAC cancellation

- ✓ Reduces SQNR degradation
- ✓ Improves coefficient scaling
- ✓ Relaxes feedforward path linearity
- ✓ Removes feedback DAC





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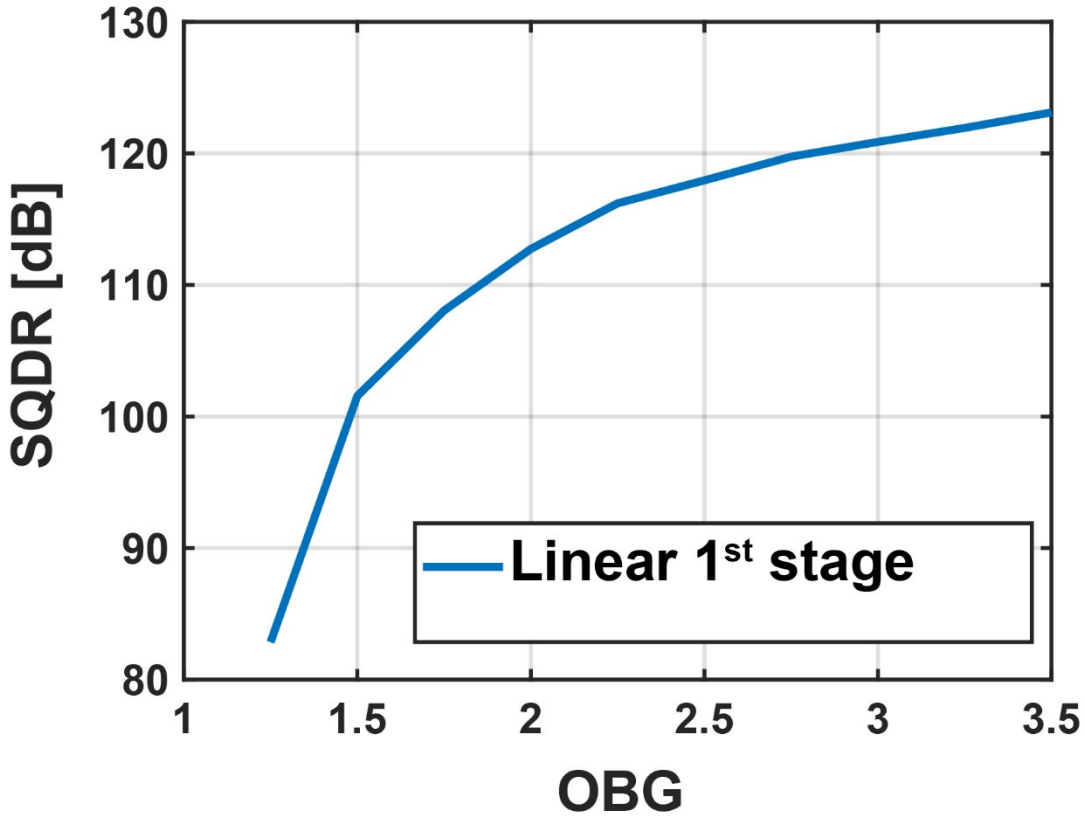
Coefficient Selection

Filter parameters:

Loop-filter order: 3

Oversampling ratio (OSR): 80

Out-of-band gain (OBG): **?**



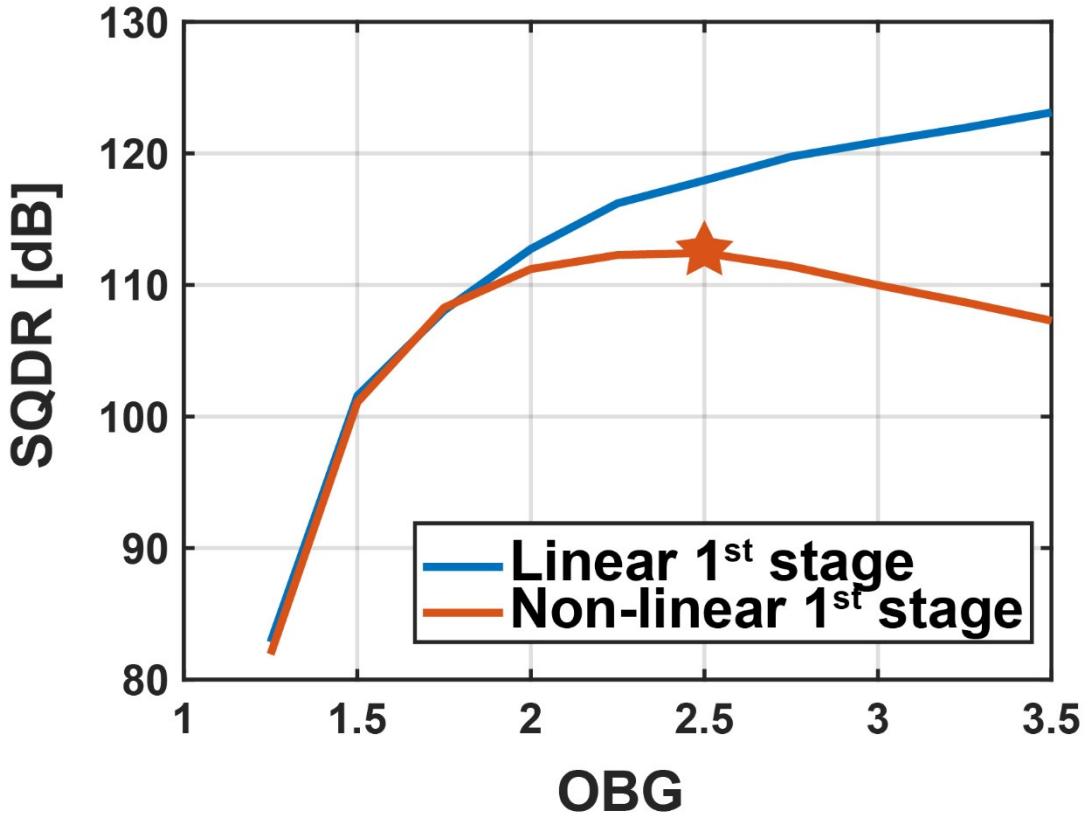
Coefficient Selection

Filter parameters:

Loop-filter order: 3

Oversampling ratio (OSR): 80

Out-of-band gain (OBG): **2.5**

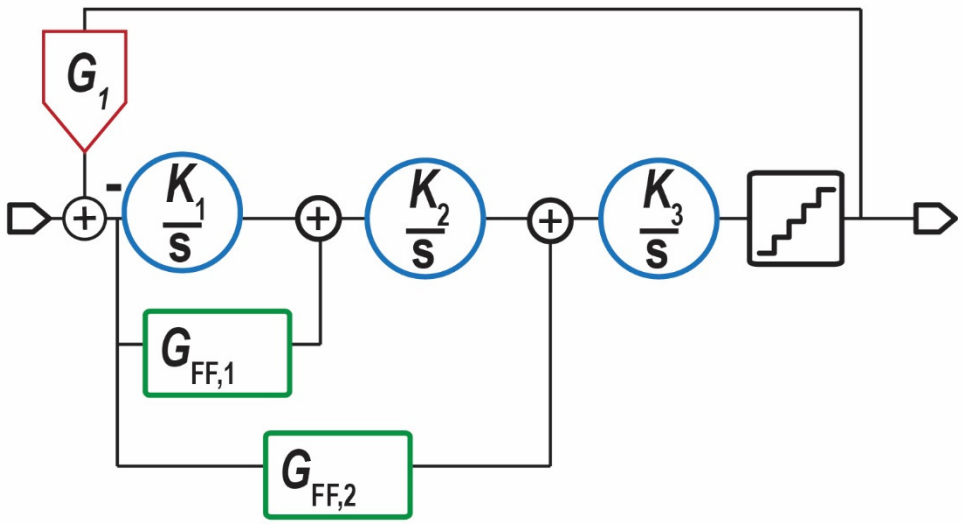


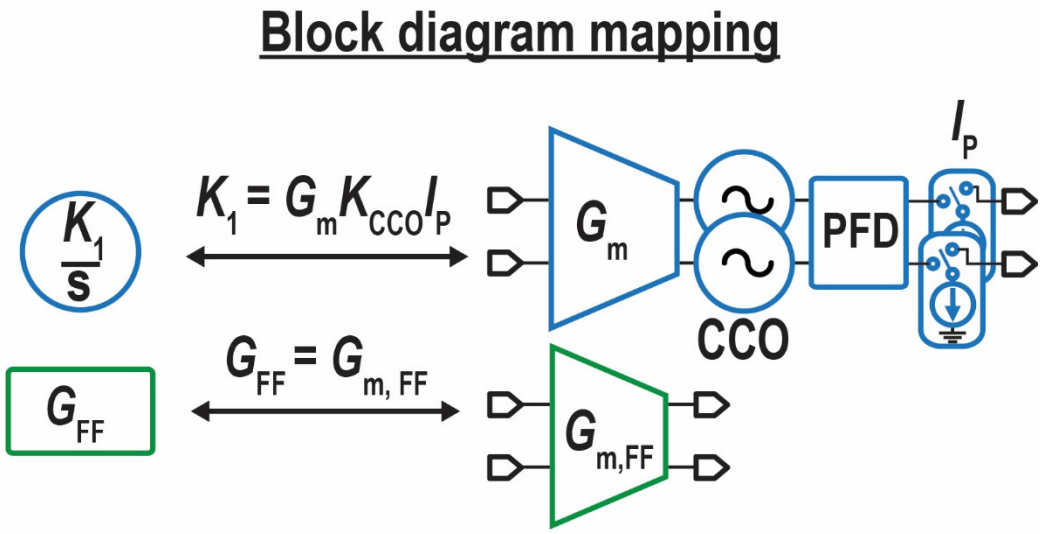
Loop coefficients obtained from the CT mapping of the DT loop-filter

Architecture Mapping

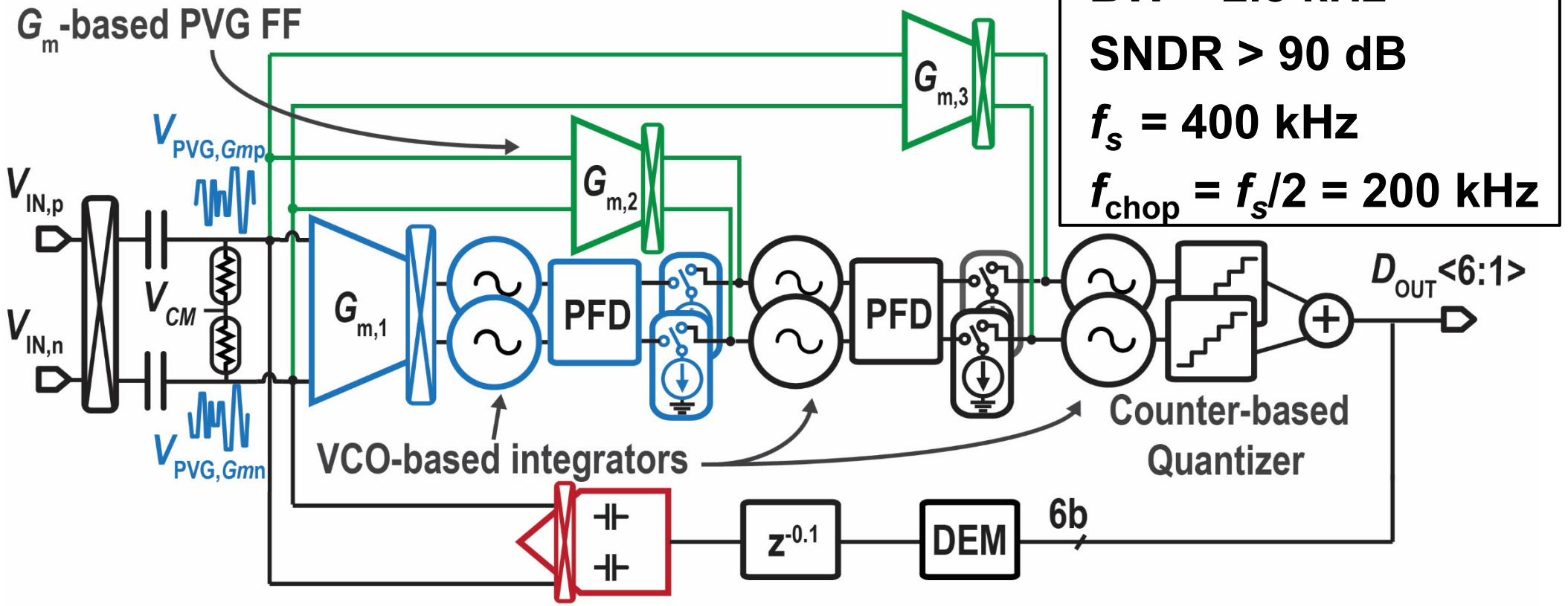
Block diagram mapping:

- Integrators mapped to G_m-CCO integrator with PFD phase detector driving a current pulser
- FF path implemented in the current domain with G_m-cells
- Coefficients scaled to guarantee $\Delta\phi < 2\pi$ between CCOs





Proposed Architecture



V_{DD} = 0.8 V
BW = 2.5 kHz
SNDR > 90 dB
f_s = 400 kHz
$f_{chop} = f_s/2$ = 200 kHz

High DR 3rd-order VCO-only ADC

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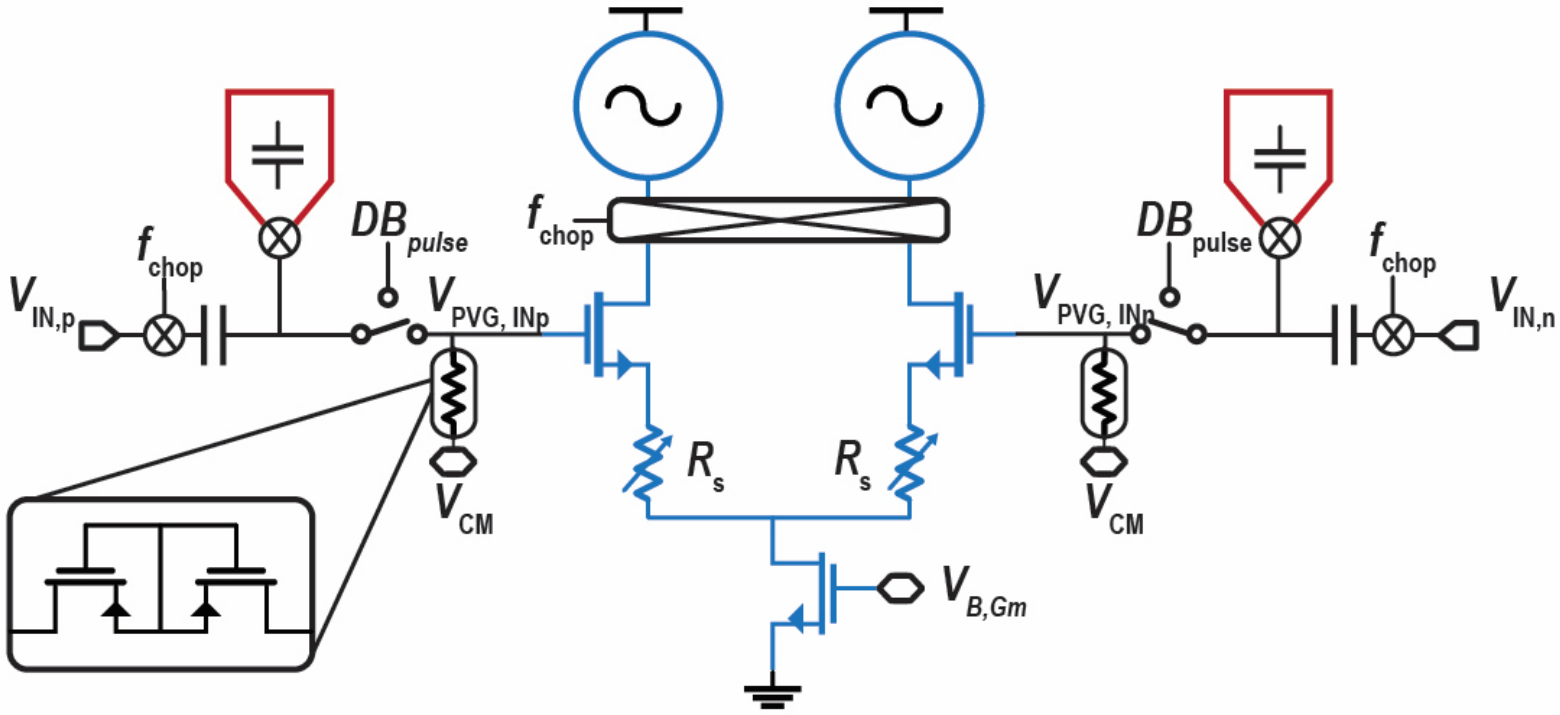
1st G_m-cell Implementation

G_m-cell source degenerated for increased linearity



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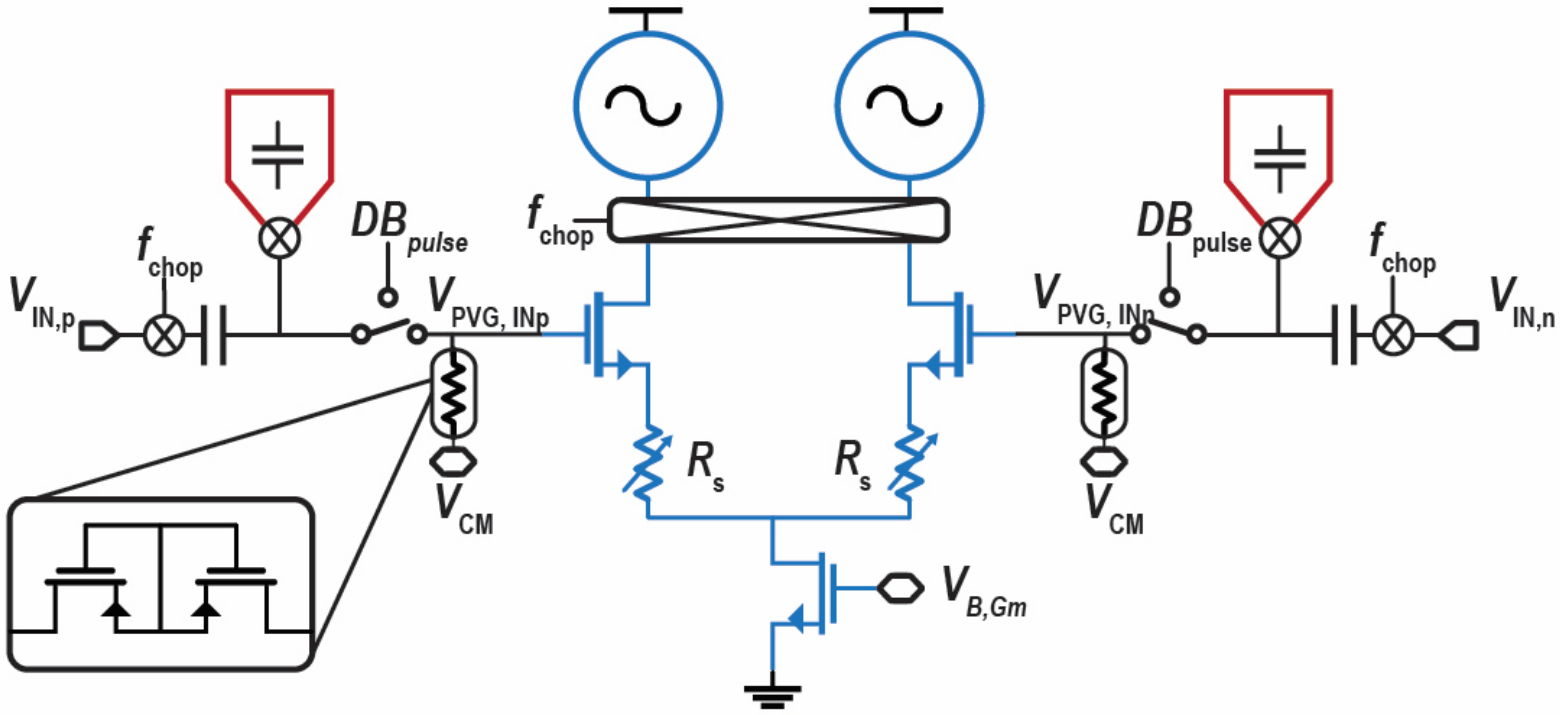

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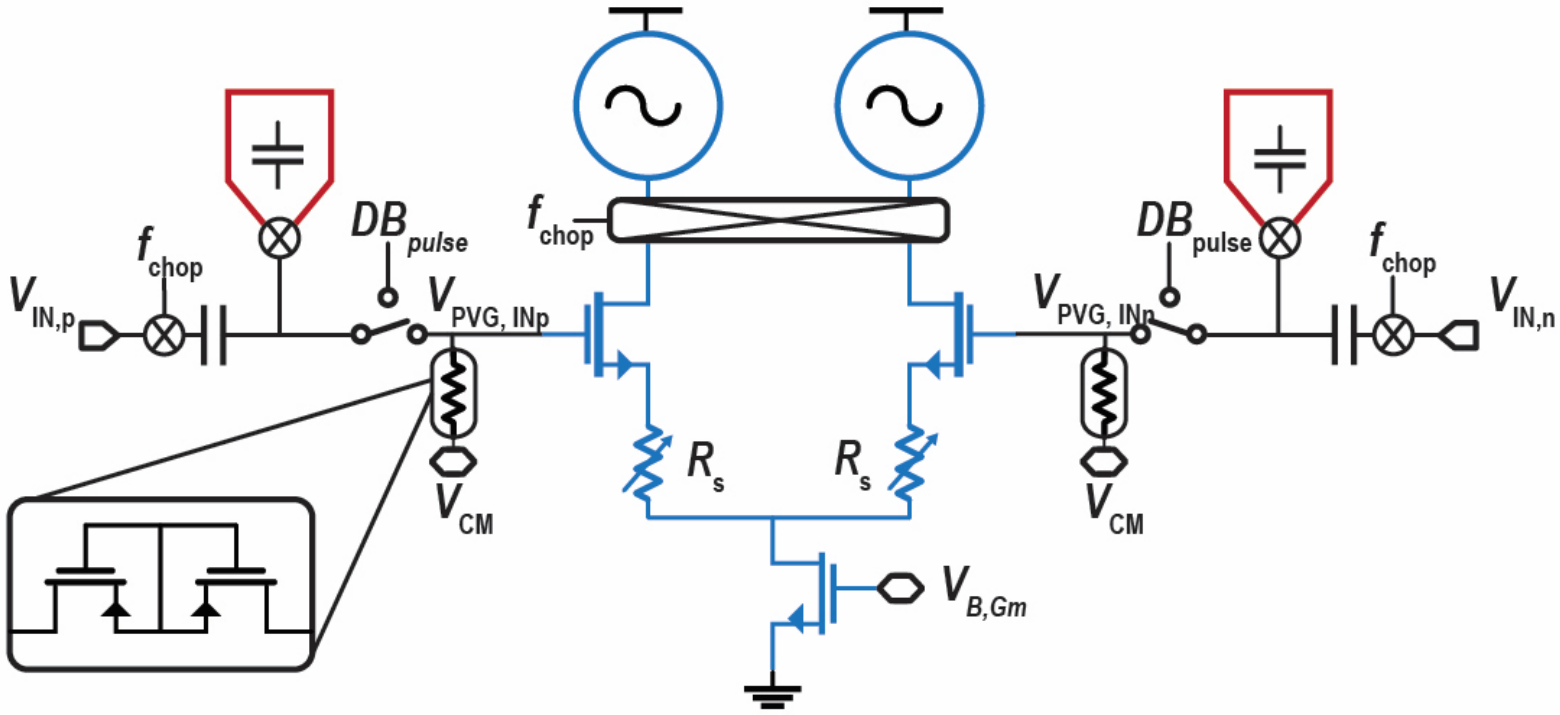

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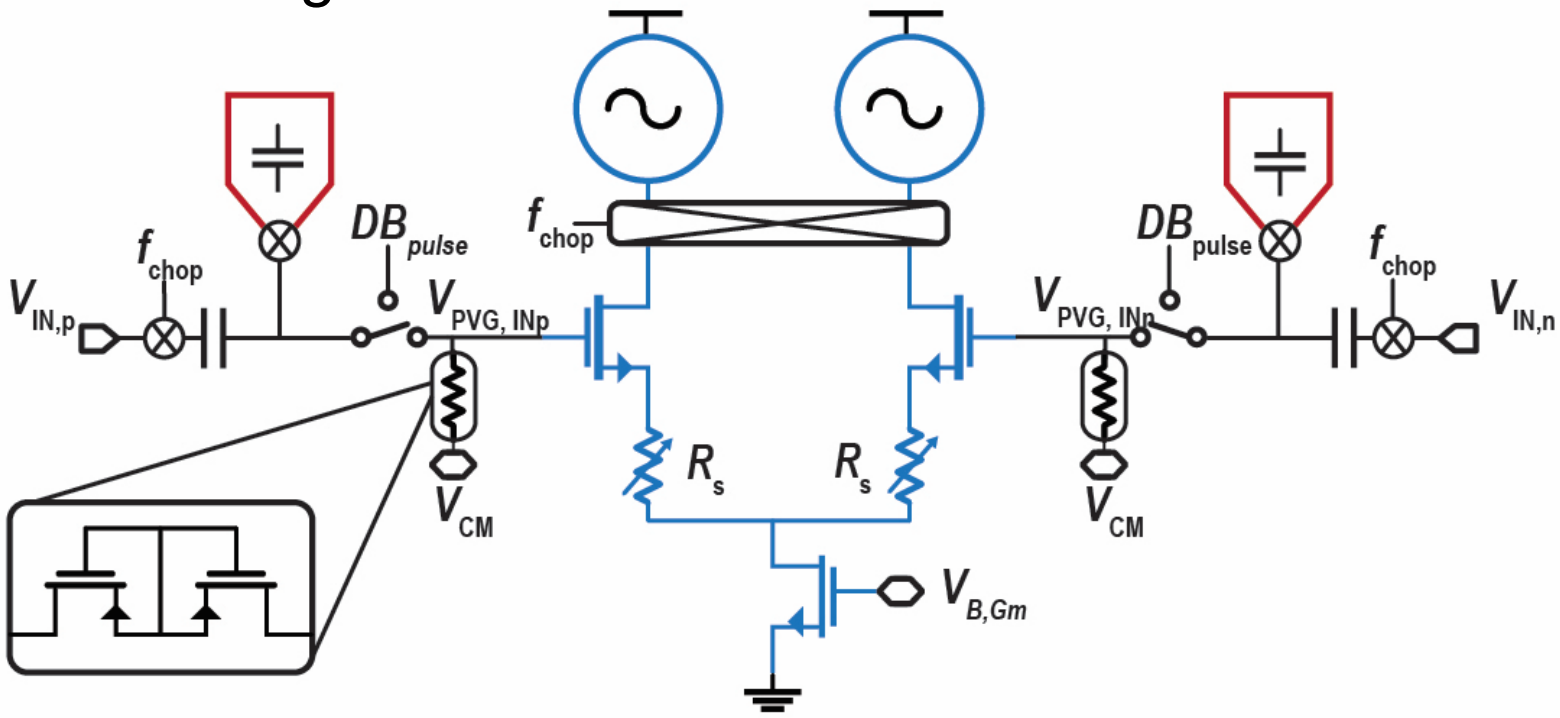
- Thick oxide devices for low gate leakage
- Pseudo-resistor biasing



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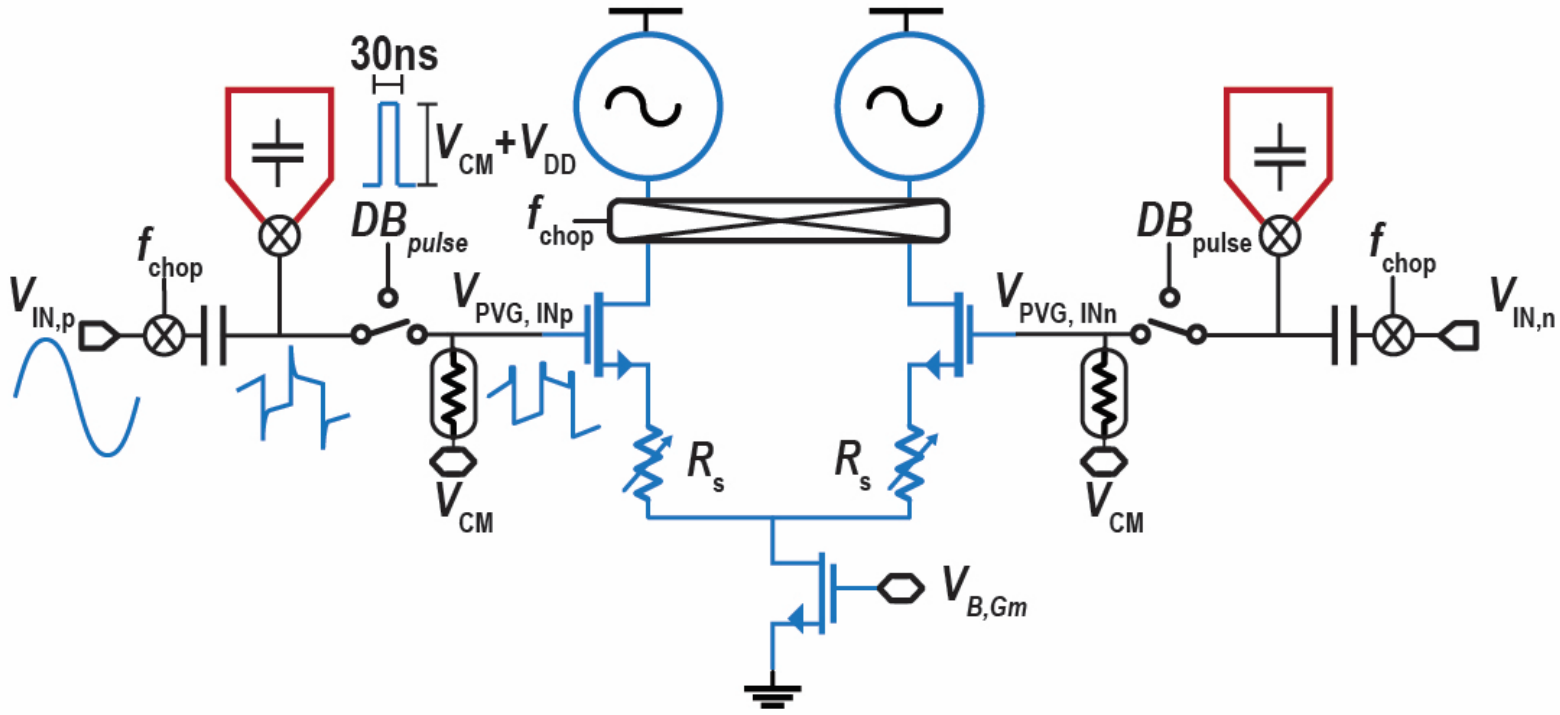
Chopping improves CMRR and upmodulates offset and flicker noise

- CDAC chopping → differential-mode chopping artifacts



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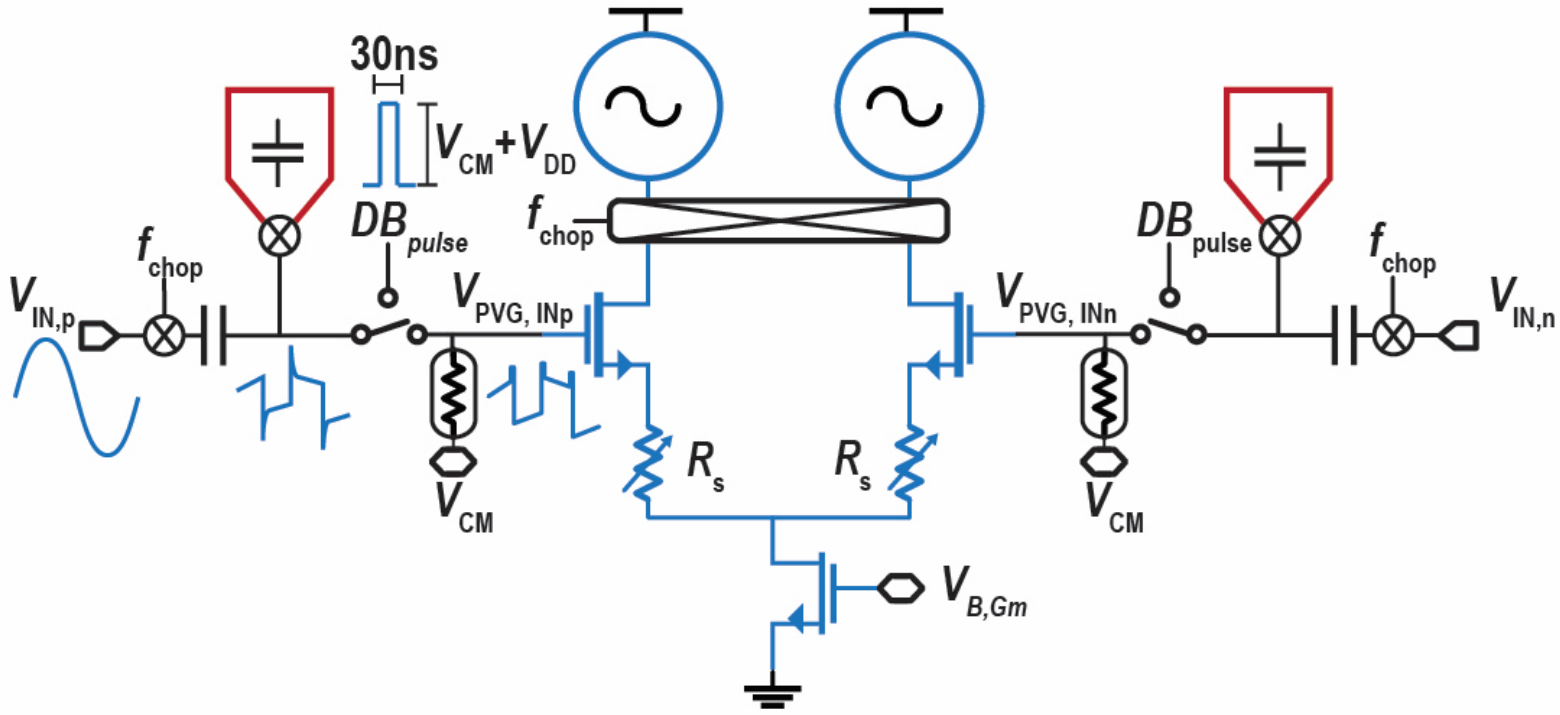
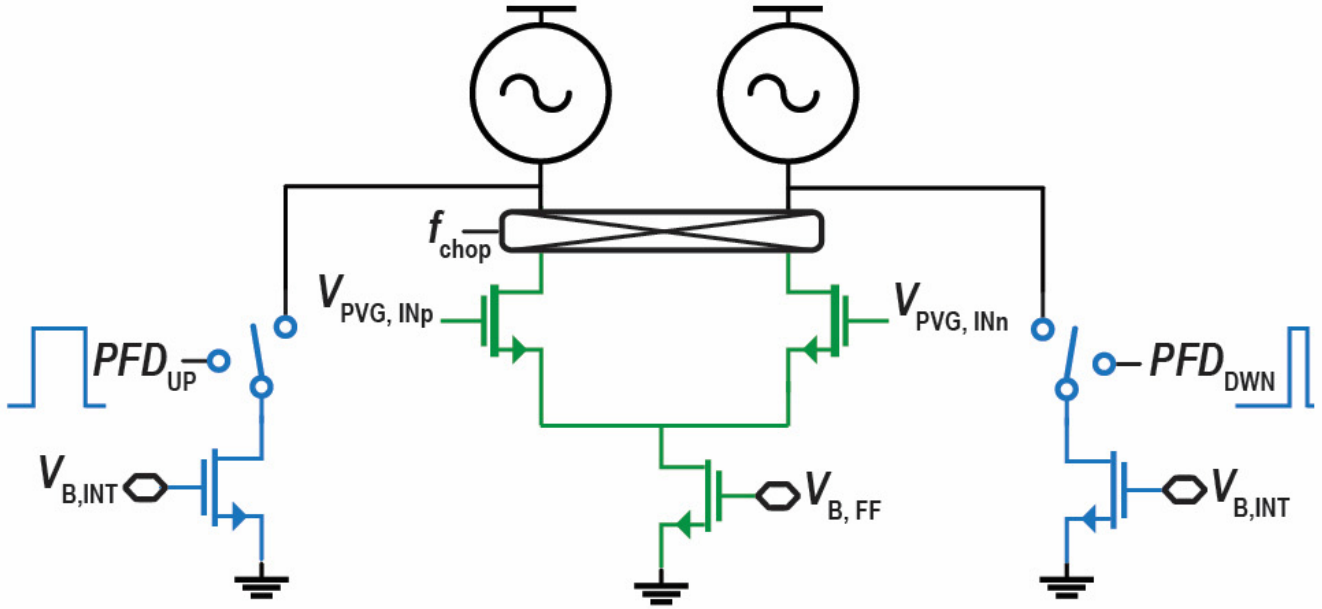
- Dead-band switch converts artifacts to common-mode



2nd & 3rd G_m-cell Implementation

G_m-cell composed of feedforward and current pulser

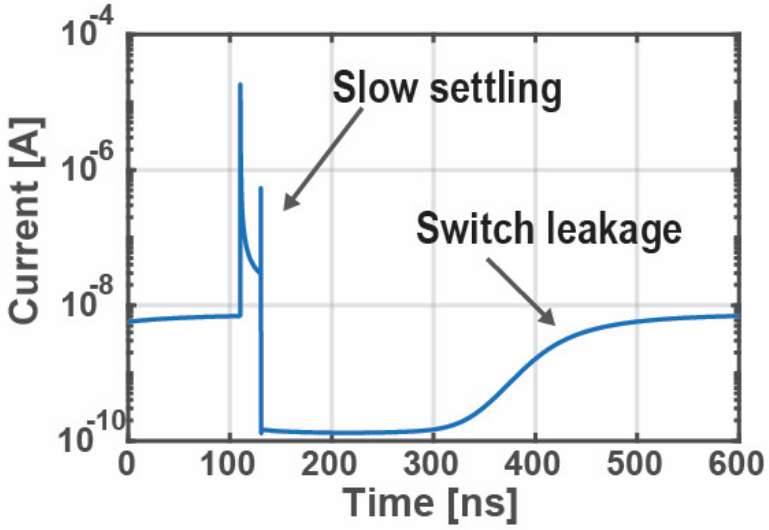
- Differential pair with $g_m/I_D > 20$
- G_m-cell current chopped down to match path polarity
- Current domain path summation directly into the CCO

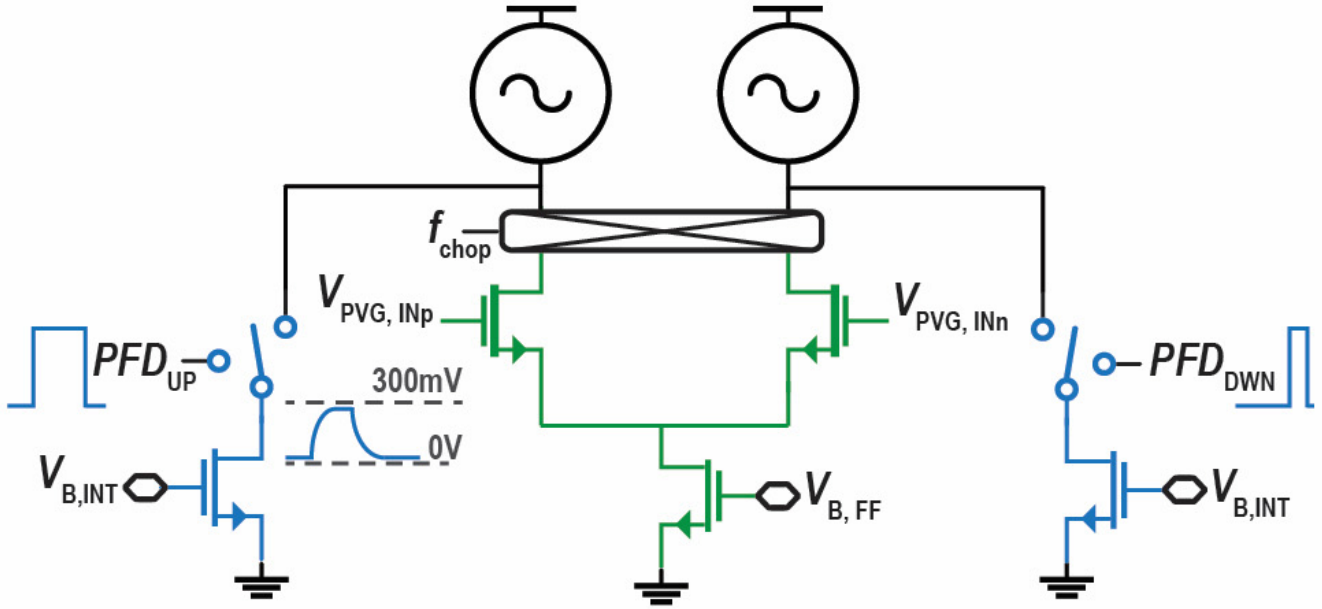


2nd & 3rd G_m-cell Implementation

Current pulser implementation suffers from:

- Slow settling time due V_{DS} = 0 at turn-on time
- Large V_{DS} across the switch when off causes leakage

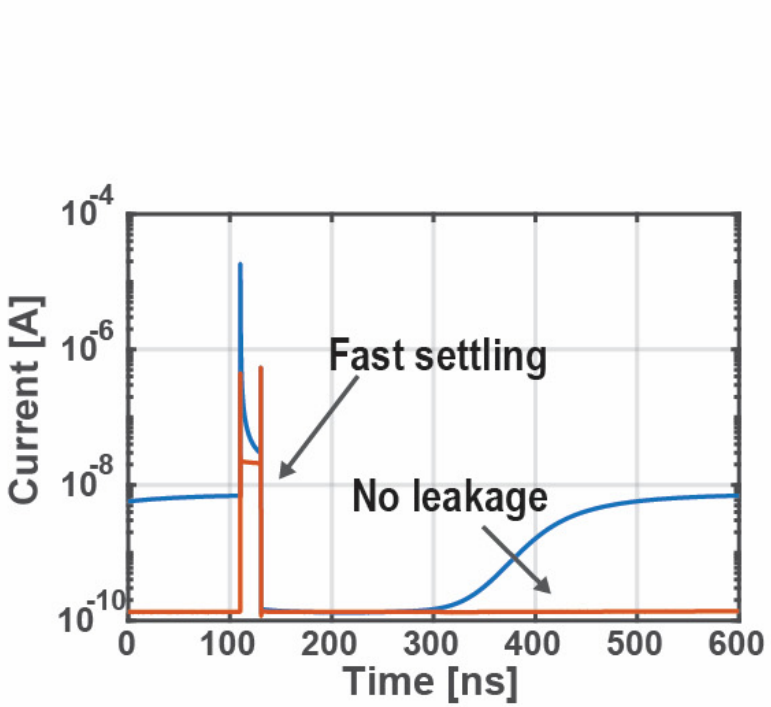


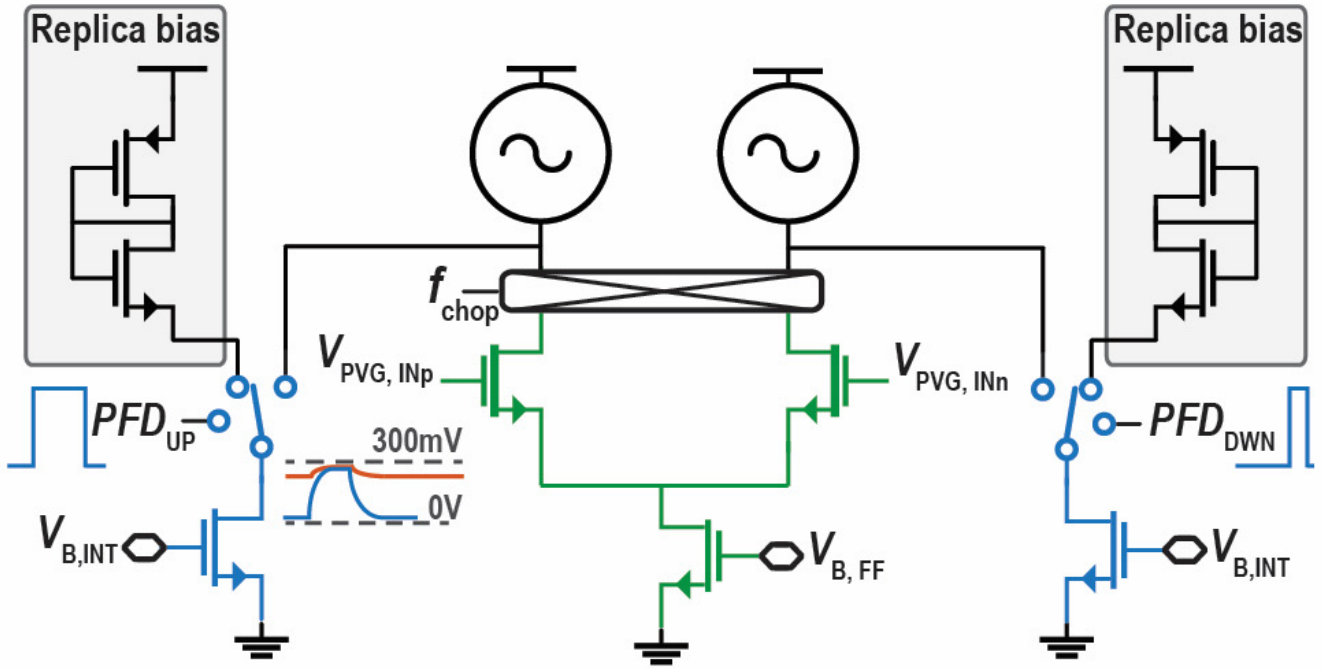


2nd & 3rd G_m-cell Implementation

Current shunted to a CCO replica solves the issues:

- Fast settling due to constant current source V_{DS}
- Low leakage due to near-zero switch V_{DS} in the off state

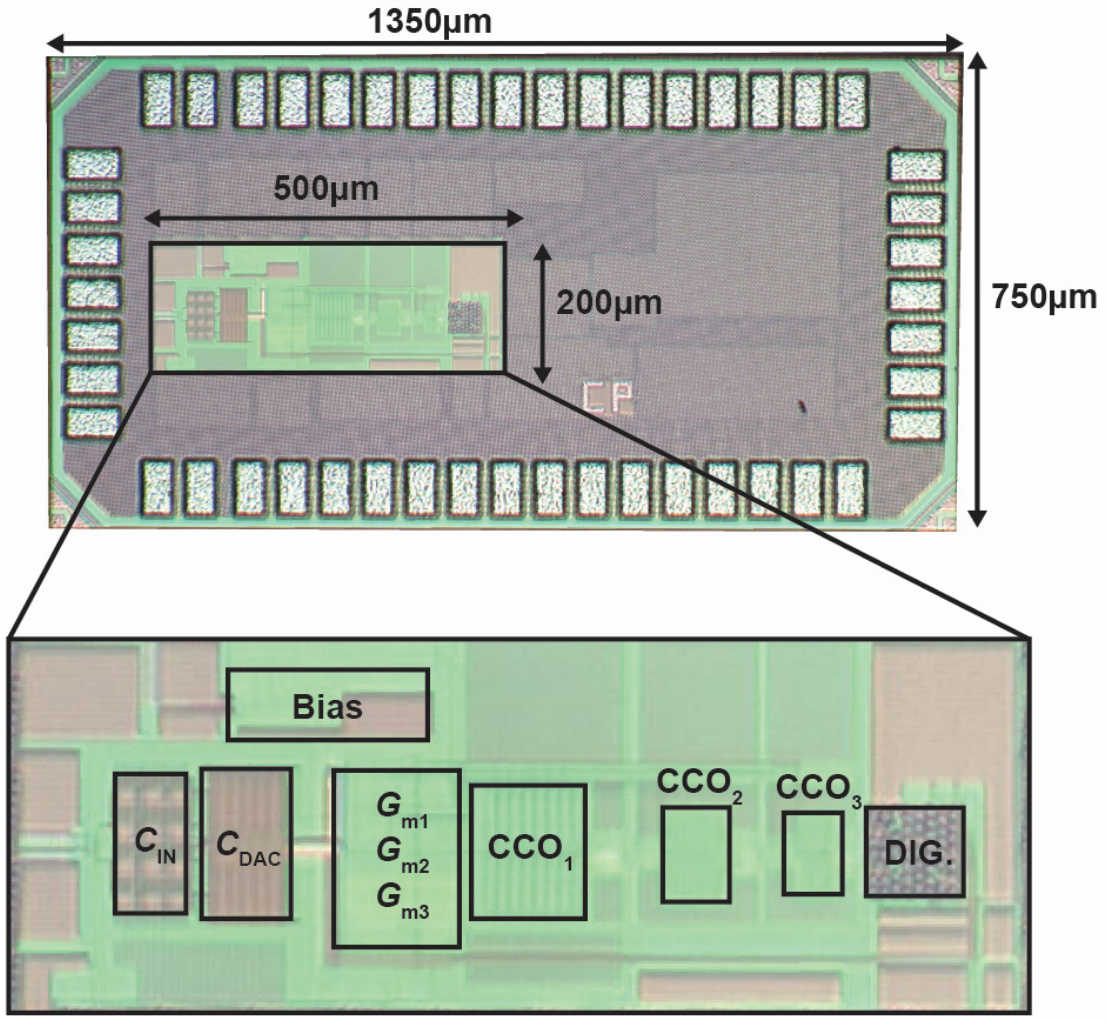


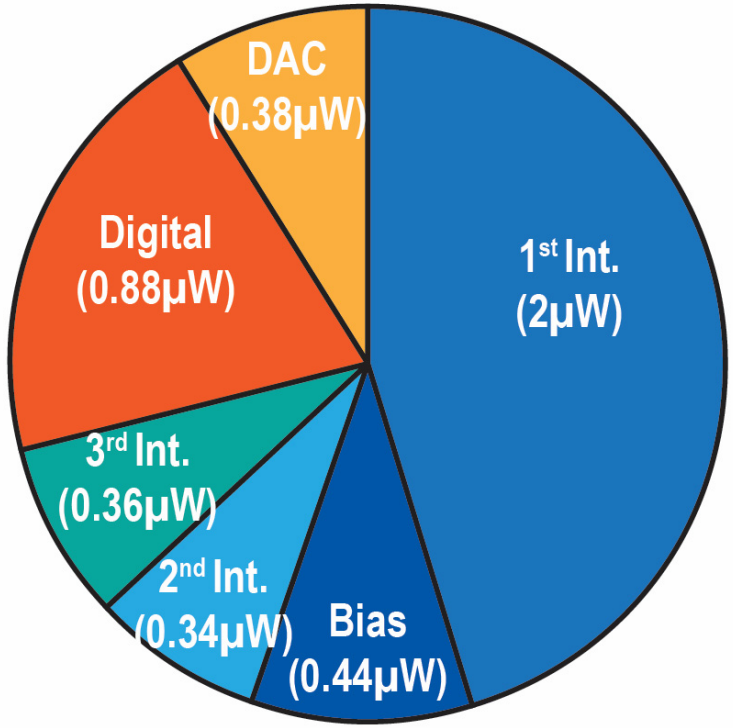


Outline

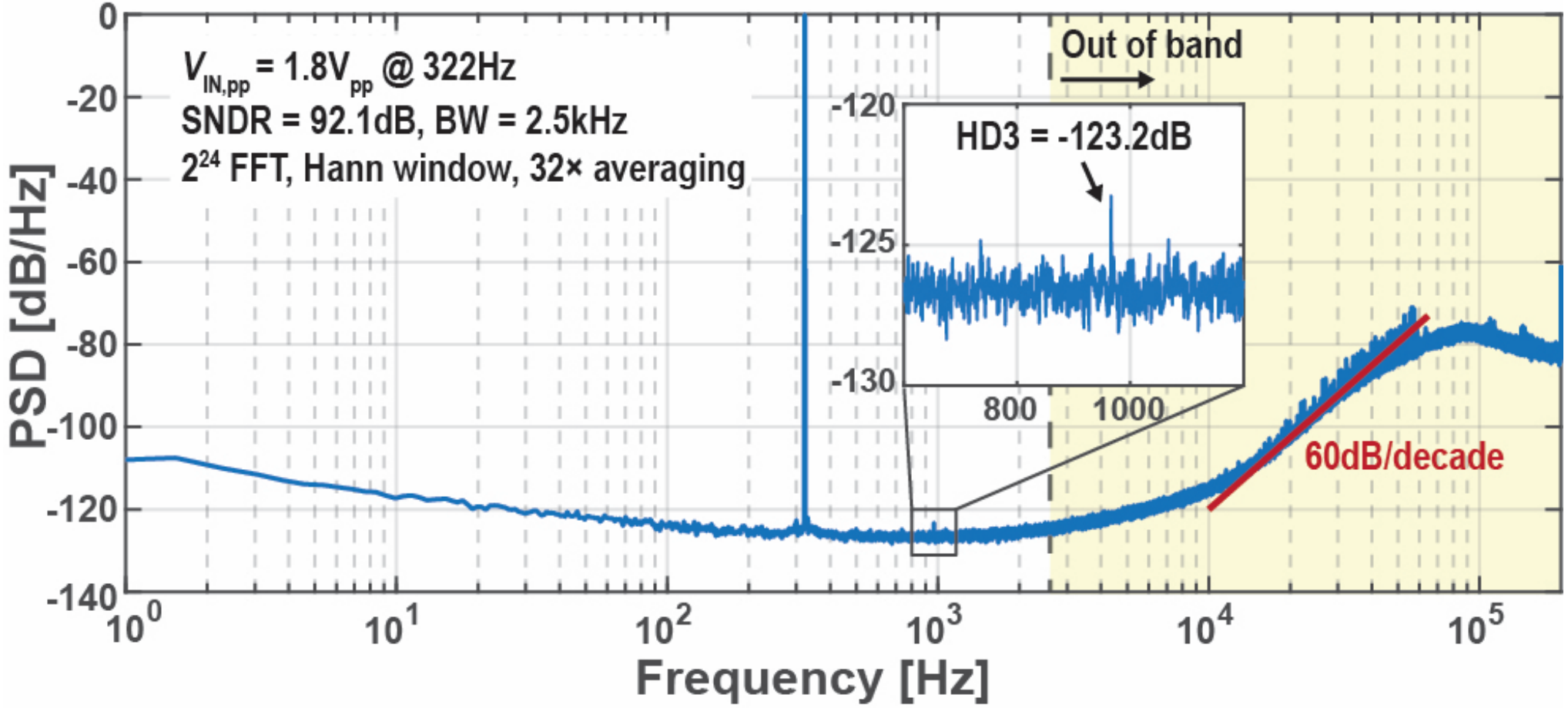
- Motivation
- Prior Work
- Pseudo Virtual Ground Feedforwarding Concept
- Proposed 3rd-order VCO-based ADC
- Circuit Implementation
- **Measurement Results**
- Conclusion

Chip Micrograph & Power Breakdown



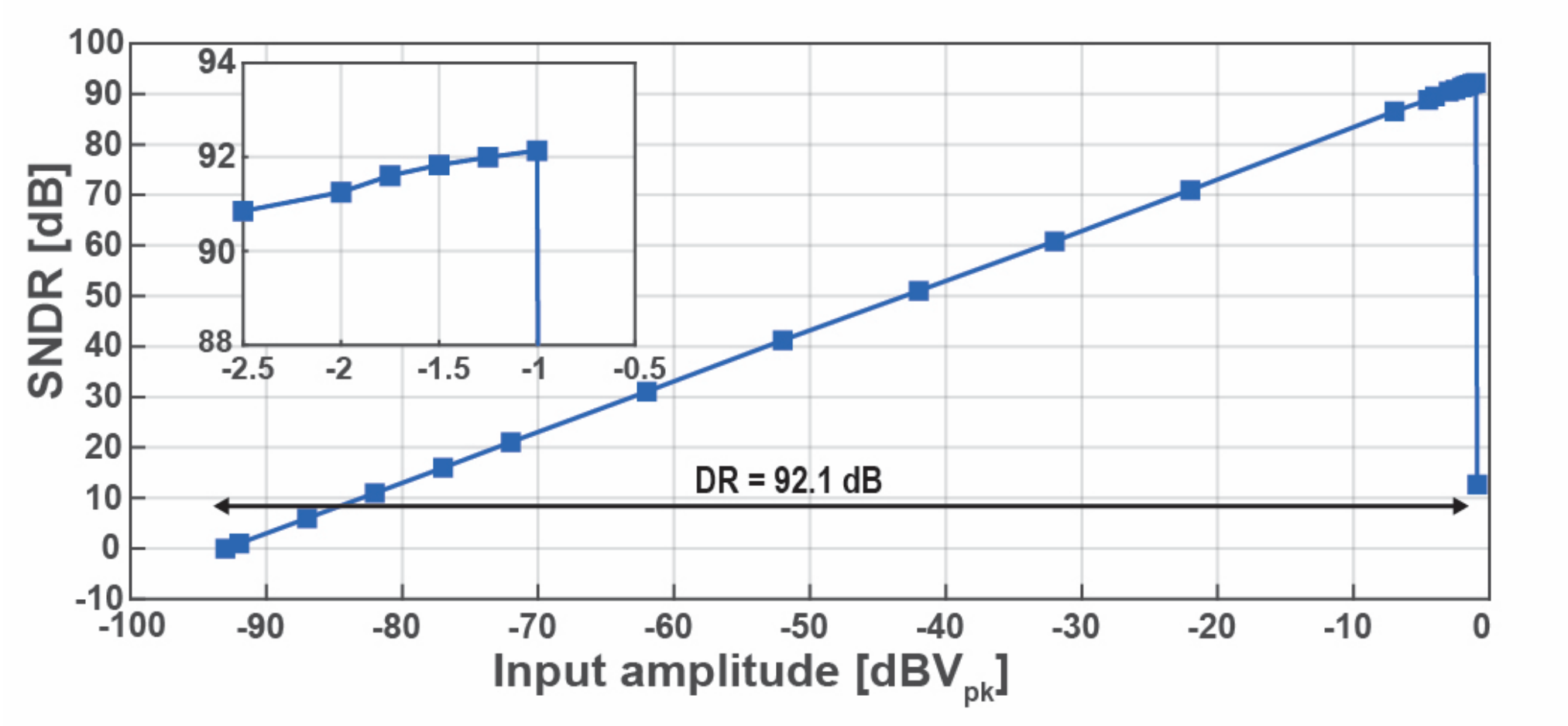


Measured Spectrum



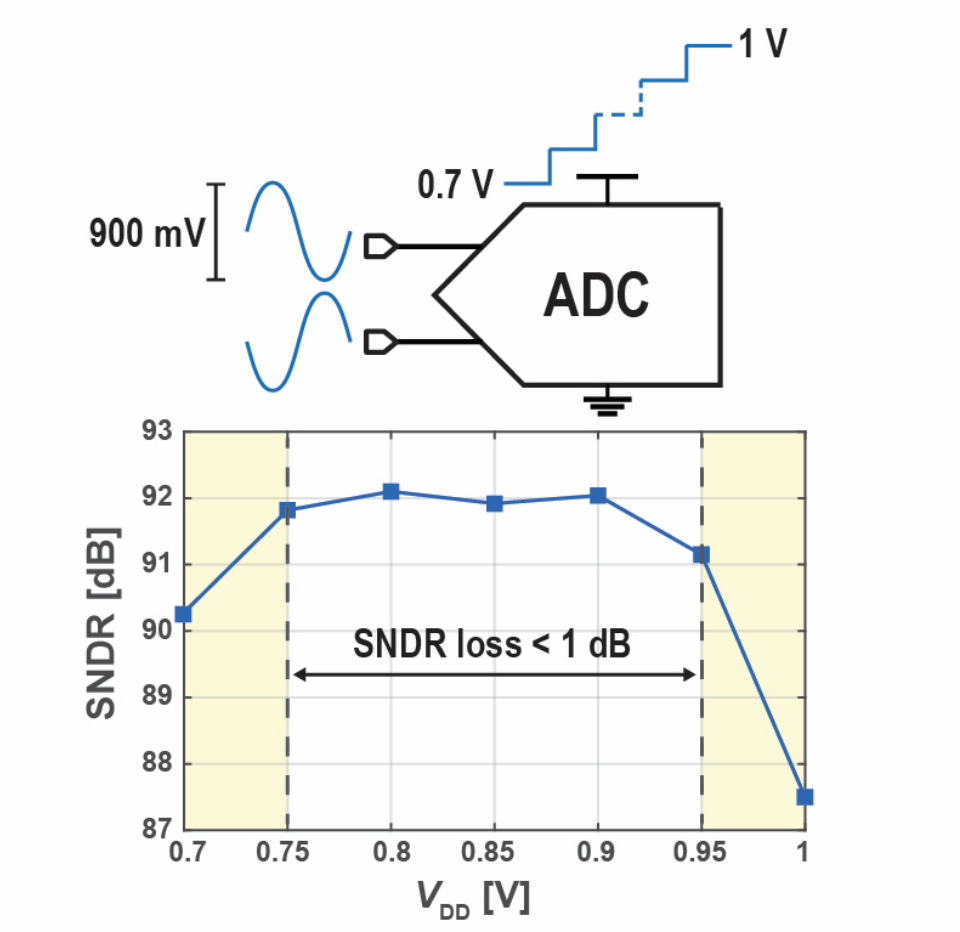
High SNDR (>90dB) and SFDR (>120dB)

Measured Dynamic Range



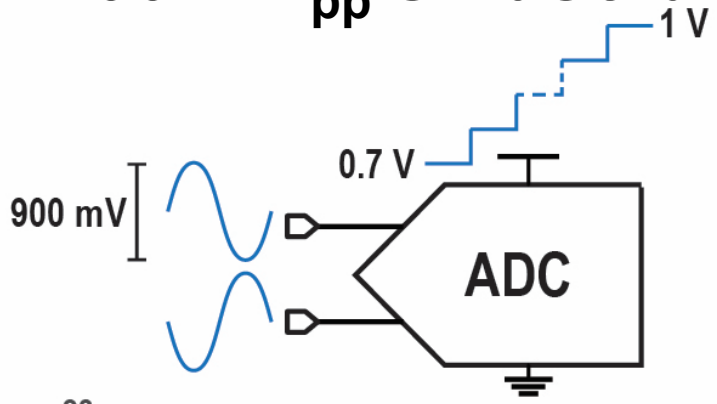
Supply sensitivity measurement

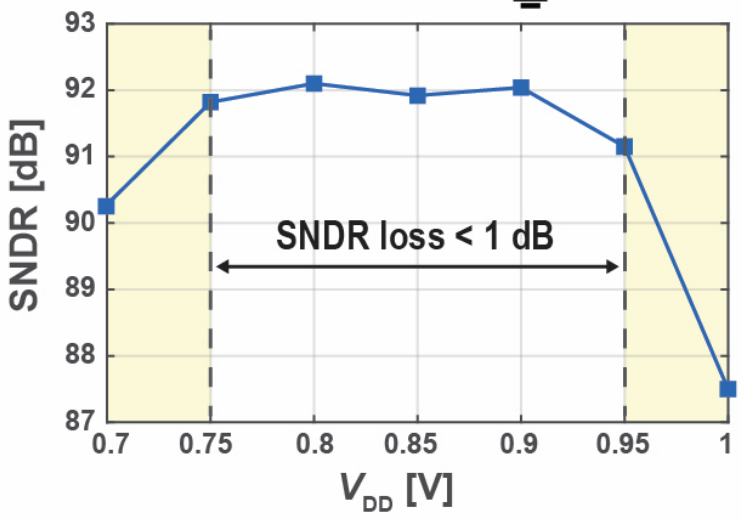
1. Supply voltage was varied from 0.7V to 1V

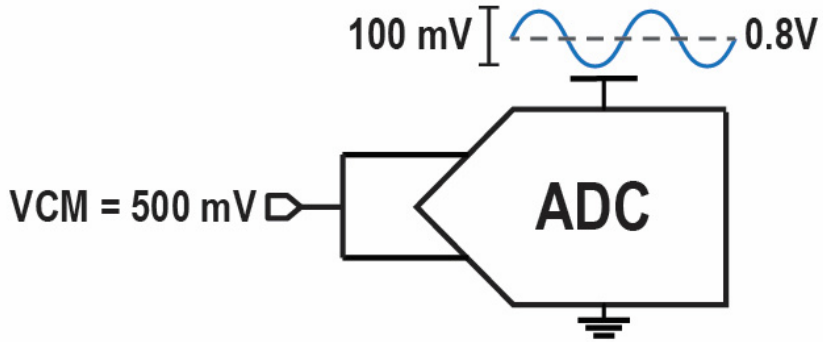


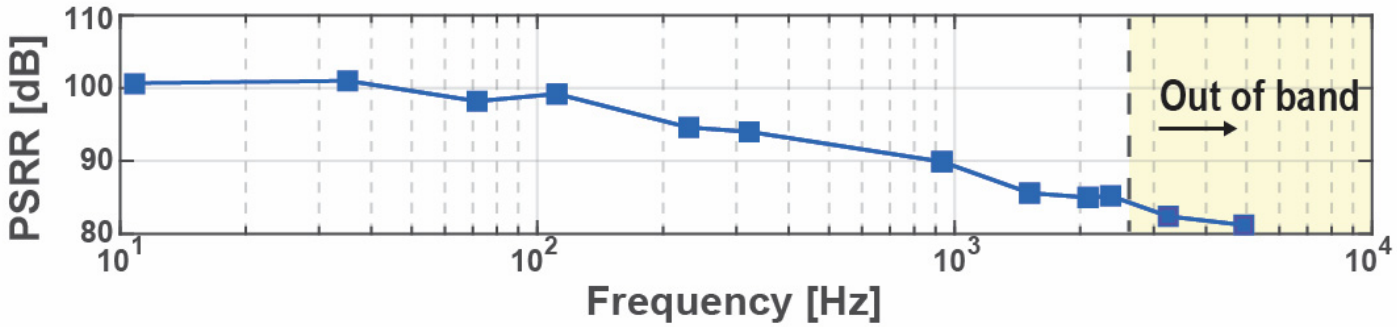
Supply sensitivity measurement

1. Supply voltage was varied from 0.7 V to 1 V
2. 100 mV_{pp} sinusoid on supply to test PSRR



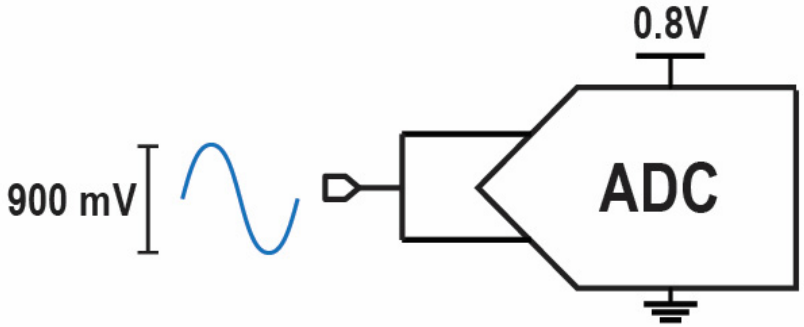


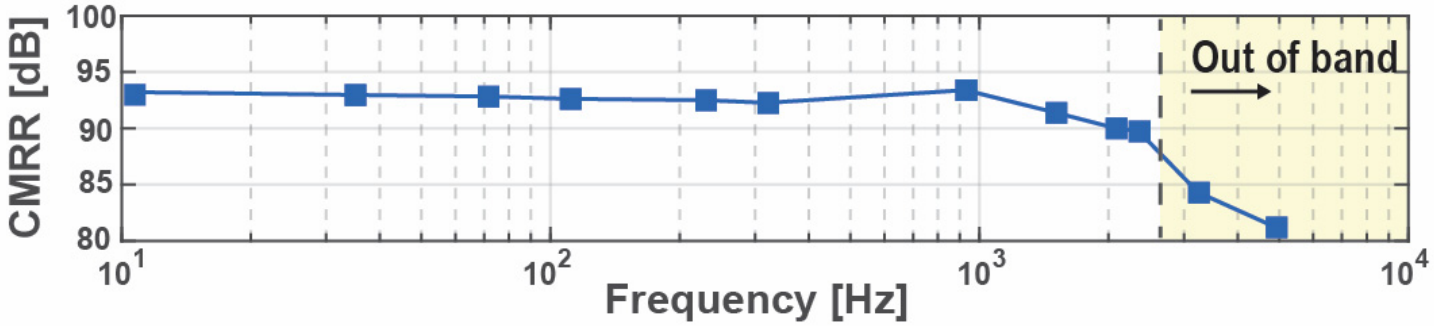




CMRR measurement

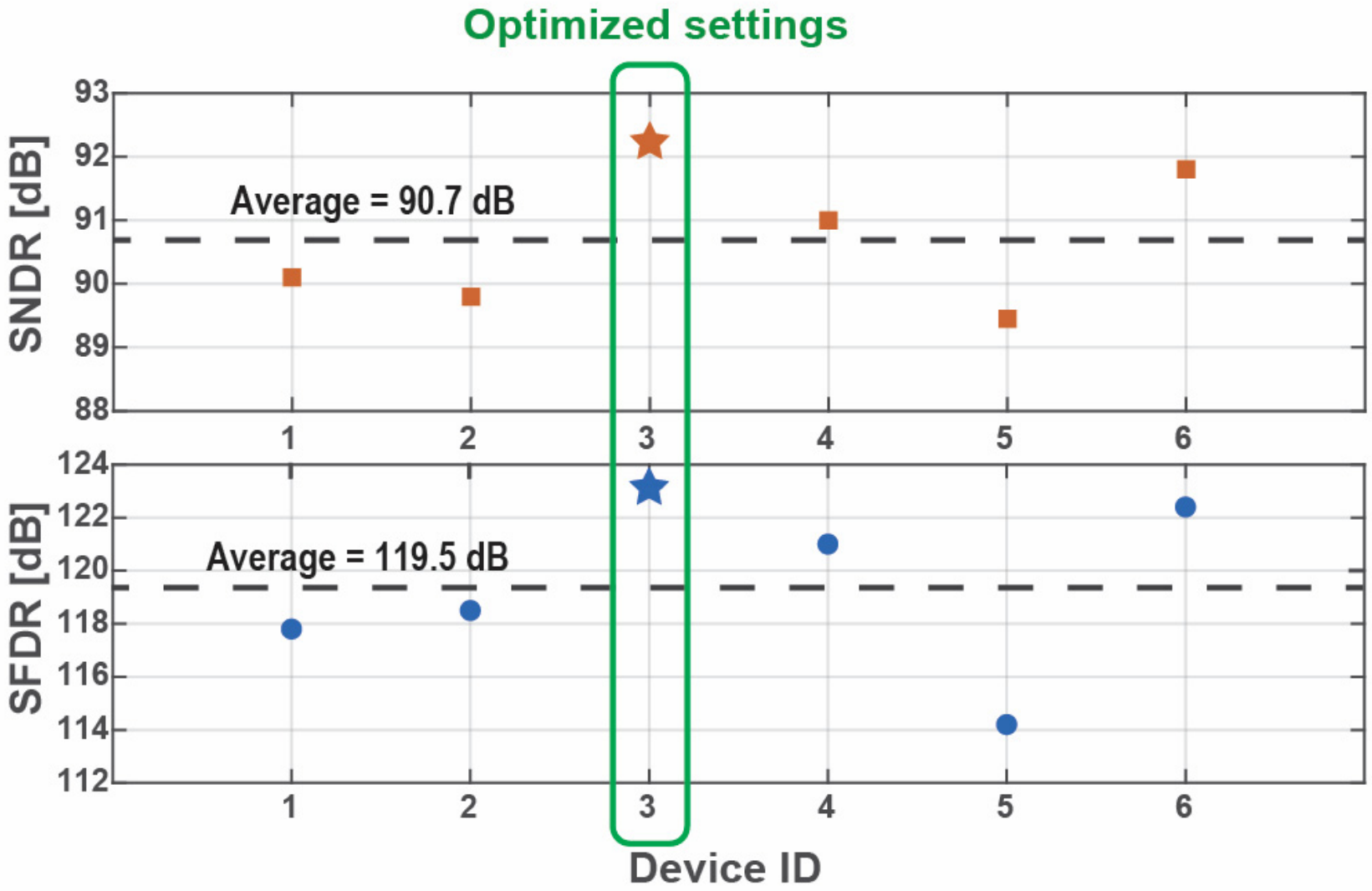
Full swing common-mode input was used to characterize the CMRR





CMRR > 87 dB in 2.5 kHz bandwidth

Performance Across Dies



Performance Summary

	H. Chandrakumar	S. Lee	C. Lee	S. Li	J. Huang	C. Pochet	**This work**
	ISSCC 2018	VLSI 2021	ISSCC 2020	CICC 2019	ISSCC 2021	ISSCC 2021	
Integration domain	Voltage	Voltage	Hybrid	Time	Time	Time	**Time**
Topology	3rd -ord.	3rd-ord.	2nd -ord.	1st -ord.	1st -ord.	2nd -ord.	**3rd -ord.**
Technology [nm]	65	28	65	40	65	65	**65**
Area [mm^2]	0.113	0.12	0.078	0.025	0.075	0.075	**0.1**
Supply (A/D) [V]	1.2	0.6	1	0.8/0.6	0.8	1.2/0.8	**0.8**
Power [µW]	4.5	33.6	6.5	4.5	1.68	5.8	**4.4**
DAC type	Capacitive	Resistive	Resistive	Capacitive	Capacitive	Capacitive	**Capacitive**
Input range [V_{pp}]	1.77	0.8	0.3	0.1	0.46	0.4	**1.8**
Sampling freq. [kHz]	400	12800	1280	2500	64	200	**400**
BW [kHz]	5	40	10	10	0.5	1	**2.5**
CMRR [dB]	N/A	55	76	83	97	89	**80-93**
SNDR [dB]	93.5	83	80.4	78.5	94.2	92.3	**92.1**
DR [dB]	96.5	86.5	80.4	79	95.1	92.3	**92.1**
SFDR [dB]	101.4	94.2	92.2	91	128	110.3	**123.2**
FoM_{SNDR}[dB]	184	173.8	172.3	172	178.9	174.7	**179.6**

$FoM_{SNDR}[dB] = SNDR + 10\log_{10}(BW/Power)$

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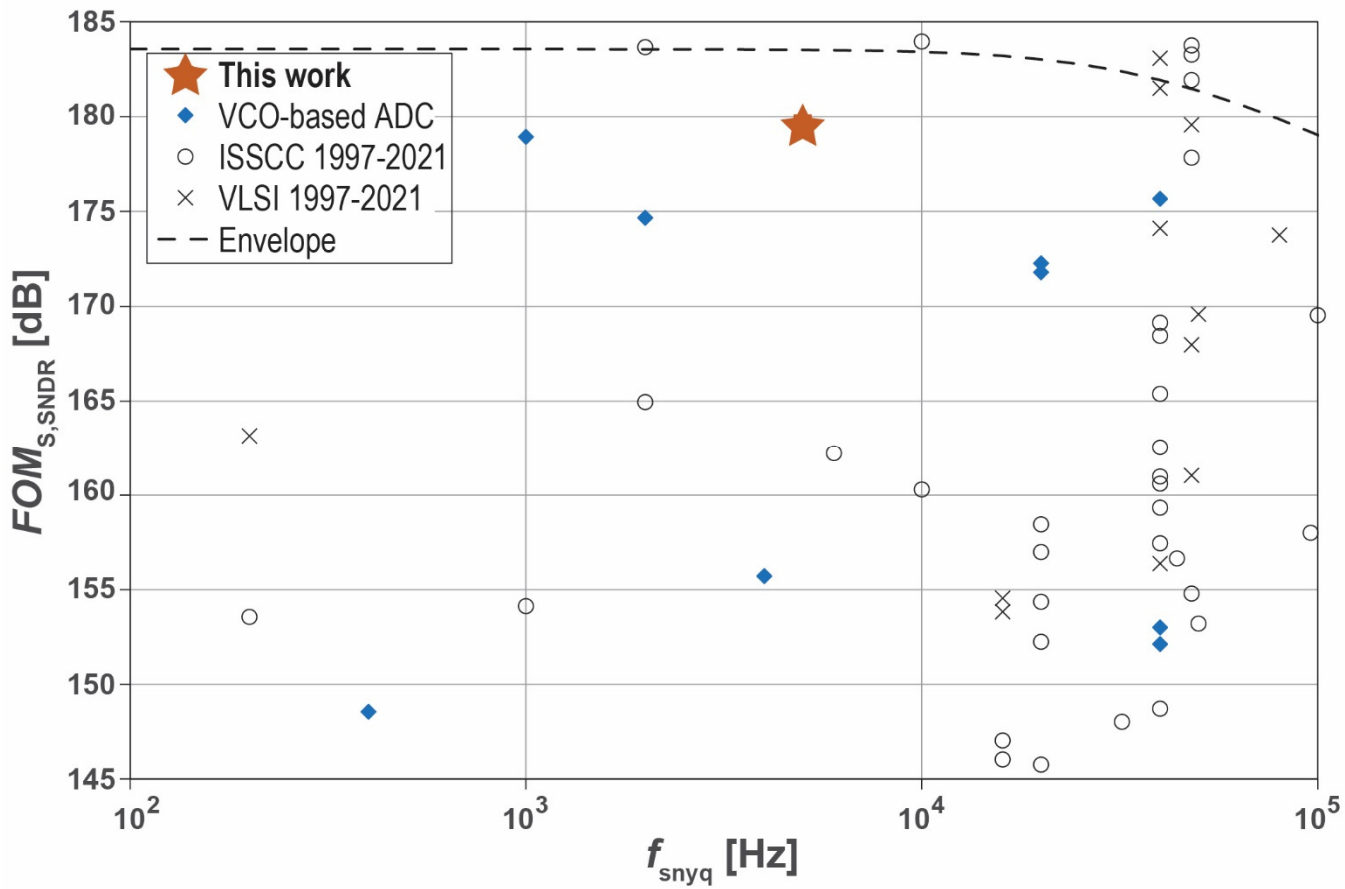
Comparison to the State-of-the-Art



[B. Murmann, "ADC Performance Survey 1997-2021"]

Highest FoM among VCO-based ADCs

Conclusion

Demonstrated a new technique enabling a higher-order VCO-based ADC with high linearity and dynamic range

Key innovations:

- **Pseudo virtual ground FF enabling 3rd-order NS and SFDR>120dB**
- **Digital friendly architecture using only VCO integrators**
- **Excellent CMRR and PSRR**
- **State-of-the-art Schreier FoM among VCO-based ADCs**

Acknowledgments

This work was supported by Synic and the Korea Electronics Technology Institute (KETI).

Thank You!