A 310 nW Temperature Sensor Achieving 9.8 mK Resolution Using a DFLL-Based Readout Circuit

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Abstract—This brief reports a high-performance, low-power temperature sensor suitable for wireless IoT devices/RFID tags. The system utilizes a mostly digital approach to achieve energy-efficient, sub- μ W operation with a resistor-based temperature sensor. A sampled, incomplete-settling, switched-capacitor-based Wheatstone bridge is read out using a digital frequency-locked loop (DFLL) while harnessing the quasi-periodic limit cycles to reduce in-band noise. Implemented in a 65 nm CMOS process, it consumes 310 nW and achieves 9.8 mK resolution in a 10 ms conversion time. This results in a 297 fJ·K² figure-of-merit (FoM) and low energy (3.1 nJ/meas.).

Index Terms—Resistance-to-digital converter (RDC), frequency-locked loop (FLL), digital, temperature sensors.

I. INTRODUCTION

R ECENT years have seen the growth of temperature sensing in IoT devices with applications such as monitoring environmental, health, and industrial machinery conditions [1]–[4]. This has steered research towards sub- μ W operation to support wireless/harvested power or extend the battery life for long-term continuous monitoring. While the emphasis on ultra-low-power design has demonstrated nW and pW power levels [2], the resolution has suffered (>35 mK). This is also reflected in their figure-of-merit (FoMs), which are nearly two orders of magnitude higher than the state-of-the-art [5].

MOS- or BJT-based temperature sensors are the usual choice for sub- μ W operation, achieving ~50 mK resolution [3]–[4]. The design in [2] achieves the best FoM among BJT/MOS-based sensors in the sub- μ W regime but is still less energy-efficient than resistor-based sensors and suffers from significant process variation. The recent trend in temperature sensors has moved towards resistor-based devices, which have high resolution and the best energy efficiency [6]. Polysilicon resistor-based temperature sensors are advantageous due to their low voltage coefficient, low 1/*f* noise, wide availability across process nodes, and low supply operation [1].

Fig. 1(a) shows readout circuits that incorporated resistive sensor(s) into a continuous-time delta-sigma modulator

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Fig. 1. (a) Conventional resistor-based temperature sensor readout circuits and (b) proposed DFLL scheme in a wireless IoT device.

(CTDSM) [5] or a frequency-locked loop (FLL) [1]. Most of these designs consume μ Ws in the front-end, and reducing that power is not straightforward as lowering the supply voltage confounds the design of analog circuits due to the limited headroom and lower signal-to-noise ratio (SNR). Another way to reduce power is to duty cycle a μ W-power temperature sensor [7]. However, the maximum current supported by IoT power harvesters can be limited by ambient-conditiondependent input power levels [8], poor conversion efficiency, or off-chip capacitors. Even rechargeable thin-film batteries have limited maximum current due to a large source resistance (~30 k Ω) [9]. Duty cycling also requires additional settling time for the sensor every time it turns on before a measurement can be taken and a wake-up timer, which adds power overhead.

This work reports a low-power temperature sensor by modifying the architecture proposed in [1] with a mostly digital readout circuit. The choice of an FLL was driven by its selfclocking nature and ease of integration with IoT systems, which often operate with wireless power and do not have an on-chip clock [10]–[11]. Fig. 1(b) illustrates the system architecture of a typical wireless-powered IoT sensor node where the sensor output is transmitted back to the receiver via backscatter by modulating the resonant frequency of

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Fig. 2. (a) Schematic of a single-ended SC-based WhB with (b) averaged output and (c) sampled output.

the wireless link. System power and complexity are highly reduced by using an FLL, as it removes the need for an onchip clock generator and an ADC. The post-processing of the output signal, which is done using a TDC and requires a clock, is shifted to the receiver, which has a more relaxed power budget. A digital FLL (DFLL) further replaces its analog counterpart's power and area-hungry blocks with digital equivalents. A similar DFLL-based architecture was recently utilized with a poly-phase filter for an ultra-low-power wakeup timer, emphasizing reducing the Allan Deviation and the line and temperature sensitivity [12]. Other prior works [13] use a semi-digital approach with analog blocks like a charge pump. This work presents a resistor-based temperature sensor consuming 310 nW with 9.8 mK resolution in a 10 ms conversion time using a DFLL. This results in an FoM of 297 $fJ \cdot K^2$ due to using a sampled incomplete-settling switched-capacitor (SC)-based WhB and harnessing quasiperiodic limit cycles. These enable an ultra-low-power DFLL while maintaining high resolution.

The rest of the brief is organized as follows: Section II describes and analyzes the proposed DFLL-based temperature sensor. Measurement results are presented in Section III and compared against prior work in Section IV.

II. DFLL-BASED TEMPERATURE SENSOR

A. Sampled Wheatstone Bridge

The core of the circuit is realized by an incomplete-settling, SC-based differential Wheatstone bridge (WhB) [1]. It consists of a silicided p-type polysilicon resistor, R, to sense the temperature, a metal-insulator-metal (MIM) capacitor, C, switched at a frequency f to match R, and a passive integrator, $C_{\rm f}$, to minimize the settling error. The fully-differential architecture increases the sensitivity, partially cancels switch imperfections, and removes the need for a reference circuit. Shown in Fig. 2(a) is a single-ended version of the WhB to illustrate the concept. In prior work, an active filter averaged the WhB output over one clock cycle to generate a voltage proportional to temperature [Fig. 2(b)]. The averaging operation required implementing the loop filter in the analog domain, which is area and power-hungry for noise and bandwidth reasons. We show through the following equations that sampling the endpoints of V_A is similar to averaging under certain design conditions and allows for a more power and areaefficient digital implementation [Fig. 2(c)]. The noise power of the WhB also remains the same since the bandwidth of the



Fig. 3. Proposed system architecture.

WhB (= $0.5/2\pi RC_f$) is kept more than two orders of magnitude lower than the sampling frequency ($f \approx 1/RC$). At the end of two clock cycles, the WhB output voltages, $V_{A,1}$ and $V_{A,2}$, are given by

$$V_{\rm A,1} = V_{\rm DD} + \left(V_{\rm A,2} - V_{\rm DD}\right) e^{\frac{-I_1}{RC_{\rm f}}}$$
(1)

$$V_{\rm A,2} = V_{\rm DD} + \left(\frac{C_{\rm f}}{C + C_{\rm f}}V_{A,1} - V_{\rm DD}\right)e^{\frac{-T_2}{R(C + C_{\rm f})}}$$
(2)

$$\approx V_{\rm DD} - \frac{V_{\rm DD}}{1 + \frac{T_1 + T_2}{RC}}, \text{ if } C_{\rm f} \gg C$$
(3)

where T_1 and T_2 are the clock phase periods. In [1], the output voltage was averaged over a clock cycle, which results in

$$\overline{V_A} \approx \frac{1}{1 + fRC} V_{\text{DD}}, \text{ if } C_{\text{f}} \gg C$$
 (4)

where $f = 1/(T_1 + T_2)$. Eq. (3) and (4) are approximately equal if $C_f \gg C$, but the former allows one to leverage process scaling and reduce power consumption with a digital readout circuit.

B. DFLL-Based Readout Circuit

A DFLL is built around the sensor to balance the WhB and read out the temperature through its output frequency, as shown in Fig. 3. The *R*-value (6.66 M Ω) was chosen to balance noise, area, and power consumption, with the latter being the primary concern in this work. It can be modified with a smaller *R* or a switched resistor in a more area-constrained design. A $C_{\rm f}/C$ ratio of 60 was selected to keep the WhB error due to incomplete-settling insignificant (<0.1 °C) [1] and reduce its susceptibility to parasitic capacitance and duty cycle error. $C_{\rm f}$ of 150 pF is implemented using MOS capacitor as the WhB is fairly insensitive to its variation. The bridge outputs are fed directly to a dynamic comparator followed by a digital filter and a digitally controlled oscillator (DCO). The DCO output is digitized by an off-chip, first-order noise-shaped time-to-digital converter (TDC), which is standard in timebased temperature sensors [1], [3]. The sampling frequency of the TDC, f_s , is chosen to keep the quantization noise of the TDC lower than the FLL output noise. The DCO generates an average output (f_{Temp}) of 20 kHz at room temperature. The choice of f_{Temp} is guided by the dynamic power consumption of the digital blocks, which is kept lower than the rest of the



Fig. 4. (a) Timing diagram; (b) Output PSDs with quasi-periodic limit cycles.

blocks. There is a direct tradeoff between the front-end capacitor area and f_{Temp} , hence the total power consumption. If the loop is closed by feeding a scaled version of the DCO output back to the SC-based WhB (*i.e.* $N \times f_{\text{Temp}}$), f_{Temp} is changed to 1/NRC to balance the WhB. This reduces the front-end capacitor area without running the whole system at $N \times f_{\text{Temp}}$, thus saving power. In this work, edge-combining multiple phases of the DCO realizes $3 \times f_{\text{Temp}}$.

The comparator and filter are clocked directly by complementary phases of f_{Temp} enabling the use of a low-speed, low-power comparator. The comparator is implemented with a dynamic preamplifier using a dynamic threshold (DTMOS) input pair to lower the input-referred noise [14]. Differential inputs and $C_{\rm f}$ mitigate the comparator kickback. The digital filter sets the loop's dominant pole near dc to ensure stability. It consists of proportional and integrator gain paths whose coefficients were derived using the bilinear transformation on its analog equivalent circuit ($\beta = -2\alpha \approx 0.001$). The sensor's worst-case start-up time depends on the filter coefficients and the sampling frequency and is \sim 80 ms. Implementing the comparator and filter digitally replaces the analog active loop filter, which is the most power and area hungry block in a conventional FLL. This results in $\sim 12 \times$ lower area and $\sim 95 \times$ lower power than the loop filter in [1]. Furthermore, having the filter implemented digitally allows for more complex algorithms and precise pole positioning. At room temperature, the output noise of the system is dominated by the comparator's thermal noise (~40%), followed by the WhB (~29%), DCO (~17%), and the quantization noise ($\sim 14\%$).

C. Time- and Frequency-Domain Waveforms

Unlike a conventional analog FLL, the DFLL locked state does not settle asymptotically to a constant value. With a 1b quantizer at the front of the readout circuit, f_{DCO} is described by periodic sequences or limit cycles [15] with an average value of f_{Temp} . This is shown in the transient waveforms [Fig. 4(a)], where f_{DCO} toggles between two adjacent states of the DCO when the system is locked. Fig. 4(b) plots the output behavior in the frequency domain. For convenience, further analysis is done on the TDC output as an alternative



Fig. 5. Simulated spur location across temperature.



Fig. 6. DCO schematic.

to the output of the FLL, but the two are directly related. For a dc input (as one would see with a temperature sensor), the output spectrum consists of f_{Temp} and multiple spurs, which are the limit cycle and its harmonics. The spurs' location and power are a function of the system bandwidth, stability, and DCO resolution. Importantly, these spurs can be pushed out-of-band beyond the decimation filter bandwidth, f_{Conv} , by design. With thermal noise, these spurs flatten out, gradually making the cycles quasi-periodic and finally completely random. This is similar to dither in a delta-sigma modulator. By limiting the noise, we ensure that the spurs are not entirely randomized, thus remaining highly localized, and only a small portion leaks into f_{Conv} . Fig. 5 shows the spur location across the entire temperature range simulated with a MATLAB model of the system. In all cases, the spur frequency is at least $9 \times$ higher than f_{Conv} and out-of-band. This model also allows one to explore the dependence on various design parameters (e.g., by changing $C_{\rm f}$ to modulate the phase margin of the system).

D. DCO Design

Fig. 6 shows the DCO implementation using a 3-stage differential current-controlled oscillator (CCO) biased with an on-chip constant- g_m and an 8b capacitive DAC (CDAC) at each stage's output. Every stage contains a differential latchbased delay cell to sharpen the edges, thus improving the DCO's 1/*f* noise. The DCO resolution (~50 Hz) was chosen to balance the noise and system complexity. The linearity requirement is relaxed (simulated with up to 5% DAC mismatch) as the DCO nominally toggles between two adjacent codes allowing capacitively-controlled frequency tuning. This is necessary as a small current step size in a current-tuned DAC places a ~4× more stringent noise specification on the bias network. The CDAC uses a 2.4 fF unit capacitor, and an additional 4b DAC was added to trim process variation.



Fig. 7. (a) Die micrograph; (b) Power distribution.



Fig. 8. Measured quantizer bitstream PSD.



Fig. 9. (a) Reference temperature transient response; (b) Measured location of spur across temperature.

III. MEASUREMENT RESULTS

This circuit was fabricated in 65 nm CMOS occupying 0.47 mm² and consumes 310 nW from a 0.9 V supply. As shown in Fig. 7, the digital readout circuit uses 49% and 22% of the total power and area, respectively. The off-chip TDC ($f_s = 2$ MHz) would consume 32.5 nW and 0.0005 mm² if implemented on-chip, making its impact on the total power and area negligible. Fig. 8 shows an FFT of the sensor's output bitstream achieving a temperature resolution of 9.8 mK with a conversion time of 10 ms. As expected, the spur from quasi-periodic limit cycles is outside f_{Conv} . The TDC noise is negligible in the bandwidth of interest and only dominates at higher frequencies. To verify that these spurs are always higher than f_{Conv} , a cooling curve experiment was performed [Fig. 9(a)] to plot their location across the entire temperature



Fig. 10. Measured transfer curves and inaccuracy after 2-point calibration and nonlinearity correction.

range [Fig. 9(b)]. The spur location was calculated from the PSDs derived from the output bitstream once every minute. The measured data is in close agreement with the MATLAB simulation, where the measured average is only $1.08 \times$ the simulated average, and all the spurs are at least $8 \times f_{\text{Conv}}$. Computing the Allan Deviation shows that the output period jitter is dominated by thermal noise until ~300 ms, after which the design is limited by 1/f noise and environmental drift with a noise floor of ~5 ppm at 1 s.

Fig. 10(a) shows data (n = 14) collected in a temperaturecontrolled chamber. A Pt-100 sensor was placed near the chip to provide an accurate reference point, and a large aluminum block in the chamber was used as a thermal filter. The output frequency varies from 17.5 to 22 kHz over the -5 to 95 °C temperature range. Process variation in the CDAC resulted in a slightly narrower temperature range than simulation. The calibration curve has an average temperature coefficient (TC) of 2,325 ppm/K and a 2.65% spread on the nominal period. To remove gain and offset error, the devices were 2-point trimmed. Silicided polysilicon resistors in 65 nm have significantly higher nonlinear coefficients (e.g., $\sim 10 \times$ higher second-order coefficient) than older technology nodes like 180 nm that are digitally corrected [13]. Without it, the sensor's peak-to-peak inaccuracy is ~ 6 °C. Hence, the trimmed data were corrected for this technology-dependent systematic non-linearity using a measured 3rd-order polynomial. This results in 3σ error of +1.8/-1.6 °C [Fig. 10(b)]. The chip has a measured line sensitivity of 0.65 %/V or ~2.8 °C/V from 0.85 to 1 V at 25 °C.

IV. DISCUSSION

Table I compares this work with prior low-power temperature sensors. This work achieves a 297 fJ·K² FoM, which is more than $2\times$ better than always-on sub- μ W temperature sensors and only higher than [7], a heavily duty cycled, high-power sensor with limited range. Fig. 11 plots this work on the recently published temperature sensors landscape to show its improved energy efficiency for low-power sensors. To summarize, this work combines the energy efficiency of

TABLE I Performance Summary and Comparison of Sub- μ W Temperature Sensors

Parameter	[18]	[19]	[4]	[3]	[17]	[7]	[2]	[20]	[16]	This Work	
Tech (nm)	180	160	180	180	65	180	65	180	65	65	
Sensor Type	MOS	DTMOS	MOS	BJT	Res	Res	MOS	BJT+MOS	Res	Res	
Active Area (mm ²)	0.09	0.085	0.0087	0.1	0.11	0.12	0.013	0.12 ^b	0.0017	0.47	
Self-clocked	Yes	No	Yes**	Yes**	No	No	Yes	No	No	Yes**	
Supply (V)	1.2	0.85-1.2	1.2	1.6-2	0.65, 1	1.6	0.9-1.2	1	0.6, 1	0.9	
Temperature Range (°C)	0 - 100	-40 - 125	-20 - 100	-30 - 120	0 - 100	27.5 - 47.5	-20 - 100	-10 - 100	-20 - 120	-5 - 95	
Inaccuracy (°C)	-1.4/1.5°	±0.4	±0.2	±0.85	-1.1/1.5°	-0.1/0.2	-2.7/1.8°	±2.35°	$\pm 0.8^{\circ}$	-1.6/1.8	
[Trim Pts]	[2]	[1]	[2]	[1]	[1]	[1]	[2]	[1]	[2]	[2]	
Line Sensitivity (°C/V)	-3.15/2.5	0.45	1.2	0.7	-	0.004	-	1.07	2.6	2.8	
Conversion Time (ms)	30	6	8	8.1	0.01	8	34.3	200	0.02	10	
Resolution (mK)	0.3	63	73	39	610	1.1	250	590	530	9.8	
Power (nW)	71	600	75	970	500	700 ^d	0.64	0.49	108	310	
FOM ^a (fJ·K ²)	190000	14100	3200	10600^{*}	1820	64 ^d	1400	34100	610	297*	
^a Energy/conversion \times (Resolution) ²		^b Requires a	n external 20	nF capacitor	* Exclue	* Excluding TDC power ** Excluding post-processing TDC clock					

° Min-max, 3 sigma for the rest

Excluding TDC power Excluding post-processing TDC clock

10 10 107 10⁰ 10 Energy/Conversion (nJ) 105 **10⁻¹⁰** 10 10 4 pJ K 10 10 10-400 fJ K² 10 MEMS 10-Better FoM 10⁰ 10⁻⁵ 10 10 10-Resolution (K) Power (µW)

Fig. 11. Performance comparison against the state-of-the-art. (a) FoM landscape; (b) FoM vs. Power for sub- μ W temperature sensors.

resistor-based temperature transducers with the advantages of digital circuits to achieve a high-performance, low-power temperature sensor suitable for wireless IoT applications. Although the proposed temperature sensor has a comparatively large area, it is a promising work that can be extended to low-cost, higher volume applications by reducing transducer area through techniques such as a switched resistor (also helps with power), with additional considerations of noise-folding and leakage.

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^d Duty cycled