# A 30.3 fA/√Hz Biosensing Current Front-End With 139 dB Cross-Scale Dynamic Range

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***Abstract*—This paper presents an 8-channel array of low-noise (30.3 fA/√Hz) current sensing front-ends with on-chip microelectrode electrochemical sensors. The analog front-end (AFE) consists of a 1st-order continuous-time delta-sigma (CT ΔΣ) modulator that achieves 123 fA sensitivity over a 10 Hz bandwidth and 139 dB cross-scale dynamic range with a 2-bit programmable current reference. A digital predictor and tri-level pulse width modulated (PWM) current-steering DAC realize the equivalent performance of a multi-bit ΔΣ in an area- and power-efficient manner. The AFE consumes 50.3 μW and 0.11 mm² per readout channel. The proposed platform was used to observe protein-ligand interactions in real-time using transient induced molecular electronic spectroscopy (TIMES), a label- and immobilization-free biosensing technique.**

***Index Terms*—Biosensor, current front-end, CT ΔΣ, IIR quantizer, sub-pA, tri-level DAC.**

## I. Introduction

With the rapid advances in exploration and screening techniques, the pharmaceutical industry identifies almost ten thousand new drug compounds annually [1]–[3]. However, the success rate from drug discovery to a clinical trial is a meager 0.05% due to the involvement of extraordinarily high-cost and time-consuming multi-phase human trials [4]. Many of these failures could have been predicted and avoided in the pre-clinical stage if scientists had tools to allow them better understand and screen drug-drug interactions. There is currently an unmet need for *in-vitro* testing of protein-ligand interactions to assess the binding properties qualitatively and quantitatively analyze the binding kinetics in physiological conditions [5]–[7].

Proteins have complex interactions with other biomolecules (*i.e.*, ligands). There has been significant effort in developing quantitative molecular-level tests for protein screening, but the performance is heavily dependent on how the molecules are prepared. For example, surface plasmon resonance (SPR) [8]–[10] and Forster resonance energy transfer (FRET) [11]–[13] require immobilization and/or labeling of the ligand, which can interfere with binding. As such, existing methods introduce disruptions (sometimes significant) in the binding kinetics and lead to results that do not resemble those *in vivo*.

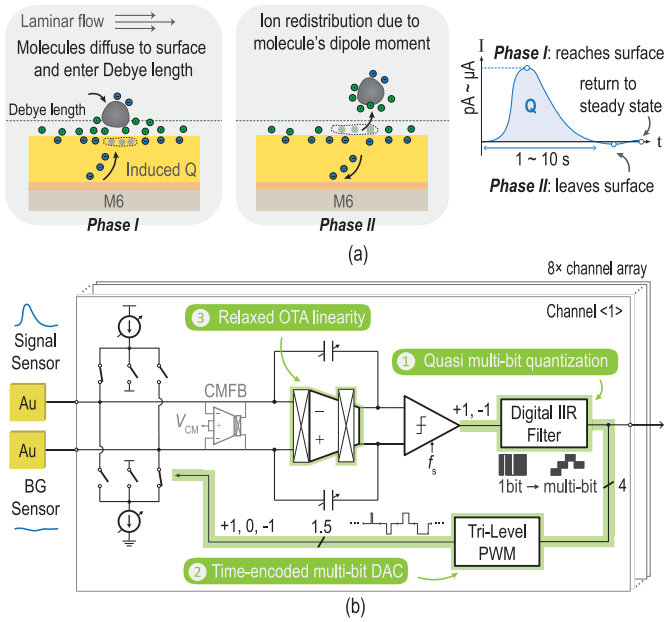


Fig. 1. (a) TIMES sensing principle and signal model; (b) system architecture of the proposed AFE.

Transient induced molecular electronic spectroscopy (TIMES) is a recently reported biosensing technique for characterizing protein-ligand interactions without imposing any physical alteration to the biomolecules such as labeling or immobilization [14]–[16]. In TIMES, the transient signal is generated as the surface charge distribution on the electrodes is reoriented by the dipole moment of a protein-ligand complex passing by under laminar flow, as shown in Fig. 1(a). As a result, TIMES is closer to physiological conditions and reveals molecular properties unattainable with existing methods. It is important to note that this is not a general-purpose biosensing technique as it intrinsically lacks specificity. TIMES's detection principle and validity have been studied using discrete sensors and an off-the-shelf transimpedance amplifier instrument (SRS 570). This work presents a monolithic integration of the sensors and a multi-channel current front-end, achieving a miniaturized sensing platform—μTIMES, as shown in Fig. 1(b).

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TABLE I
TARGET SPECIFICATIONS OF THE CURRENT SENSING AFE

| | Application Requirement | AFE Target |
|---|---|---|
| **Sensitivity*** | 0.1 μM detection limit | 100 fA |
| **Dynamic Range** | 0.1 μM – 10 mM | 100 fA – 1 μA |
| **Bandwidth** | 5 cm/s laminar flow rate | 10 Hz |
| **Active Area** | 8 on-chip electrodes | 0.1 $mm^2$/ch |

*Lysozyme protein on a $300\times300$ $\mu m^2$ sensor.

Integrating a sensor with the readout circuit eliminates parasitics due to long cables from the sensor to the front-end, exhibits better environmental interference resilience, and generally leads to lower noise, higher fidelity measurements. Table I lists the design specifications for μTIMES based on prior benchtop studies. To implement eight parallel channels on a $3\times3$ $mm^2$ CMOS chip, a $3\times5$ sensor array (8 channels with shared references and test structures) was designed, each with a maximum sensor area of 300 μm × 300 μm, which limits the active circuit area and scales the signal range down to 100 fA – 1 μA for the target protein concentration range of 0.1 μM – 10 mM. The 140 dB dynamic range (DR) was portioned across 4 on-chip references in this work, relaxing the DR for each reference to 80 dB. The laminar flow rate (5 cm/s) is the determinant factor in the bandwidth, but the physical dimension of the channel is also relevant as smaller molecules like ligands theoretically move faster. Therefore, the transient response of ligands was used to determine the 10 Hz upper bound on the signal bandwidth. In contrast, chemical parameters such as the molecule's surface charge affect signal magnitude more than bandwidth.

In electrochemical techniques such as cyclic voltammetry or chronoamperometry, where sensing electrodes need to be electrically modulated, intermediate stages such as transimpedance amplifiers [17], [18] or current conveyors [19], [20] are commonly used to decouple the readout front-ends from the large voltage variation. However, during a TIMES study, both working and reference electrodes (WE and RE) are biased at a dc potential and thus can be interfaced with a current-input analog-to-digital converter (I-ADC) for direct quantization. While there are many I-ADCs, such as voltage-controlled oscillators (VCOs) [21] and current-to-frequency (*I*-to-*F*) converters [22], delta-sigma modulator ($\Delta\Sigma$)-based ADCs are by far the most embraced due to their excellent resolution-to-energy tradeoff for low bandwidth signals [23]–[30]. However, few works can achieve the 100-fA resolution target with such a wide cross-scale DR.

In [24], a pulse width modulated (PWM) switch was added at the input of a 1st-order incremental $\Delta\Sigma$. This scales down the input signal and lets the $\Delta\Sigma$ operate with a lower reference current for better energy efficiency. A large DR was achieved by partitioning the signal range across five references from 50 pA to 500 nA. However, the input modulation makes this architecture sensitive to noise folding and aliasing since a discrete-time (DT) $\Delta\Sigma$ does not have inherent anti-aliasing. Furthermore, charge injection from the input switch can perturb the sensor, such as with the capacitive sensor in μTIMES. In [27], asynchronous input flipping was proposed in an hourglass-$\Delta\Sigma$ to avoid saturating the integrator, resulting in a state-of-the-art DR of 160 dB while using a single reference. However, this work requires two continuous-time comparators, a 5th-order polynomial calibration loop, and dynamic element matching (DEM) – making it both area- and power-hungry and thus less attractive for multi-channel applications.

Fig. 1(b) shows the proposed architecture for each readout channel, where a 1st-order continuous-time current-mode $\Delta\Sigma$ modulator was implemented for its compact area and good energy efficiency. To increase resolution while consuming low area and power, we propose to add a digital infinite impulse response (IIR) filter after the single-bit quantizer in a $\Delta\Sigma$ to achieve multi-bit quantization. The added IIR filter effectively achieves a 4-bit feedback system by predicting the next output from previous 1-bit quantizer outputs. This improves the modulator resolution with finer feedback levels. The output is then fed back using a tri-level (return-to-open) PWM current-steering DAC (I-DAC). The proposed architecture is equivalent to a multi-bit modulator that can be clocked at a lower sampling rate than a single-bit modulator for the same resolution, thus relaxing the bandwidth requirement and improving the anti-aliasing. A cross-scale dynamic range of 140 dB was achieved by partitioning the reference current. This work expands on the work originally reported in [30].

The rest of this paper is organized as follows. Section II describes the TIMES sensing principle. The system architecture and the proposed IIR quantizer are discussed in Section III. Section IV describes the circuit implementation, and Section V presents both electrical and *in-vitro* measurement results. Finally, conclusions are drawn in Section V.

## II. SENSING PRINCIPLE

In this label- and immobilization-free detection scheme, an electronic signal is generated through a non-faradic process when a molecule or complex (*i.e.*, a protein-ligand) diffuses towards the electrode. The protein, ligand, and buffer are introduced in two separate microfluidic channels to create a flux of molecules towards the electrode, with the buffer-only channel serving as a reference. Background currents and interferences (*e.g.*, 60 Hz, temperature drift, etc.) common to both channels are canceled by differential sensing. In the protein-ligand channel, the protein is the *only* macromolecule that possesses a dipole moment. The formation of a protein-ligand complex alters the 3D configuration, changing the dipole moment and charge distribution [31]. Fig. 1(a) illustrates this process where ions on the sensor surface redistribute by the protein-ligand dipole moment to maintain local charge neutrality, introducing a charge flux due to the image charge effect. The transient change in the surface charge results in a current signal that the AFE records. In contrast to FET-based sensing, where the source-drain current is modulated by the change in surface change when immobilized probes capture or release the targets, TIMES is a label-free and immobilization-free measurement so different kinds of biomolecules can be measured with the same device.

The reference electrode (RE) used in TIMES is a pseudo-reference electrode biased at mid-scale, 0.9 V. Due to the TIMES

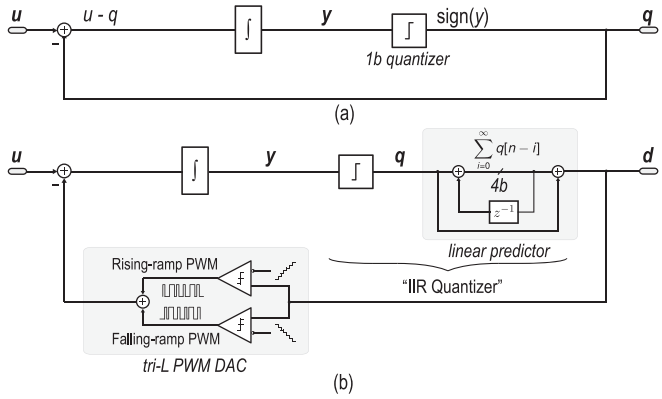


Fig. 2. Block diagram of (a) conventional 1st-order 1-bit $\Delta\Sigma$ and (b) the proposed $\Delta\Sigma$ modulator with IIR quantizer and tri-level PWM DAC.

sensing principle, where the charge perturbation on the electrodes is measured, the potential between the solution and the electrodes does not need to be as well defined as in many other electrochemical sensing approaches. Therefore, there is no need for a dedicated potentiostat to drive the RE. This sensing technique can be generalized to all types of molecular interactions, including protein-ligand, protein-protein, and protein-nucleic acid interactions. By measuring the transient signals induced by the ligand, protein, and mixtures of ligand and protein molecules in different ratios, one can calculate the dissociation coefficient, $K_{\mathrm{d}}$, of the protein-ligand interaction. As in Table I, the dynamic range for $K_{\mathrm{d}}$ measurements can vary between mM (weak/nearly no binding) to nM (strong binding). Furthermore, this technique can also be used to capture a "*molecular fingerprint*" of the target biomolecule's (or complex) interaction with the sensor surface.

## III. System Architecture

The transient signal induced by the protein-ligand complex in μTIMES is intrinsically band-limited to only a few hertz. Oversampled data converters are well-suited for capturing such signals. Specifically, a 1st-order $\Delta\Sigma$ modulator with a moderate to a high oversampling ratio (OSR) can provide sufficient signal-to-noise ratio (SNR) to meet the 13-bit resolution target while being area- and power-efficient; two factors that are important in multi-channel/arrayed applications.

Historically, single-bit quantization in $\Delta\Sigma$, as shown in Fig. 2(a), has been widely adopted because of its ease of implementation and inherent linearity, avoiding the need for DEM [23]–[25]. However, several nonideal aspects of single-bit quantization can significantly degrade the performance. First and foremost, for a 1st-order loop filter, doubling the sampling frequency, $f_{\mathrm{s}}$, only improves the signal-to-quantization noise ratio (SQNR) by 9 dB (1.5 bits); thus, one must resort to a high OSR causing higher power consumption. Another problem is that the quantization noise is strongly deterministic, resulting in in-band harmonic distortion and limit cycles. Consequently, 1st-order single-bit $\Delta\Sigma$ modulators are challenging to model and analyze with a linear model, highlighting the third issue—arbitrary quantizer gain. Since a single-bit quantizer only has two levels, its gain can take a wide range of values, potentially shifting the poles and altering the loop dynamics. As a result, designing a 1st-order, single-bit $\Delta\Sigma$ usually relies on exhaustive simulation [32].

This work proposes a 4-bit IIR quantizer to avoid the aforementioned issues with single-bit quantization. As shown in Fig. 2(b), the IIR quantizer consists of a single-bit quantizer (*i.e.*, a comparator) and a 4-bit digital IIR filter that increases the effective quantization resolution by linearly predicting its quantization level based on two previous comparator decisions, $q$. The proposed IIR quantizer balances the tradeoff between low implementation complexity and higher resolution from using a multi-bit quantizer. Finally, a tri-level PWM DAC encodes the 4-bit output, $d$, into a symmetrical pulse sequence whose width is proportional to the digital code and is subtracted from the input, $u$, to close the feedback loop.

### A. Linear Prediction in a 1st-order Single-bit $\Delta\Sigma$

Unlike a Nyquist-rate ADC (*e.g.*, flash, SAR, etc.) where the result is instantaneously available, a $\Delta\Sigma$ modulator outputs a time-encoded sequence, of which each sample is dependent on the previous values. This "memory" effect and oversampling form the fundamental basis for using linear prediction to increase the quantizer resolution. For a reasonably large OSR, any input signal can be estimated by linearly extrapolating from its previous samples [33]. For example, with a slow-varying discrete-time sequence $x$, $x[\mathrm{n}+1]$ can be approximated by taking the first two terms in the Taylor expansion around $x[\mathrm{n}]$. It can then be shown that each sample in $x$ is a linear combination of its previous two samples, *i.e.*,

$$x\left[\mathrm{n}+1\right] \approx x\left[\mathrm{n}\right] + \frac{\partial x}{\partial t}T \;=\; 2x\left[\mathrm{n}\right] - x\left[\mathrm{n}-1\right], \qquad (1)$$

where $T$ is the sampling period.

Before applying the concept of linear prediction to a single-bit $\Delta\Sigma$, we first look at how each output relates to the instantaneous input magnitude. Starting with a standard single-bit CT $\Delta\Sigma$, the comparator output is directly subtracted from the input. The quantizer input, $y$, is equal to the previous sample plus the instantaneous residue between the input and feedback, as shown in Fig. 2(a), where

$$y\left[\mathrm{n}\right] = \; y\left[\mathrm{n}-1\right] + u\left[\mathrm{n}\right] - q\left[\mathrm{n}\right]. \qquad (2)$$

On average, $q$ is fed back such that the residue seen by the integrator, $u - q$, is minimized, so it is reasonable to expect a statistical relationship between $u$ and $q$. For example, for a $u$ close to the positive full-scale range, the local density of $+1$'s in $q$ is also large because the modulator tries to feedback a large *mean* value.

### B. IIR Quantizer

To realize (1) with only single-bit quantization, Fig. 2(b) shows the comparator output is passed through a filter whose transfer function can be derived from the difference equation

$$d\left[\mathrm{n}\right] = \; d\left[\mathrm{n}-1\right] + 2q\left[\mathrm{n}\right] - q\left[\mathrm{n}-1\right]. \qquad (3)$$

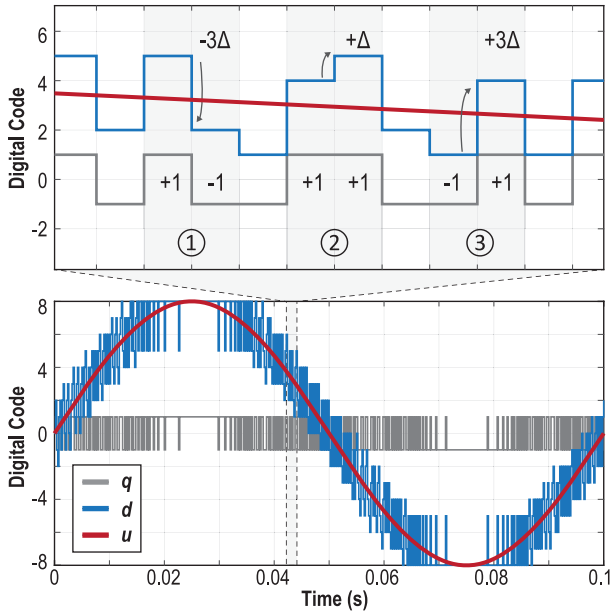


Fig. 3. Transient waveforms of the linear prediction in a IIR-ΔΣ with input, $u$, comparator output, $q$, and modulator output bitstream, $d$.

The addition of $d[\mathrm{n}-1]$ compared to (1) is because $q$ only contains the polarity of $y[\mathrm{n}-1]$. Here the state variable, $d[\mathrm{n}]$, is a multi-bit quantity that stores the cumulative sum of the 1-bit comparator decision, $q[\mathrm{n}]$. Since the output code of a ΔΣ is a time-encoded sequence where each sample is decoded from all prior samples, a state variable is needed to capture such "memory" effect of ΔΣ modulation. The $z$-transform of (3) is

$$\frac{d[z]}{q[z]} = \frac{2 - z^{-1}}{1 - z^{-1}}, \tag{4}$$

which has the characteristic response of a direct-form I IIR filter. In Fig. 2(b), the IIR filter is visually represented as a delay-free DT integrator $(1 - z^{-1})^{-1}$ and a unity-gain feedforward path from $q$ to $d$. If $q[0] = d[0] = 0$, then $d[\mathrm{n}]$ is the cumulative sum of all $q$ and $q[\mathrm{n}]$, *i.e.*, $d[\mathrm{n}] = q[\mathrm{n}] + \sum_{i=1}^{n} q[i]$, showing that one way of implementing the IIR filter is with an accumulator and adder. In this work, a 4-bit adder (with an extra overflow bit) was used; therefore, $d$ has a 4-bit resolution.

A transient waveform of the proposed 1st-order ΔΣ with an IIR quantizer is shown in Fig. 3. The inclusion of the IIR filter results in the output bitstream, $d$, tracking $u$, as in a multi-bit modulator. Importantly, the IIR filter updates $d$ synchronously with $q$, introducing no excess loop delay (ELD) and thus no stability concerns. As shown in Fig. 3, the IIR quantizer step size can be either $\pm\Delta$ or $\pm 3\Delta$, where $\Delta$ is the minimum step size. Consequently, the 4-bit IIR quantizer has higher quantization noise than a 4-bit Nyquist quantizer, whose quantization step is strictly $\Delta$. A conservative quantization noise analysis reveals that the IIR quantization error, $e_{\mathrm{q}}$, has a uniform probability density function (PDF) bounded between $\pm 3\Delta/2$, thus resulting in a total integrated quantization noise power of $9\Delta^2/12$. Theoretically, the proposed IIR-ΔΣ has 14.6 dB lower quantization noise

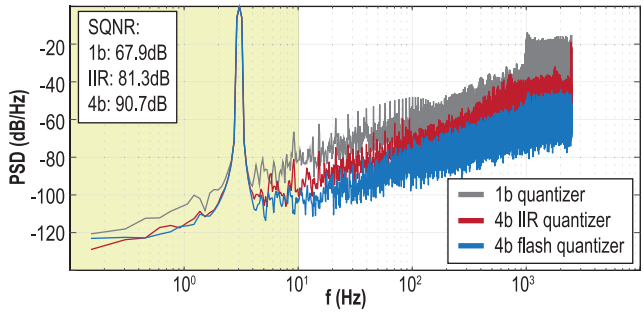


Fig. 4. Simulated SQNR of a 1st-order ΔΣ with a 1-bit, 4-bit IIR, and 4-bit flash quantizer.

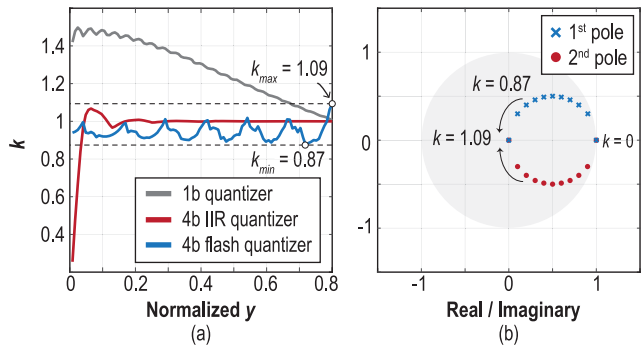


Fig. 5. (a) Simulated quantizer gain, $k$, within the non-overloading range for 1-bit, 4-bit IIR, and mid-tread 4-bit flash quantizers; (b) root locus.

power than a single-bit ΔΣ while still being 9.5 dB higher than a true 4-bit ΔΣ. This is in close agreement with the simulated results shown in Fig. 4 of a 1st-order ΔΣ with an ideal 1-bit, 4-bit IIR, and 4-bit flash quantizer achieving 67.9, 81.3, and 90.7 dB SQNR, respectively, at an OSR of 250. Thermal noise was not included to ensure the modulator is quantization noise limited. For optimal prediction efficacy, the IIR step, $3\Delta$, should be larger than the maximum signal change in one sampling period. It can be shown that an OSR $> 8$ is needed for a 4-bit IIR resolution, which sets a conservative lower bound for the OSR. However, as will be discussed later, an OSR $> 64$ ensures the STF and NTF of the proposed IIR-ΔΣ are identical to its 1-bit counterpart.

The quantizer gain, $k$, of a single-bit quantizer is determined by the statistical correlation between the input and output, specifically the slope of a straight line that minimizes the error between $y$ and $d$ for a given range of $y$ [32], namely

$$k = \frac{\langle d, y \rangle}{\langle y, y \rangle} \tag{5}$$

where $\langle d, y \rangle$ is the cross-correlation between $d$ and $y$ and $\langle y, y \rangle$ is the autocorrelation of $y$. The simulated $k$ values for a 1-bit, 4-bit IIR, and 4-bit flash quantizer are shown in Fig. 5(a). For illustration purposes, the quantizer input, $y$, was swept from 0 to 80% of the full-scale range (FSR), at which point $k_{1\mathrm{b}} = 1$, whereas in transient simulation, $y$ was kept within 20% FSR for all $u$. As expected, $k_{\mathrm{flash}}$ has near unity gain and $k_{1\mathrm{b}}$ monotonically increases as $y$ decreases resulting in an input-dependent

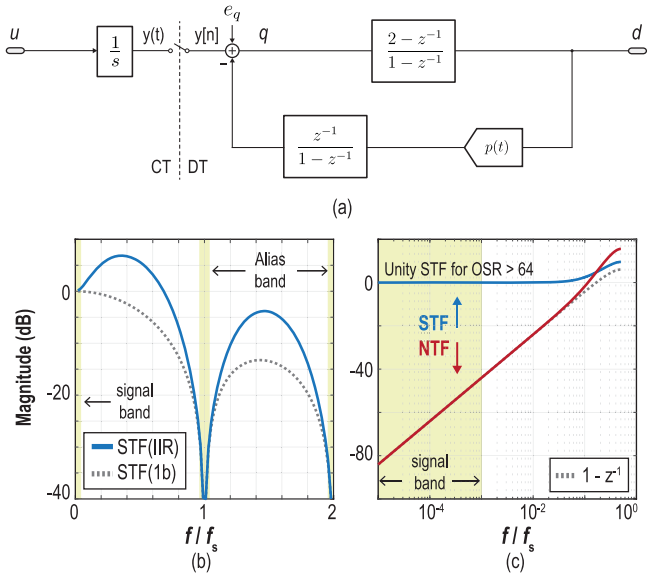


Fig. 6. (a) Mathematical model of the IIR-$\Delta\Sigma$ separated into the continuous- and discrete-time domains; (b) STF of IIR-$\Delta\Sigma$ and 1-bit $\Delta\Sigma$ showing the inherent anti-aliasing and (c) STF and NTF of the IIR-$\Delta\Sigma$.

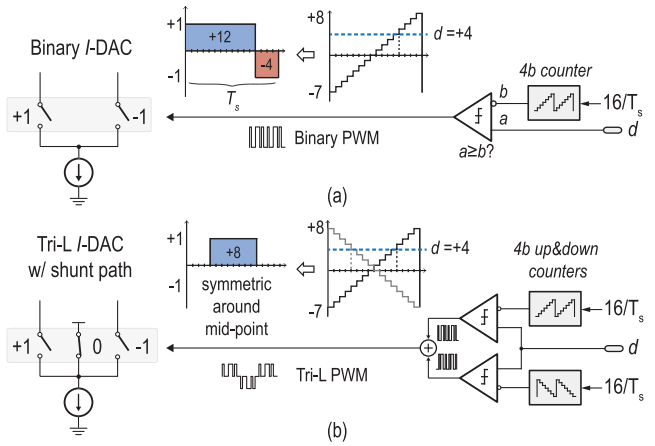


Fig. 7. Visualization of (a) two-level PWM with current-steering DAC and (b) tri-level PWM with current-steering DAC with additional shunt path.

gain. Importantly, $k_{\mathrm{IIR}}$ closely tracks $k_{\mathrm{flash}}$ with a minimum and maximum of 0.87 and 1.09, respectively. The variation of $k_{\mathrm{IIR}}$ exhibits input-dependence, and the effect of varying $k$ on the modulator's noise transfer function (NTF) is

$$NTF_{\mathrm{k}}(z) = \frac{\frac{2-z^{-1}}{1-z^{-1}}}{1 + L(z)\,k}, \tag{6}$$

where $NTF_{\mathrm{k}}(z)$ is the NTF with a quantizer gain of $k$ and $L(z)$ is the loop filter gain with $k = 1$. Fig. 5(b) shows a root locus with $k$ varying from 0.87 to 1.09. The IIR quantizer introduces a pair of conjugate poles residing within the unit circle and therefore has a negligible impact on the modulator's stability.

The addition of the IIR filter changes the modulator's signal transfer function (STF) and NTF. Fig. 6(a) shows the equivalent analytical model for the proposed IIR-$\Delta\Sigma$, where $p(t)$ is a generalized pulse function representing the tri-level PWM DAC. In the case of a CT $\Delta\Sigma$, the block diagram can be redrawn such that the CT integrator and sampler are rearranged to better visualize the STF and NTF. The STF in the CT domain is found by multiplying the CT integrator by the NTF evaluated at $e^{j2\pi f}$, *i.e.*,

$$NTF(z) = \left(2 - z^{-1}\right)\left(1 - z^{-1}\right) \tag{7}$$

$$STF(f) = \frac{1}{j2\pi f}\left(2 - e^{-j2\pi f}\right)\left(1 - e^{-j2\pi f}\right). \tag{8}$$

Fig. 6 shows the effect of the extra scaling factor $(2 - z^{-1})$ in the STF and NTF compared to those of a standard 1-bit CT $\Delta\Sigma$. Although this extra term contributes to slightly higher out-of-band gain (OBG), its in-band effect is negligible, as can be seen when $f \to 0$, the $(2 - z^{-1})$ term evaluates to unity. Fig. 6(b) shows that the modified STF preserves the inherent anti-aliasing property by having notches at integer multiple of $f_{\mathrm{s}}$. For an OSR $> 64$, the IIR-$\Delta\Sigma$ has a nearly identical STF and NTF to its 1-bit counterpart, as shown in Fig. 6(c). The NTF's OBG is increased by $\sim$9 dB, which results in a 2 dB loss in the maximum stable amplitude (MSA). The effect of increased OBG on MSA is more prominent in higher-order modulators [34]. It is also worth noting that in higher-order modulators, the *Bode sensitivity integral* suggests that higher OBG helps attenuate in-band noise (IBN) [32]; however, in an IIR-$\Delta\Sigma$ this has no effect due to the extra scaling factor.

### C. Tri-Level PWM DAC

The addition of an IIR filter necessitates a multi-bit DAC to close the loop. Since any nonlinearity introduced by the feedback DAC is directly added to input, the DAC must be as linear as the overall modulator. A conventional multi-bit DAC implementation uses unit or weighted cells with DEM or data-weighted averaging (DWA) to randomize/shape the mismatch [35], [36]. However, this typically results in a large area for an I-DAC as each current source transistor still needs to be sized relatively large to minimize the residual 1/*f* noise after DEM or DWA. It also has a power penalty from the circuitry used to generate the pseudo-random bit sequence [27]. As a result, an area- and power-efficient implementation is needed for multi-channel applications like µTIMES.

Critically, in a 1$^{\mathrm{st}}$-order CT $\Delta\Sigma$, it can be shown that the modulator is insensitive to the shape of the feedback waveform as long as the total charge delivered in each cycle is proportional to the digital code, *i.e.*,

$$\int_0^{T_{\mathrm{s}}} p(t)dt = d[\mathrm{n}], \tag{9}$$

where $p(t)$ is the feedback pulse, $d[\mathrm{n}]$ is the normalized output code, and $T_{\mathrm{s}}$ is the sampling period. In other words, feeding back a fraction of the reference for $T_{\mathrm{s}}$ is equivalent to feeding back the full-scale reference for the same fraction of $T_{\mathrm{s}}$. The only difference is that for the latter, just a single unit DAC is needed, so nonidealities such as asymmetric rise/fall time

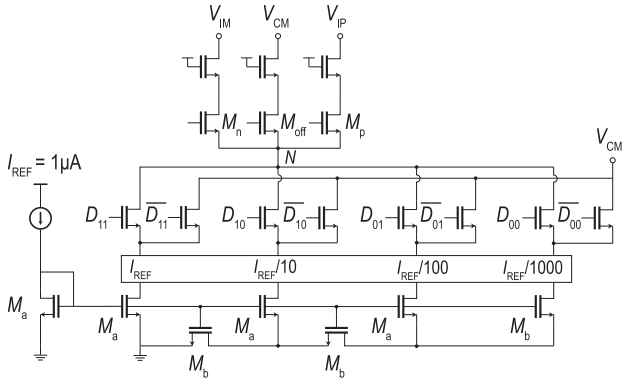


Fig. 8. Circuit implementation of the large dynamic range current reference using current-splitting.

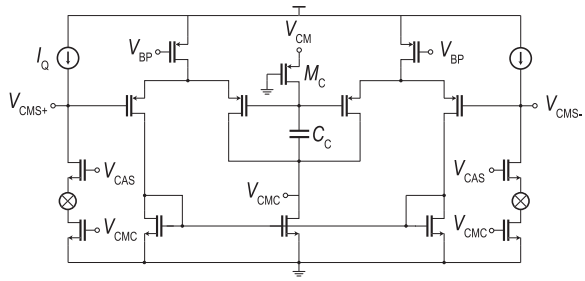


Fig. 9. Circuit implementation of the CMFB amplifier (biasing not shown).

introduce a constant offset that is common to all codes. To evenly partition $T_{\rm s}$, a faster, synchronized clock can be used at the cost of increased jitter sensitivity. For example, in a 4-bit IIR implementation, a clock at $16/T_{\rm s}$ can clock a 4-bit counter and generate a two-level PWM waveform, as shown in Fig. 7(a). The modulator output code, $d$, is held during each $T_{\rm s}$ and compared to the counter. The two-level PWM waveform is generated by combinational logic that determines if $d$ is greater or equal to the counter.

Although a two-level PWM waveform is inherently linear, this work implements a tri-level PWM for better noise performance, as shown in Fig. 7(b). By having a dedicated "0" (shunt) state, linearity is no longer maintained with current source mismatch. The "0" state introduced by the tri-level PWM disconnects the feedback from the loop, effectively bypassing the thermal noise from the current sources, which results in lower input-referred noise for small inputs. By combining a pair of two-level PWM signals, the tri-level PWM is essentially a half-scale return-to-zero (RZ) pulse train that is free of even-order distortion [37]. Reducing the feedback amplitude by half also relaxes the linearity requirement for the loop filter since the amplifier only needs to sink or source a fraction of the current. For the same reason, the tri-level PWM has a 6 dB lower jitter sensitivity than the two-level PWM. For all codes except $\pm 1$, the feedback pulse in a tri-level implementation is a fraction of the sampling period and symmetric around the midpoint. Thus, the tri-level PWM DAC is also robust against intersymbol interference (ISI).

The tri-level PWM is used to modulate an I-DAC. An I-DAC was chosen over its resistive counterpart (R-DAC) for two reasons. First, to partition a large DR over multiple references, the DAC should have scalability over a large range. For current sources, current-splitting can generate a reference current over several decades while maintaining a relatively compact area. Second, resistive loading from an R-DAC at the virtual ground reduces the loop gain around the loop filter. The situation is exacerbated when the resistors are large and have large parasitic capacitance. The reduced feedback factor increases the input-referred noise and degrades the integrator's linearity. In contrast, cascoded current sources ensure that the I-DAC has a large output impedance across the entire reference range.

## IV. Circuit Implementation

### A. Current-Splitting DAC

The reference for each channel is generated from a programmable 2-bit current-splitting DAC [38] that progressively divides a 1 $\mu$A reference current, $I_{\rm REF}$, by a factor of $10\times$ down to 1 nA, as shown in Fig. 8. Current-splitting is inherently linear, regardless of the transistor's region of operation. Transistors $M_{\rm a}$ and $M_{\rm b}$ form a ratiometric current-splitting chain, like an *R*-2*R* ladder. The current through each branch is proportional to the transistor's *W*/*L* where the unit transistor, $M_{\rm b}$, is 10 $\mu$m/10 $\mu$m for low 1/*f* noise and good matching such that the relative error at $I_{\rm REF} = 1$ nA is within 10%. Transistors $M_{\rm a}$ are proportionally sized 90 $\mu$m/10 $\mu$m for splitting by a factor of $10\times$. All transistors are biased in subthreshold, and $M_{\rm a}$ and $M_{\rm b}$ are implemented using thick-oxide, deep n-well (DNW) devices to minimize leakage. Cascode transistors boost the output impedance by $160\times$ to ensure negligible impact on the overall input impedance seen by the sensor and precise current mirroring down to 1 nA. High output impedance in the I-DAC is also critical to ensure the virtual ground voltage does not modulate the current. When one of the four references is selected, the other three branches are shunted to $V_{\rm CM}$ at 0.9 V. The tri-level functionality is realized with switches $M_{\rm p}$, $M_{\rm n}$, and $M_{\rm off}$, whose source voltages are always maintained at the virtual ground voltage, thus reducing the transition delay and distortion from signal-dependent perturbation at the tail node, *N*. Cascode transistors isolate the integrator inputs from the switching transistors to minimize distortion from clock feedthrough.

### B. Input Common-Mode

Since the inputs are directly connected to high impedance on-chip electrodes, a system-level continuous-time common-mode feedback (CMFB) [39] is needed to set the input common-mode voltage while providing a high output impedance at the current summing nodes. The CMFB does not affect the normal operation of the modulator since the CMFB only responds to common-mode variation, whereas the I-DAC operates in differential-mode. As shown in Fig. 9, the CMFB consists of a two-stage differential difference amplifier (DDA) to ensure a high dc loop gain ($> 90$ dB) and minimize input common-mode

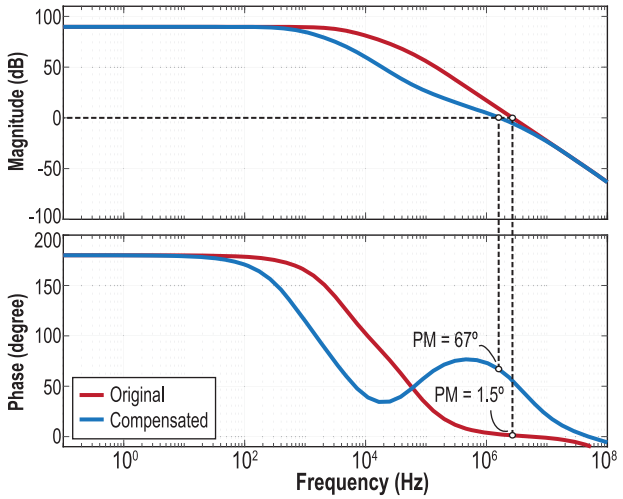


Fig. 10. Simulated loop gain of CMFB with LHP zero compensation.

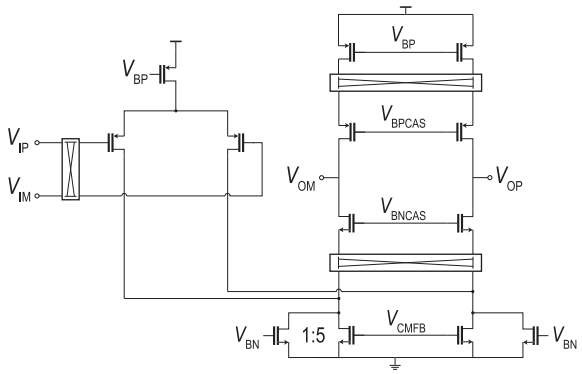


Fig. 11. Circuit implementation of the chopper-stabilized folded-cascode OTA (biasing and CMFB not shown).

offset while still allowing for large input swing. In the DDA, the four input transistors average and compare the differential input voltage, $V_{\rm CMS}$, to the desired reference voltage, $V_{\rm CM}$. The difference is then amplified and converted into a common-mode output current to adjust $V_{\rm CMS}$ until it matches $V_{\rm CM}$. Similar to the I-DAC, the CMFB has a cascoded output stage ($I_{\rm Q} = 500$ nA) for high output impedance such that the output current is independent of the virtual ground voltage. In this two-stage amplifier, the second stage contributes a pole at ∼3 kHz, and the first stage has a second pole at ∼30 kHz. As such, the two low-frequency poles result in less than 1.5° phase margin without compensation. A left-half-plane zero was added by connecting $V_{\rm CM}$ to a 10 pF capacitance, $C_{\rm C}$, and a long-channel triode PMOS (220 nm/1 µm), $M_{\rm C}$, with a ∼250 kΩ impedance. These place a zero near the unity-gain frequency, increasing the phase margin to 67°. Fig. 10 shows the simulated loop gain of the amplifier with and without the compensation. The conductance of $M_{\rm C}$, and therefore the phase margin of the CMFB, will deviate due to process variation. A 100-point Monte Carlo simulation showed an average phase margin of 66° with a standard deviation of 5°, ensuring CMFB stability. At start-up, the input common-mode voltage is near ground. Therefore, only a PMOS-input CMFB is necessary to stabilize the input common-mode voltage to $V_{\rm DD}/2$ and remains within the input-common range after that.

### C. Chopper-Stabilized OTA

A conservative rule of thumb is that the OTA dc gain should be approximately equal to the OSR such that the increase in quantization noise due to NTF zero shift is negligible [40]. However, finite integrator gain and the nonlinear nature of the quantizer can lead to dead-zones where the modulator is unresponsive to small input signals. Therefore, the dc gain requirement of the OTA in a 1st-order ΔΣ is particularly stringent. In this work, the OTA dc gain was chosen to be at least 80 dB. Because the feedback DAC is modulated at 16× the sampling frequency, the OTA's unity-gain frequency (UGF) should be at least $16\times f_{\rm s} = 80$ kHz to avoid increasing the in-band noise (IBN) and nonlinearity.

A fully-differential folded-cascode amplifier was implemented for good energy efficiency and large output swing, as shown in Fig. 11. Large PMOS input transistors (40 $\mu$m/1 $\mu$m) were used to reduce 1/*f* noise while maximizing the $g_{\rm m}$ for low input-referred noise and offset. The other transistors are sized to have $g_{\rm m}/I_{\rm D} > 18$ S/A with a 1 $\mu$A bias current. Chopper stabilization was used at the inputs and low-impedance nodes of the cascode stage to further reduce 1/*f* noise and offset. A chopping frequency of $f_{\rm s}/2$ was chosen to avoid noise folding. The CMFB is a DDA-based amplifier load compensated with a 10-pF capacitor to achieve a phase margin of 86°. A 1:5 current ratio was used to partition the CMFB and bias currents for robustness.

From simulation of the extracted amplifier layout, the OTA has an 84 dB dc gain, 8 MHz unity-gain bandwidth, and an ∼80 kHz 1/*f* corner. A 100-point Monte Carlo simulation shows a mean offset of 78 µV after chopping, with a standard deviation of 8 µV. Notably, the OTA offset voltage does not impact the modulator linearity but results in an offset current from the input impedance. The input-referred noise was reduced from 620 to 26 nV/$\sqrt{\rm Hz}$ with chopping at 100 kHz, which results in a negligible current noise of 4 $\rm fA_{rms}$ for the 20 MΩ input impedance of the modulator. The input-referred current noise is dominated by the shot noise and residual flicker noise of the CMFB (95%), while only a small fraction is contributed by the OTA (0.1%) and I-DAC (5%).

In current front-ends, the input impedance, $R_{\rm in}$, is a critical parameter because an $R_{\rm in}$ too large will result in in-band noise peaking when combined with a large input capacitance, $C_{\rm in}$, which considerably impacts the total noise performance [41]. The simulated input-impedance of the proposed front-end with the CMFB is ∼110 kΩ at 10 Hz, which is sufficiently low to push the noise zero out of band with the load from the capacitance interface.

### D. Comparator

The comparator is implemented by a preamplifier followed by a regenerative latch, as shown in Fig. 12. The preamplifier has a moderate gain of ∼5 V/V to attenuate the noise from the latch. The propagation delay is less than 10 ns to minimize dead-zones

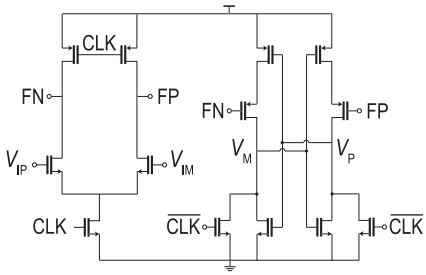


Fig. 12. Circuit implementation of the dynamic comparator (SR-latch not shown).

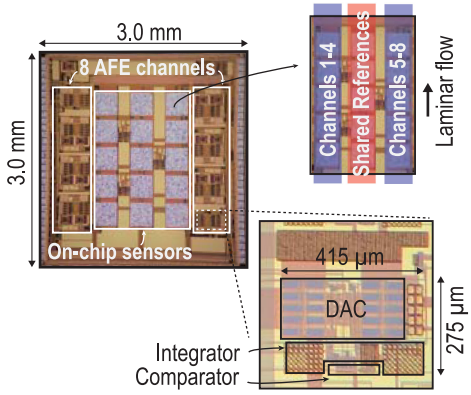


Fig. 13. Die micrograph annotated with microfluidic channels.

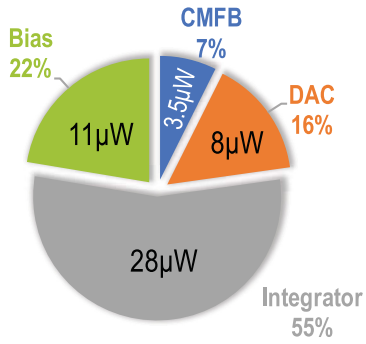


Fig. 14. Measured power breakdown for each readout channel.

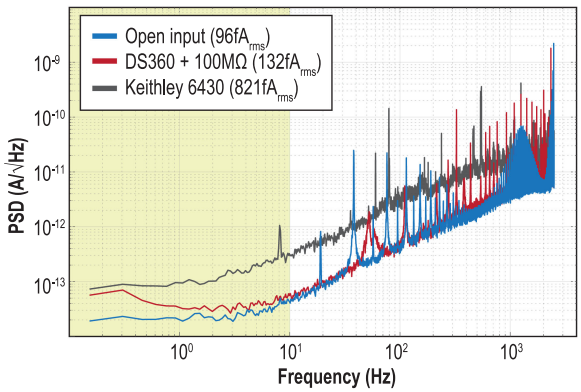


Fig. 15. Measured input-referred current noise PSD with open input and different instruments.

and ELD. The output nodes of the latch, $V_{\rm M}$ and $V_{\rm P}$, connect to an SR latch with high skew inverters to prevent false triggering and minimize dynamic errors. The input-referred noise of the comparator was simulated with transient noise (noisefmax = 10 MHz) and fitting the averaged comparator decisions to an error function for a given range of input offset [42]. The 6.2 $\rm mV_{rms}$ comparator noise is not a concern because the NTF significantly attenuates it.

## V. Measurement Results

This design was fabricated in a 180 nm CMOS process and occupies $3\times3$ $\rm mm^2$. As shown in Fig. 13, there are eight recording channels with four shared reference electrodes. The majority of the chip area is dedicated to on-chip sensors implemented on the top metal layer. The active area per readout channel is 0.11 $\rm mm^2$, including the bias circuits. Electrical and *in-vitro* measurements were performed with the circuit enclosed in a dark faradic cage to suppress 60 Hz interference.

### A. Electrical Characterization

With a 1.8 V supply and $I_{\rm REF} = 1$ µA, the power consumption per channel is 50.3 µW, and the power breakdown is shown in Fig. 14. The digital IIR filter and tri-level PWM logic were implemented off-chip in an FPGA (Opal Kelly XEM6310). If implemented on-chip, these circuits would consume 50 nW based on simulations using synthesized logic. Unless stated otherwise, all measurements were made with $f_{\rm s} = 5$ kHz at an OSR of 250.

The total integrated input-referred noise (IRN) measured with the input floating (open input) was 96.2 $\rm fA_{rms}$ over a 10 Hz bandwidth, as shown in Fig. 15. For sensitive current sensing AFEs, capacitive loading at the input introduces a noise zero that directly amplifies the current noise and limits the resolution. Using a sub-fA SourceMeter (Keithley 6430), the measured IRN was 821 $\rm fA_{rms}$ due to the added capacitive loading. Isolating the instrument's capacitive loading through a 100 MΩ resistor reduced the noise to 132 $\rm fA_{rms}$. The estimated electrical double-layer (EDL) capacitance of the electrode in $1\times$ HEPES is ∼90 nF (∼1 pF/µm$^2$). This large capacitive load increases input-referred current noise to ∼1.2 $\rm pA_{rms}$ (890 $\rm fA_{rms}$ in simulation) in a 10 Hz bandwidth.

For ac measurements, a sinusoidal input current was generated by connecting a low-distortion function generator (SRS DS360) in series with a large resistor for *V*-to-*I* conversion. The resistor introduces a negligible current noise while significantly attenuating the voltage noise of the instrument. The series resistance and the input capacitance of the AFE also low-pass filter the instrument noise. Resistances of 1, 10, 100, and 5000 MΩ were used for input ranges of 1000, 100, 10, and 1 nA, respectively. With a 100 MΩ input resistance, it is shown in Fig. 15 that the *V*-to-*I* configuration leads to comparable IRN as the open-input configuration.

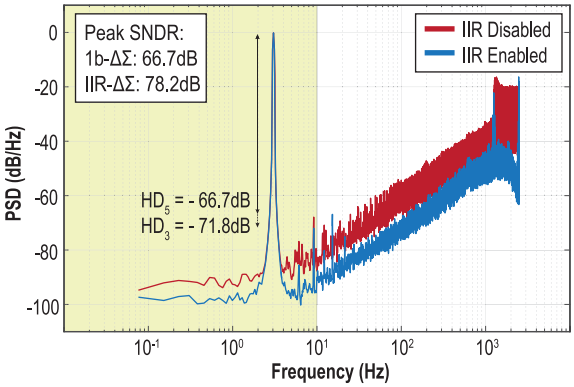


Fig. 16. Measured peak SNDR for a single-bit and IIR-ΔΣ at -2 dBFS input.

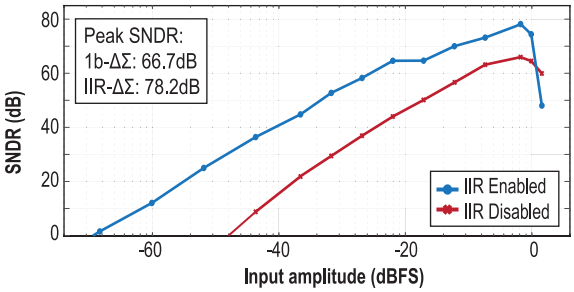


Fig. 17. Measured SNDR vs. input amplitude of single-bit and IIR-ΔΣ.

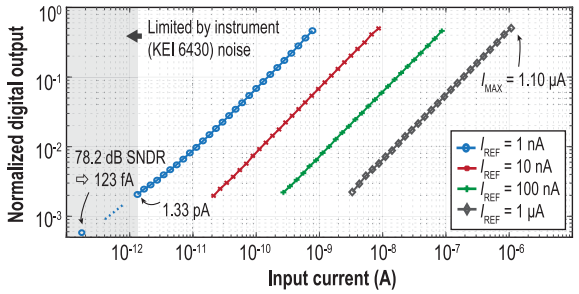


Fig. 18. Measured cross-scale dynamic range of IIR-ΔΣ.

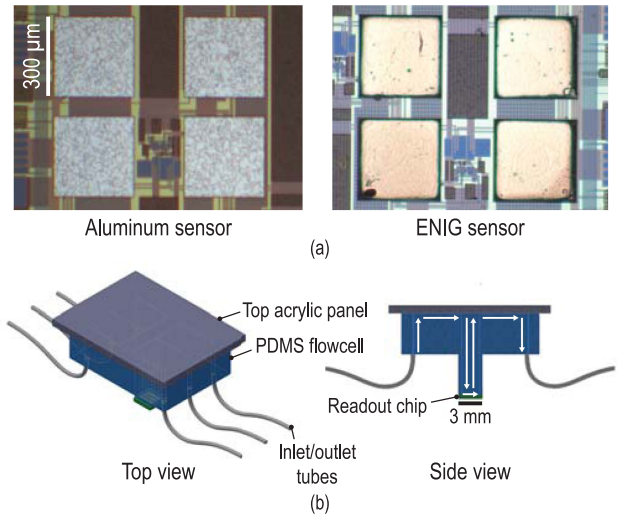


Fig. 19. (a) Optical images of aluminum sensor surface post-treated with ENIG and (b) top and side view of PDMS microfluidic flow cell.

Fig. 16 shows the measured spectra of single-bit and IIR-ΔΣ with a –2 dBFS sinusoidal input at 3.052 Hz. The peak SNDR of the IIR-ΔΣ was 78.2 dB – an 11.5 dB improvement over its single-bit counterpart. This is slightly lower than the simulated 14.6 dB improvement shown in Fig. 4 due to increased harmonic distortion (HD), specifically $HD_3$ and $HD_5$ at -66.7 dB and -71.8 dB, respectively. The increased HD is due to mismatch in the tri-level PWM DAC. The measured relative error (from a stand-alone DAC test structure) increases as $I_{REF}$ scales down from 0.12% at 1 μA to 9.9% at 1 nA.

Fig. 17 shows the SNDR plotted against the input amplitude. The measured DR demonstrates that the modulator has performance commiserate with a multi-bit quantizer by exhibiting a 21.5 dB improvement in the DR for low input amplitudes, where a significant amount of the current source noise is shunted from the input by the "0" state of the tri-level PWM DAC. The SNDR of the IIR-ΔΣ rolls off much more sharply than its 1-bit counterpart for inputs larger than full-scale. To plot the entire working range of the reported AFE, a sub-fA SourceMeter was used to sweep the dc current from 100 fA to 1.1 μA. As shown in Fig. 18, the minimum was limited by the instrument and measured to be 1.33 pA, which is consistent with the integrated input-referred noise measured for the instrument shown previously. The sensitivity of 123 fA was defined by the peak SNDR measured at 1 nA reference. This AFE achieves a 78.2 dB DR and a 139 dB cross-scale DR.

### B. *in-vitro Measurements*

The top metal of most CMOS processes is aluminum, which is prone to oxidation in ionic solutions. Therefore, before microfluidic assembly, the μTIMES chip was treated with an electroless nickel immersion gold (ENIG) to coat the sensor surface with gold. Fig. 19(a) shows the ENIG post-processed device. The microfluidics used in this work consists of two layers of polydimethylsiloxane (PDMS) to deliver reagents to the sensing area, as shown in Fig. 19(b). The microfluidic mold was fabricated by patterning a positive photoresist (SU8-2050) on a four-inch silicon wafer. The silicon wafer was cleaned with acetone, methanol, and isopropanol sequentially with sonication. The surface was then treated with $O_2$ plasma (Technics PEIIB Planar Etcher). SU8 was spin-coated and patterned. Two 30-μm thick molds were formed on the wafer. The microfluidic flow cell was fabricated by pouring PDMS on the mold and curing it at 65°C overnight. To bond the PDMS and μTIMES chips, ultraviolet/ozone treatment was used to activate the surface. Finally, the microfluidic blocks were aligned and bonded using an acrylic plate to apply pressure for sealing.

In the following proof-of-principle *in-vitro* experiment, Lysozyme, an enzyme that hydrolyzes polysaccharide chains, and its specific ligand, N,N,N"-triacetylchitotriose ($NAG_3$),

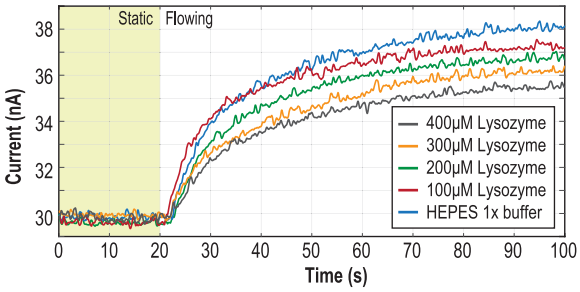


Fig. 20. *in-vitro* measurement results of Lysozyme at various concentrations.

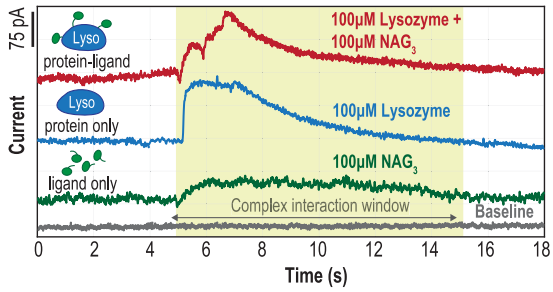


Fig. 21. *in-vitro* measurement results of Lysozyme, $NAG_3$, and 1:1 mixture of Lysozyme and $NAG_3$.

were prepared in 1× HEPES buffer at 7.16 pH. A standard dialysis procedure was performed for the HEPES buffer to maintain buffer consistency throughout the experiment. A washing buffer containing 25 mM tris, 150 mM NaCl, and 1% CHAPS was used to remove biomolecule residues and preserve ENIG integrity between experiments. All *in-vitro* experiments were performed at a pump rate of 10 μL/min to avoid channel leakage. Signals were decimated to a 10 Hz bandwidth without additional post-processing, such as offset removal and filtering. Each experiment was performed multiple times to verify the reproducibility. More TIMES experimental data can be found in [14]–[16].

At the start of an *in-vitro* flow experiment, the microfluidic channel with the reference sensor was filled with 1× HEPES buffer, and the channel with the working electrode was soaked in 1× HEPES buffer containing Lysozyme at different concentrations ($100 - 400\ \mu$M). At $t = 20$ s when the syringe pump was turned on to displace the solution over the working electrode with buffer, the output current rose and settled at a new level dependent upon the Lysozyme concentration (Fig. 20). Between each Lysozyme run, the channel was rinsed with washing buffer to preserve sensor integrity and remove sensing artifacts due to the experiment sequence. This can be verified that the initial baseline for each run settled to a consistent value of 30 nA in Fig. 20.

The baseline signal (*i.e.*, response from 1× HEPES without Lysozyme) between running buffer over the working electrode and the still buffer over the background electrode is from the electro-osmosis effect where the pressure-driven flow caused a net ionic current near the electrode. In electro-osmotic flow, the velocity profile is constant along the cross-section of the channel, as opposed to a parabolic profile for laminar flow. Assuming the system has a negative zeta potential, cations are accumulated at the electrolyte/electrode interface, and the flow of cations produces a net current immediately above the electrode. This ionic flow creates a voltage drop, thus changing the oxidation rate of the Au electrode. By adding Lysozyme to the buffer, the Lysozyme adsorbed to the electrode and increased the effective spacing between the ions and the electrode, reducing the electro-osmosis-induced oxidation current. When the buffer solution is introduced to the channel, the absorbed Lysozyme are desorbed from the electrode surface, generating the signal corresponding to this dynamic process in Fig. 20. We demonstrate that the coupling of the microfluidic device and the electronic circuit allows us to characterize molecular coating on a surface, a key parameter for electrochemical biosensors where capture probes need to be deposited on metal surfaces with an optimal surface coverage.

Fig. 21 shows measured transient signatures for different protein-ligand configurations. The *in-vitro* data was sampled (50 kHz) and decimated (100 Hz) at a 10× faster rate to show clearer temporal details. This experiment investigates the biochemical reaction produced by Lysozyme (protein), $NAG_3$ (ligand), and a 1:1 mixture of Lysozyme and $NAG_3$, which produces Lysozyme-$NAG_3$ complex having its concentration determined by the dissociation coefficient (*i.e.*, the inverse of the reaction constant) of the two molecules. In parallel experiments, sample solutions (Lysozyme, $NAG_3$, and Lysozyme-$NAG_3$ complex) were injected into the working channel to displace buffer solution pre-filled at the start of each recording. The difference in the signal can be attributed to the dipole moment difference of each biomolecule compound as they approach the electrode. For the same concentration of Lysozyme and $NAG_3$, the resulting current of $NAG_3$ is noticeably lower than Lysozyme due to a much smaller dipole moment. On the other hand, even though the size, molecular weight, and dipole moment of $NAG_3$ are much smaller than those of Lysozyme, $NAG_3$ still significantly alters the structure stability and the dipole moment direction of Lysozyme, giving rise to differently induced electrical responses. The signal produced by the mixture of $NAG_3$ and Lysozyme in a 1:1 ratio is not a superposition of signals from the individual molecules, suggesting that the two molecules react to form a protein-ligand complex. A detailed analysis of the waveforms allows one to obtain the dissociation coefficient of the reaction.

Table II compares this work to other state-of-the-art current sensing front-ends. This work achieves the best input-referred current noise density of 30.3 fA/√Hz by utilizing linear prediction and a return-to-open I-DAC in the feedback loop. The added digital logic was shown to contribute little power (and area) overhead. The resolution-to-power tradeoff was captured by the resolution-FoM, which is widely used to characterize the power efficiency of sensor front-ends [43]–[45]. This work achieves the best FoM of 0.046 $pA^2\mu J$, which is 7.4× better than other current sensing front-ends. While it is tempting to scale down the reference current, $I_{REF}$, to attempt a better resolution-FoM, the overall signal-to-noise ratio (SNR) is compromised with a smaller input range. Therefore,

TABLE II
COMPARISON TO PRIOR CURRENT SENSING AFES

| | [23] Stanacevic TBCAS'07 | [24] Li TBCAS'16 | [25] Son TBCAS'17 | [26] Ghoreishizadeh TBCAS'17 | [27] Hsu ISSCC'18 | [29] Wu ISSCC'21 | [22] Lu TBCAS'21 | **This work** |
|---|---|---|---|---|---|---|---|---|
| AFE Architecture | Inc. $\Delta\Sigma$ | Inc. $\Delta\Sigma$ | $\Delta\Sigma$ | TIA + SAR | Hourglass $\Delta\Sigma$ | $\Delta\Sigma$ | CC + *I*-to-*F* | IIR-$\Delta\Sigma$ |
| Technology Node (nm) | 500 | 500 | 350 | 350 | 180 | 55 | 180 | 180 |
| On-chip Sensors? | × | × | × | Yes | × | × | × | Yes |
| Number of Channels | 16 | 50 | 1 | 1 | 1 | 1 | 1 | 8 |
| Area/ch. ($mm^2$) | 0.25** | 0.157 | 0.5 | 0.6 | 0.2 | 0.585 | 3.17 | 0.11 |
| Power/ch. (μW) | 3.4 | 241 | 16.8 | 9,300 | 295 | 1011 | 25 | 50.3 |
| Max Input (μA) | 1 | 16 | 2.8 | 20 | 10 | 200 | 10 | 1.1 |
| IRN* (fA) @ BW (Hz) | 100 @ 0.1 | 100 @ 1 | 22,000 @ 10 | 470 @ 10 | 100 @ 1.8 | 2,000,000** @ 4k | 87,000 @ 0.15 | 96 @ 10 |
| Dynamic Range (dB) | 40** | 54** | 77.5 | 65.9** | 160 | 140 | 58 | 78.2 |
| Cross-scale DR (dB) | 140 | 164 | - | 156 | - | - | - | 139 |
| IRN Density (fA/√Hz) | 316 | 100 | 6,960 | 149 | 74.5 | 31,600 | 225,000 | 30.3 |
| FoM*** ($pA^2$μJ) | 0.34 | 2.4 | 810 | 210 | 1.0 | 1,000,000 | 1,300,000 | 0.046 |

*Measured with open input; **Not explicitly given; ***FoM = resolution$^2$ × energy/conversion; Cross-scale DR = $I_{MAX}/I_{MIN}$;
IRN: input-referred noise; Inc. $\Delta\Sigma$: incremental $\Delta\Sigma$ CC: current conveyor.

it is not a good design strategy to shrink $I_{REF}$ only for noise purposes. The merit of this work is that it achieves the best resolution-FoM while having a comparable dynamic range as other work listed in Table II. It is also worth noting that the high resolution achieved by this work is not from having a small I-DAC reference. Instead, it is from the advantage of using a tri-level PWM I-DAC where most I-DAC noise is shunted away from input.

## VI. CONCLUSION

This paper presents a multi-channel current sensing front-end that achieves 123 fA sensitivity and 139 dB cross-scale DR while consuming only 50.3 μW and 0.11 $mm^2$ per readout channel. In each channel, a 1st-order CT-$\Delta\Sigma$ was implemented with a digital IIR filter and tri-level PWM DAC. The IIR filter linearly predicts the input magnitude from single-bit quantization results and generates a multi-bit resolution output. The tri-level PWM DAC modulates the feedback current pulse width to achieve multi-bit feedback. The resulting modulator is a low-power and compact AFE used to characterize real-time protein-ligand interaction in a label- and immobilization-free manner.

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