

# A 26.5 pA<sub>rms</sub> Neurotransmitter Front-End With Class-AB Background Subtraction

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**Abstract**—This paper presents an analog front-end (AFE) for fast-scan cyclic voltammetry (FSCV) with analog background subtraction using a pseudo-differential sensing scheme to cancel the large non-faradaic current before seeing the front-end. As a result, the AFE can be compact and low-power compared to conventional FSCV AFEs with dedicated digital back-ends to digitize and subtract the background from subsequent recordings. The reported AFE, fabricated in a 0.18- $\mu\text{m}$  CMOS process, consists of a class-AB common-mode rejection circuit, a low-input-impedance current conveyor, and a 1<sup>st</sup>-order current-mode delta-sigma ( $\Delta\Sigma$ ) modulator with an infinite impulse response quantizer. This AFE achieves an effective dynamic range of 83 dB with a state-of-the-art 39.2 pA<sub>rms</sub> input-referred noise when loaded with a 1 nF input capacitance (26.5 pA<sub>rms</sub> open-circuit) across a 5 kHz bandwidth while consuming an average power of 3.7  $\mu\text{W}$ . This design was tested with carbon-fiber microelectrodes scanned at 300 V/s using flow-injection of dopamine, a key neurotransmitter.

**Index Terms**—Analog background subtraction, current conveyor, current-mode delta-sigma modulator, fast-scan cyclic voltammetry, neurotransmitter.

## I. INTRODUCTION

THE nervous system controls nearly all bodily function by directing communication between the various organs. This coordination occurs through electrical (*i.e.*, action potentials propagating along axons) and chemical (*i.e.*, release and uptake of neurotransmitters across synaptic junctions) signaling [1]–[4]. Accurate action potential monitoring has been achieved with large-array extra-/intra-cellular voltage recording front-ends [5]–[8]. Quantitatively studying neurotransmitters is also important in neurological research as disturbances in these chemical messengers influence numerous health conditions, including addiction, anxiety, cognition, and movement disorders [9]–[12]. Dopamine is a neurotransmitter closely linked to reward-motivated behavior, and its dysfunction is often involved in many psychiatric disorders like schizophrenia and Parkinson’s disease [13].

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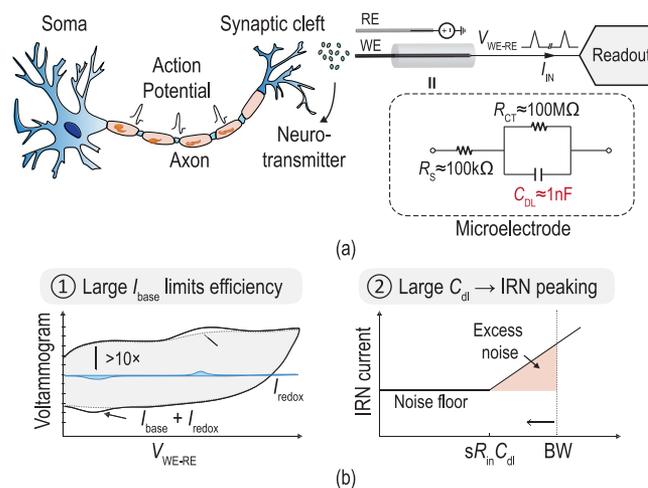


Fig. 1. (a) Overview of a neurotransmitter model and typical FSCV readout system; (b) practical challenges in FSCV front-end designs.

Several techniques have been proposed for neurotransmitter detection and real-time monitoring to diagnose and analyze neurological diseases. For example, nuclear medicine tomographic imaging (single-photon [14] and two-photon [15]) detects photon emission from a radioactive tracer injected intravenously to map neuronal activity in three dimensions. Optical techniques such as Raman spectroscopy [16] or Forster resonance energy transfer (FRET) [17] can also observe neurotransmitters with high sensitivity. Since most neurotransmitters are electroactive, electrochemical techniques such as amperometry [18] and fast-scan cyclic voltammetry (FSCV) [19]–[21] have gained popularity as a non-optical alternative. Fig. 1(a) illustrates a typical FSCV system in which microelectrodes rapidly sweep the potential to oxidize and reduce analytes of interest. The redox current is measured and plotted as a function of the applied potential. The resulting voltammogram provides a “fingerprint” for analyte identification and quantification [22]. As such, FSCV can achieve excellent spatial and temporal resolution.

Like most current-sensing circuits, an FSCV analog front-end’s (AFE) performance is heavily affected by capacitive loading from the sensor. With electrochemical sensors, the input capacitance is dominated by the double-layer capacitance,  $C_{dl}$ , due to the electrode-electrolyte interface, which is typically a few nanofarads [23], [24]. This large  $C_{dl}$  is particularly problematic in FSCV since the working electrode (WE) is swept at 300–400

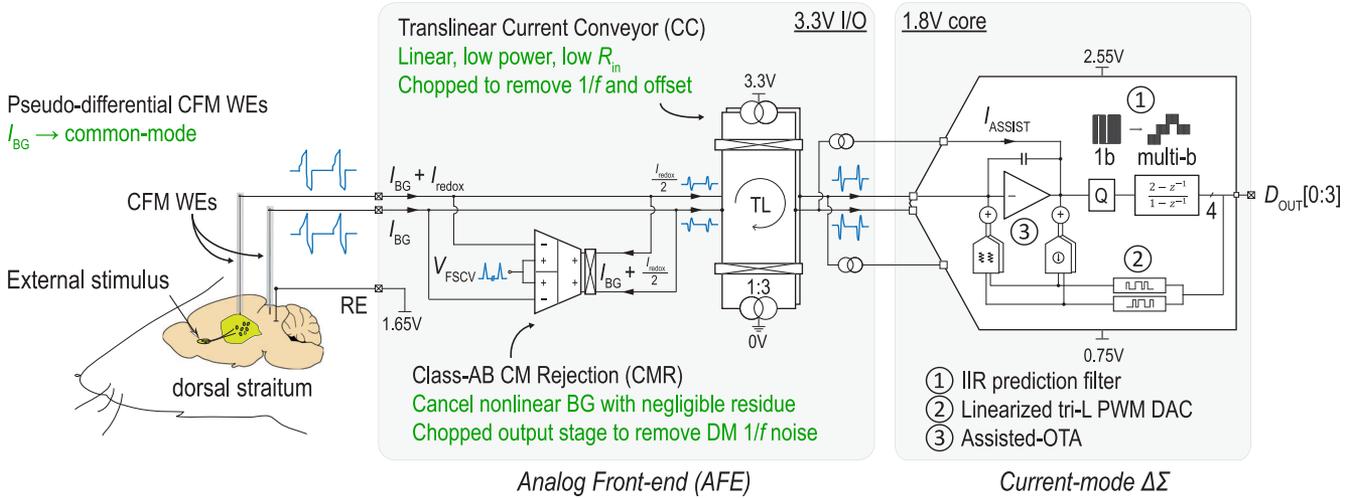


Fig. 2. System architecture of the pseudo-differential FSCV front-end with background current cancellation.

V/s for high temporal resolution, which unavoidably introduces a large (300-400 nA) non-faradaic current,  $I_{BG}$ , superimposed on the much smaller faradaic signal current,  $I_{redox}$  ( $< 10$  nA), as shown in Fig. 1(b).

There has been increasing effort in integrating FSCV AFEs with wireless telemetry to enable real-time monitoring of dopamine release in freely moving small animals necessitating low-power designs [25]–[34]. These designs have two main issues: the non-faradaic background current and the input impedance since it is tied to the noise performance. The large  $I_{BG}$  has typically been dealt with by recording a reference scan at the start of the experiment to capture a neurotransmitter-free background signal that is subtracted from subsequent scans in software. However, resolving the quasi-repetitive large background current requires an AFE with a high dynamic range (DR), increasing the power consumption. Therefore, several techniques have been reported to cancel  $I_{BG}$  such that the AFE output is primarily  $I_{redox}$  from the neurotransmitter of interest. In [26], a digital signal processor (DSP) performed background subtraction on-chip, but with a significant area and power cost. In [27] and [35], a two-step approach stored and subtracted  $I_{BG}$  after the transimpedance stage; however, this still requires the ADC and DAC to have high DR. The lowest power design, described in [36], cancels  $I_{BG}$  prior to it seeing the front-end with a coarse subtraction, but the nonlinear nature of an FSCV signal requires sophisticated calibration to be effective. The second challenge described in Fig. 1(b) is the need for a low input impedance,  $R_{in}$ . A small  $R_{in}$  is crucial so that the noise zero introduced by  $sR_{in}C_{dl}$  is beyond the signal bandwidth.

In this work, we overcome the aforementioned challenges using a pseudo-differential sensing scheme and a common-mode rejection (CMR) circuit that cancels  $I_{BG}$  before seeing the front-end. When the electrode properties (*e.g.*, electrolyte, material, size) are nominally the same,  $C_{dl}$  (and therefore  $I_{BG}$ ) track and can be turned into a common-mode (CM) signal that is canceled by a CMR circuit in the front-end. In Fig. 2, the *in-vivo* system is shown, where the main WE is placed in the dorsal striatum, and a replica WE is placed in a less

active region. The two WEs are surrounded by cerebrospinal fluid (CSF), a common fluid found in vertebrates' brains, and thus present similar  $C_{dl}$  at the front-end input. The resulting differential current is only the faradaic and residual background current copied to a current-mode ADC by a class-AB regulated current conveyor (RCC) for low input impedance. The ADC is implemented as a 1<sup>st</sup>-order delta-sigma ( $\Delta\Sigma$ ) modulator with an assisted-operational transconductance amplifier (OTA) and an infinite impulse response (IIR) quantizer for high energy efficiency [37], [38]. The architecture can tolerate  $I_{BG}$  up to 290 nA without a differential linearity penalty, achieving an effective DR of 83 dB. Furthermore, it has the lowest input-referred noise (39.2 pA<sub>rms</sub>) over a 5 kHz bandwidth when loaded with a 1 nF input capacitance (26.5 pA<sub>rms</sub> with open input) while consuming only 3.7  $\mu$ W since the AFE power was optimized to only resolve the small redox current.

The remainder of this paper is organized as follows: Section II describes the system architecture, and Section III covers the circuit implementation. Section IV reports electrical and *in-vitro* measurement results, followed by concluding remarks in Section V.

## II. SYSTEM ARCHITECTURE

The key concept in this work is the combination of a pseudo-differential sensing scheme and a CM rejection circuit at the AFE input such that a significant portion of  $I_{BG}$  is eliminated. As a result, the front-end's DR can be reduced, thus decreasing the system power. Fig. 2 shows the FSCV architecture, which measures the current from two carbon-fiber microelectrodes (CFM) and a shared Ag/AgCl reference electrode (RE). The double-layer capacitance,  $C_{dl}$ , given by the Helmholtz model, is

$$C_{dl} = \frac{\epsilon_0 \epsilon_r A}{t} \quad (1)$$

where  $\epsilon_0$  and  $\epsilon_r$  are the free space permittivity and the electrolyte's relative permittivity, respectively,  $A$  is the electrode's surface area, and  $t$  is the Helmholtz double-layer thickness in

CSF [23], [24]. According to (1), CFMs with similar physical properties (*e.g.*, material, dimension) in the same electrolyte have similar capacitances. For a CFM with a  $\mu\text{m}$  diameter,  $C_{\text{dl}}$  is  $\sim 1$  nF, which is much larger than the capacitance from electrode interconnects ( $< 10$  pF) and AFE input ( $\sim$  pF). The large capacitance at the AFE input makes designing an FSCV front-end challenging, specifically the DR, frequency response, and noise performance.

From an architectural perspective, existing FSCV AFEs can be categorized by their domain of operation. In voltage-mode AFEs [27], [33], the input current is converted into a voltage followed by a voltage-mode quantizer. The transimpedance elements are sized proportionally to the DR, often in a large array when the input signal spans many orders of magnitude. Whereas current-mode AFEs, for example, a current-mode  $\Delta\Sigma$  ( $I-\Delta\Sigma$ ), directly quantize current signals without area and power consumed by an extra transimpedance stage [26], [28], [35]. However, the modulator cannot be directly connected to the electrode since the  $1.4 V_{\text{pp}}$  FSCV waveform introduces a large voltage excursion on the DAC, compromising the linearity. This work uses a current-mode architecture for a compact design and high current efficiency while isolating the ADC from the FSCV waveform to prevent linearity degradation seen in prior work [25], [26].

In an FSCV measurement, the WE is swept across a voltage range to observe the two-electron redox reaction between dopamine and its oxidized form, dopamine-ortho-quinone. The oxidization and reduction potentials for dopamine are 0.7 and  $-0.1$  V, respectively [1]. Due to CSF's high conductivity and the small currents in FSCV, a two-electrode setup with no counter electrode (CE) was chosen over a potentiostat [20]. The WEs are swept from  $-0.4$  to  $1.0$  V relative to the RE at  $300$  V/s with a  $10$  Hz interval, resulting in a  $9.3$  ms scan time. To ensure sufficient headroom, a  $3.3$  V supply was used for the AFE, while a  $1.8$  V supply was used for the ADC for better energy efficiency. The Ag/AgCl RE is biased at the AFE CM voltage ( $V_{\text{CM}}$ ),  $1.65$  V. To center the  $V_{\text{CM}}$  of the AFE and ADC, the ADC ground is biased at  $0.75$  V requiring that all NMOS transistors in the ADC are in a deep N-well such that they are isolated from the substrate. Using a  $1.8$ -V supply for the ADC more than doubles the energy efficiency; however, such a dual-supply scheme complicates the supply generation, possibly reducing the benefit of doing so when fully integrated.

As shown in Fig. 2, the large  $I_{\text{BG}}$  resulting from charging and discharging  $C_{\text{dl}}$  is a CM input to the front-end and absorbed by a class-AB CMR circuit. The push-pull nature helps handle large bidirectional CM signals with a quiescent current that is a small fraction of the peak current. This allows the AFE to have low average power. The FSCV voltage waveform modulates the positive terminal of the CMR circuit, which drives both WEs at the negative terminals to the desired scan voltage through negative feedback.

The CMR circuit absorbs half of the signal due to the pseudo-differential configuration. The  $I_{\text{redox}}$  and residue  $I_{\text{BG}}$  from mismatch enter the RCC serving as a current buffer before the ADC. Dynamic element matching (DEM) was implemented to remove flicker ( $1/f$ ) noise and mismatch from the current mirrors. A

current gain of  $3\times$  was chosen to balance the noise and ADC DR. Unlike other CC variants [39], the RCC is fully-differential with the quiescent current,  $I_{\text{Q}}$ , set by a translinear input stage, which also operates in class-AB and has a well-defined  $R_{\text{in}}$ . An  $I_{\text{Q}}$  of  $50$  nA was budgeted to be  $2.5\times$  more than the current needed to support a maximum dopamine concentration of  $1$   $\mu\text{M}$ . This allows the AFE to tolerate a  $\sim 10\%$  mismatch in  $C_{\text{dl}}$  when swept at  $300$  V/s. For a typical nF value of  $C_{\text{dl}}$ ,  $R_{\text{in}}$  needs to be less than  $30$  k $\Omega$  for the noise concern described above, which is difficult to achieve with an open-loop CC structure whose  $R_{\text{in}}$  is  $\sim 1/g_{\text{m}}$  and on the order of a few hundred k $\Omega$ . Therefore, amplifiers were used to cascode-regulate the CC to further reduce its input impedance for low input-referred noise in the presence of large  $C_{\text{dl}}$ .

The physiological range of dopamine means  $I_{\text{redox}}$  can span up to  $60$  dB. To not have the ADC limit the DR, a  $12$ -bit  $1^{\text{st}}$ -order  $I-\Delta\Sigma$  digitizes the RCC output current at a moderate oversampling ratio (OSR) of  $128$ . Compared to a conventional  $1$ -bit modulator, this work utilizes an IIR filter after the comparator to realize multi-bit quantization for improved resolution at a low power and area overhead. A single-bit R-DAC is used for low noise and inherently linear tri-level feedback. In addition, the OTA output is assisted with a replica of both the input (simply with an extra mirror branch in CC) and feedback signals such that it can be low power while achieving  $>70$  dB linearity.

### III. CIRCUIT IMPLEMENTATION

#### A. Class-AB Common-Mode Rejection (CMR) Circuit

The CMR circuit shown in Fig. 3 is implemented by a two-stage differential-difference amplifier (DDA) with two input pairs and a class-AB output stage. The structure is connected in unity-gain feedback such that it acts similar to current-mode common-mode feedback (CMFB) with bipolar current driving capability [40]. The CMR circuit operation can be described as follows. During a measurement, the  $1.4 V_{\text{pp}}$  FSCV waveform,  $V_{\text{FSCV}}$ , directly modulates the positive terminals of the DDA, which drives the WEs to the same voltage through negative feedback. When both  $V_{\text{I1}}$  and  $V_{\text{I2}}$  are equal to  $V_{\text{FSCV}}$ , the DDA is in equilibrium and drives zero current from the outputs,  $V_{\text{O1}}$  and  $V_{\text{O2}}$ . Now suppose both  $V_{\text{I1}}$  and  $V_{\text{I2}}$  are momentarily larger than  $V_{\text{FSCV}}$  with the drains of  $M_1/M_4$  and  $M_2/M_3$  shorted, the DDA input pairs inject more current to the drain of  $M_{10}$  than  $M_9$ , raising  $V_{\text{N}}$ , causing  $M_{13}$  to sink more current (than  $M_{14}$  sources) and pulls down  $V_{\text{I1}}$  and  $V_{\text{I2}}$  until they match  $V_{\text{FSCV}}$ . When the DDA is in equilibrium,  $M_{13}$  and  $M_{14}$  each carry a  $50$ -nA quiescent current,  $I_{\text{Q}}$ . If  $V_{\text{I1}}$  and  $V_{\text{I2}}$  are significantly larger than  $V_{\text{FSCV}}$ ,  $V_{\text{N}}$  increases and turns off  $M_8$  (more). This causes  $M_{12}$  to source less current and  $V_{\text{P}}$  to go up, turning off  $M_{14}$  further while  $M_{13}$  is sinking more current. This push-pull operation allows the bi-directional current driving capability of more than  $6\times I_{\text{Q}}$ .

All transistors in the CMR circuit are I/O devices operating in subthreshold with  $V_{\text{DSAT}} \approx 100$  mV and remain in saturation even with large CM voltage variation. The DDA input pairs,  $M_1-M_4$ , were sized to have a large aspect ratio with a  $g_{\text{m}}/I_{\text{D}}$  of  $22$  S/A. Two floating current sources,  $M_5/M_6$  and  $M_7/M_8$ ,

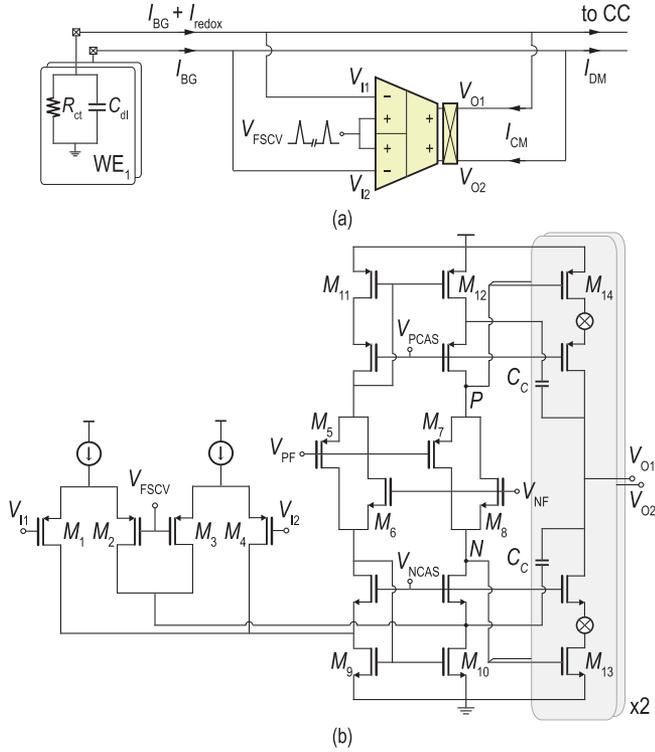


Fig. 3. (a) Block diagram of the class-AB CMR circuit and (b) schematic.

each carry 250 nA such that a total of 300 nA flows through  $M_9$  and  $M_{10}$ . Simulation showed that a large current in the cascode stage is necessary for fast settling during an FSCV scan cycle. The floating current sources bias the cascode stage precisely and allow  $V_N$  and  $V_P$  to swing near the supplies. As a result, the class-AB output stage can sink or source the current necessary to maintain the correct voltages on both terminals. The simulated dc loop gain was 105 dB with a unity-gain bandwidth of 8.2 kHz, which is accurate and fast enough to settle a 1.4 V<sub>pp</sub> FSCV triangular waveform.

Since the CMR circuit is connected in unity-gain feedback, its current noise is directly referred to the input. With the folded DDA stage shared between the two output stages,  $M_1 - M_{12}$  contribute only CM noise. Chopping ( $f_{\text{chop}} = 100$  kHz) removes the amplifier's  $1/f$  noise and offset. After chopping, the CMR input-referred current noise was reduced from 86 to 17.36 pA<sub>RMS</sub> in simulation. In practice, input imbalance (electrode impedance, transistor mismatch, etc.) will lead to imperfect CM noise cancellation from the CMR amplifier. With a 10% electrode and CMR amplifier mismatch, the input-referred noise increased by 15% in Monte-Carlo simulations.

Stability is another design concern, especially when interfaced with a large reactive load. Cascode compensation was chosen over Miller compensation because the former offers a faster transient response (from having a smaller  $C_C$ ) and does not introduce a right-half-plane zero [41]. As shown in Fig. 3, a 4.5 pF capacitor is connected from  $V_{O1}$  to the drain of  $M_{10}$  (and another to  $M_{12}$ ), an internal low impedance node, resulting in an 80° phase margin at  $C_{dl} = 1$  nF.

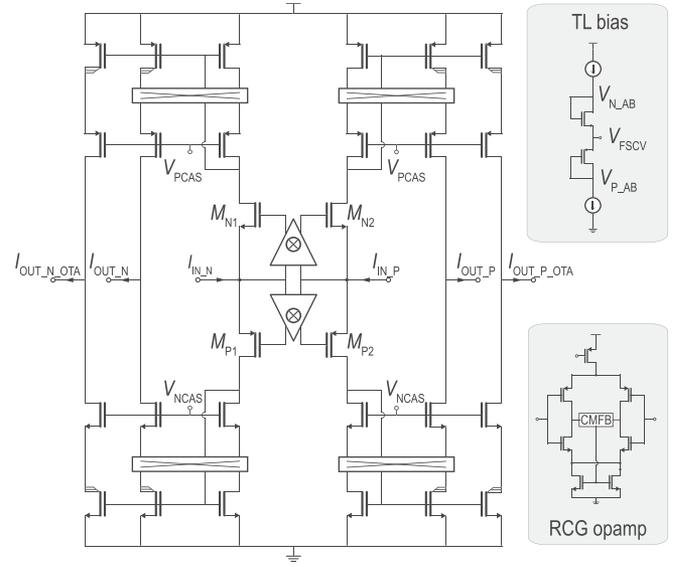


Fig. 4. Schematic of the class-AB RCC.

### B. Fully-Differential Regulated Current Conveyor (RCC)

The RCC isolates the ADC from the electrodes preventing the large CM excursion from deteriorating the ADC linearity while also providing a low input impedance for noise purposes. Fig. 4 shows the implementation of the RCC, which stems from a classic second-generation current conveyor (CCII) biased by a translinear (TL) stage for class-AB operation [42]. The TL principle ensures accurate voltage tracking from node  $X$  to  $Y$  while defining a PVT-insensitive 50 nA  $I_Q$  flowing through transistors  $M_{N1,2}$  and  $M_{P1,2}$ . With a 3.3-V supply, all transistors are in saturation, tolerating up to a 2 V<sub>pp</sub> input with a negligible impact on the linearity.

One issue with the original TL-based CC is that its input impedance is solely determined by the transconductance,  $g_m$ , of the input transistors, which is highly dependent on process variation and  $I_Q$ . The transistors have a small  $g_m$  for a low power design, resulting in a large input impedance. For example,  $R_{in} \approx 500$  k $\Omega$  at  $I_Q = 50$  nA, placing the noise zero from  $sR_{in}C_{dl}$  at 320 Hz, well below the targeted 5 kHz bandwidth, thus significantly increasing the input-referred noise. To address this, a regulated common-gate (RCG) structure was integrated within the TL loop with a high-gain opamp actively driving the gates of the input transistors,  $M_{N1,2}$  and  $M_{P1,2}$ , reducing  $R_{in}$  by the opamp's open-loop gain,  $A_{reg}$ . The opamp was designed with a complementary, current-reuse structure for high current efficiency. The opamp has a 41-dB dc gain and 13-MHz unity-gain bandwidth in simulation. The regulated TL operation can be intuitively understood as follows: when an influx of current tries to raise the input voltage, the opamps steer the gates of  $M_{N1,2}$  and  $M_{P1,2}$  in the opposite direction. This simultaneously reduces and increases the current through  $M_{N1,2}$  and  $M_{P1,2}$ , respectively, counterbalancing the input voltage while maintaining the class-AB operation of the TL loop. The loop was simulated

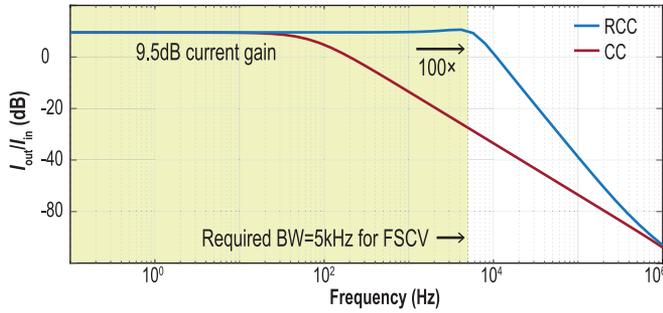


Fig. 5. Simulated bandwidth improvement from the RCC.

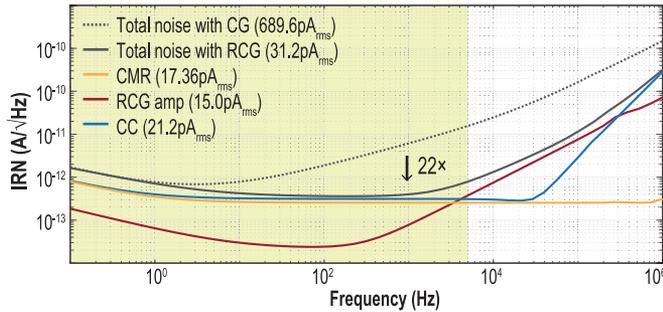


Fig. 6. Simulated input-referred noise of the CMR and RCC.

and had more than  $70^\circ$  phase margin across the  $1.4 V_{pp}$  input range.

Fig. 5 shows the simulated bandwidth improvement from the RCC, with an  $R_{in}$  of  $\sim 4.5 k\Omega$ . The dc operating point of  $M_{N1,2}$  and  $M_{P1,2}$  is maintained by setting the opamp output CM voltage to  $V_{N-AB}$  and  $V_{P-AB}$ , the original bias voltage defined by the TL stage. Fig. 6 shows the simulated noise contribution from the combined CMR and RCC blocks. If the PMOS and NMOS input transistors have equal  $g_m$ , then the total input-referred current noise, including the CMR stage, can be written as

$$\begin{aligned} \overline{i_{n,rms}^2} &= 2q(I_{CMR} + I_{CC}) \left(1 + s \frac{1}{2A_{reg}g_m} C_{dl}\right)^2 \\ &+ \overline{v_{n,op}^2} \left(\frac{1 + sR_{ct}C_{dl}}{R_{ct}}\right)^2, \end{aligned} \quad (2)$$

where  $q$  is the electron charge,  $I_{CMR}$  and  $I_{CC}$  are the bias currents of the CMR and CC, respectively,  $\overline{v_{n,op}^2}$  is the input-referred noise voltage of the opamp, and  $R_{ct}$  is the electrode's charge transfer resistance, which is  $>100 M\Omega$  for CFMs. The first term in (2) is the shot noise of the CMR and CC, whereas the second term is the opamp noise reflected into a current by the input impedance (*i.e.*,  $R_{ct} \parallel 1/sC_{dl}$ ). For the opamp to contribute negligibly to the overall noise, it was designed to have a  $40\text{-nV}/\sqrt{\text{Hz}}$  noise floor for a noise efficiency factor (NEF) of 2.4. DEM reduces the  $1/f$  noise and mismatch from the 1:3 current mirror. The total input-referred noise current with  $C_{dl} = 1 \text{ nF}$  was reduced from 689.6 to 31.2  $\text{pA}_{rms}$  with DEM in simulation. The dominant inband noise is the shot noise from

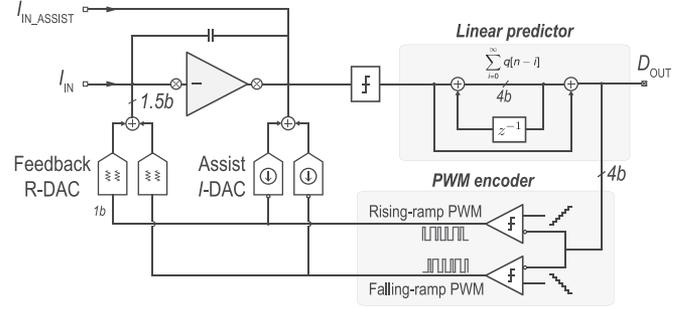


Fig. 7. Block diagram of the current-mode IIR- $\Delta\Sigma$ .

the CMR circuit, while the opamp dominates the high-frequency noise.

### C. Energy-Efficient IIR- $\Delta\Sigma$

It was shown in [37] that modifying a 1<sup>st</sup>-order 1-bit  $\Delta\Sigma$  with an IIR predictor and tri-level pulse width modulated (PWM) DAC can realize the equivalent performance of a multi-bit  $\Delta\Sigma$  in an area- and power-efficient manner. As shown in Fig. 7, the IIR filter can be implemented as a delay-free, discrete-time integrator and a unity-gain feedforward path from the 1-bit quantizer output,  $q$ , to the modulator output,  $d$ . It was also shown that  $d[n]$  could be derived from the cumulative sum of all  $q[n]$ , *i.e.*,  $d[n] = q[n] + \sum_{i=1}^n q[i]$ . Therefore, the IIR predictor can be simply realized with a digital accumulator and adder [37]. The same digital implementation was used in this work, and  $d$  has a 4-bit resolution.

A multi-bit DAC is needed to close the loop, and it must be as linear as the modulator. Taking advantage of a 1<sup>st</sup>-order continuous-time  $\Delta\Sigma$  being insensitive to the shape of the feedback waveform,  $d$  is encoded in time by modulating the pulse width of a single DAC unit. In [38], where the noise was critical, the tri-level feedback DAC was modulated by a tri-level control sequence (0 and  $\pm 1$ ) such that the “0” state shunts away DAC noise for smaller inputs. But without mismatch shaping, the intrinsic DAC linearity was not preserved across codes, as shown in Fig. 8(a). This work solves this problem by splitting the tri-level DAC into two 1-bit DACs and summing the currents at the modulator's virtual ground to improve linearity without using a multi-bit current source. As shown in Fig. 8(b), each split DAC is controlled by a 1-bit PWM signal with complementary phases such that the sum of the two pulses is a return-to-zero (RZ) waveform symmetric around the mid-point in each sample period. By not having a discrete “0” feedback level, the resulting tri-level DAC is linear by averaging the mismatch across codes, similar to a tri-level DAC with rotational DEM [43].

A resistive DAC (R-DAC) was used for lower thermal noise than a current-steering DAC. The impact of reduced loop-gain due to the DAC impedance was negligible with OTA assistance, where a DAC current replica,  $I\text{-DAC}_a$ , is injected directly at the OTA output, effectively bypassing the OTA from processing the DAC signals, therefore improving the linearity [44], as shown in Fig. 7. Since the nonlinearity, noise, and mismatch

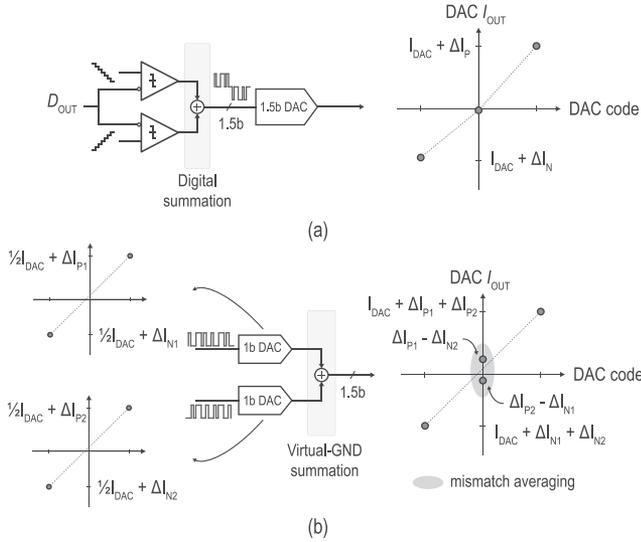


Fig. 8. Block diagram and linearity of (a) non-linear tri-level feedback DAC and (b) linearized tri-level feedback DAC.

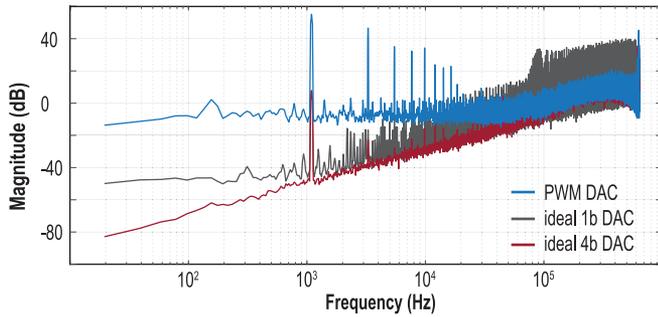


Fig. 9. Comparison of the harmonic content from PWM DAC and an ideal 1b/4b DAC at the virtual ground of the IIR- $\Delta\Sigma$ .

of the assistance DAC are suppressed when input-referred, an  $I$ -DAC was used to provide minimum loading at the OTA output. Shunting also improves the OTA tolerance to increased harmonic content at the virtual ground due to the PWM DAC compared to its single-bit and multi-bit counterparts, as shown in Fig. 9.

The OTA was implemented with high energy efficiency ( $NEF = 1.7$ ) by a two-stage current-reuse amplifier, as shown in Fig. 10. The first-stage was designed with a low quiescent current of 200 nA and long-channel ( $L = 1 \mu\text{m}$ ) input devices with a 40 dB gain and a dominant pole at  $\sim 20$  kHz. The second stage provides an additional 20 dB of gain. The feedforward transconductance stage,  $g_{m3}$ , adds a left-half-plane zero controlled by the ratio of  $g_{m2}$  and  $g_{mf}$  (1:2) and cancels the non-dominant pole contributed by the 2<sup>nd</sup> stage. Feedforward compensation was chosen to avoid energy consumed by charging/discharging the compensation capacitor,  $C_C$ , and the extra branch needed for Miller compensation [44]. In extracted simulations, the two-stage OTA has a 64 dB dc gain and a 54 MHz unity-gain bandwidth. The OTA stability was verified with a 200-point Monte Carlo simulation and had a mean phase margin of  $72^\circ$  ( $\sigma = 1.4^\circ$ ). As shown in Fig. 11, transient noise simulation shows

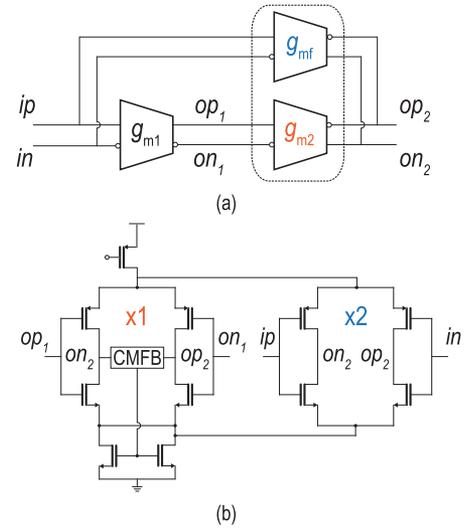


Fig. 10. (a) Block diagram and (b) schematic of feed-forward inverter-based OTA.

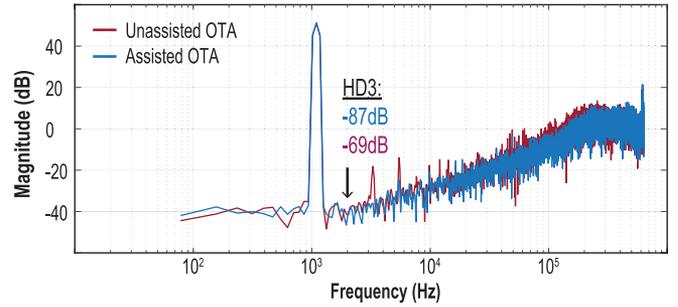


Fig. 11. Simulated spectra of IIR- $\Delta\Sigma$  with OTA-assistance for a  $-2$  dBFS input.

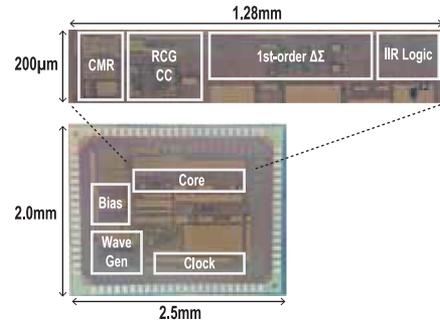


Fig. 12. Die micrograph.

that the ADC's peak SNDR with the assisted-OTA is 72.1 dB, which is  $>5$  dB better than the unassisted case and  $>11$  dB more than the IIR-disabled case.

#### IV. MEASUREMENT RESULTS

The reported FSCV front-end was fabricated in a 180 nm CMOS process with the digital IIR filter and tri-level PWM logic synthesized on-chip. As shown in Fig. 12, the AFE and

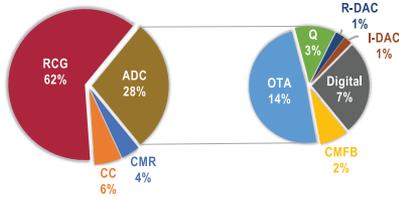


Fig. 13. Measured power breakdown.

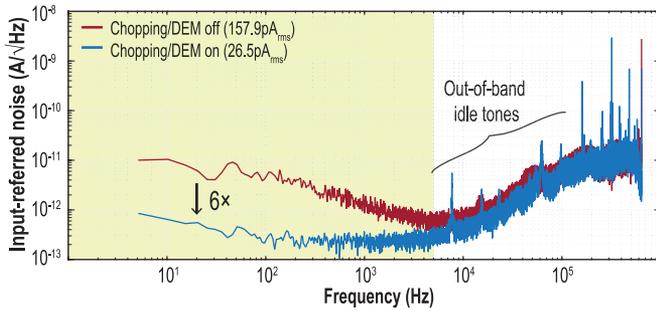


Fig. 14. Measured input-referred current noise PSD (open input).

ADC have an active area of  $1.28 \times 0.2 \text{ mm}^2$ . The AFE was implemented with thick-oxide (3.3 V) devices to tolerate a 1.4 V<sub>pp</sub> FSCV waveform, whereas the ADC and digital back-end used 1.8 V core devices. The ADC and synthesized logic were placed inside a deep n-well with an elevated ground voltage of 0.75 V to center the AFE output and ADC input CM voltage at 1.65 V. With a deep n-well, substrate coupling between the digital and analog circuits is minimized. Electrical and *in-vitro* measurements were performed with the device enclosed in a dark faradic cage to suppress 60 Hz interference and photodiode leakage currents.

#### A. Electrical Characterization

The measured static power consumption of the FSCV front-end is 35.25  $\mu\text{W}$ , among which the AFE and ADC consume 24.8  $\mu\text{W}$  and 10.44  $\mu\text{W}$ , respectively. When averaged over a 10-Hz FSCV cycle (9.3 ms active), the average active power consumption is 3.74  $\mu\text{W}$ . The power breakdown is shown in Fig. 13. Unless stated otherwise, all measurements were taken with  $f_s = 1.28 \text{ MHz}$  for an OSR of 128, which is sufficiently large for the IIR filter not to affect the modulator's STF and NTF [38]. The integrated input-referred noise (IRN) current measured with open inputs was 26.5 pA<sub>rms</sub> in a 5 kHz bandwidth, as shown in Fig. 14, demonstrating that chopping reduces the IRN by more than 6 $\times$ . For sensitive current sensing, capacitive loading at the AFE input introduces a noise zero, amplifying the current noise and limiting resolution. The CFM electrode's double-layer capacitance in  $1 \times \text{HEPES}$  is  $\sim 1 \text{ nF}$ . Due to the relatively low input impedance, this capacitive loading increases the input-referred current noise from 26.5 to 39.2 pA<sub>rms</sub> in a 5 kHz bandwidth. Fig. 15 shows the measured IRN at four discrete input loading conditions (100, 250, 500, and 1000 pF).

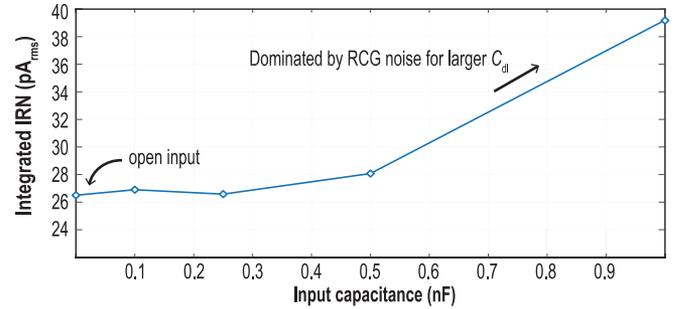


Fig. 15. Measured input-referred current noise vs. input capacitance.

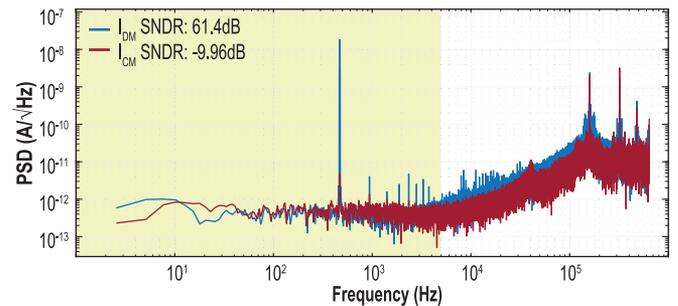


Fig. 16. Measured spectra with a -2 dBFS differential-mode (DM) and common-mode (CM) input.

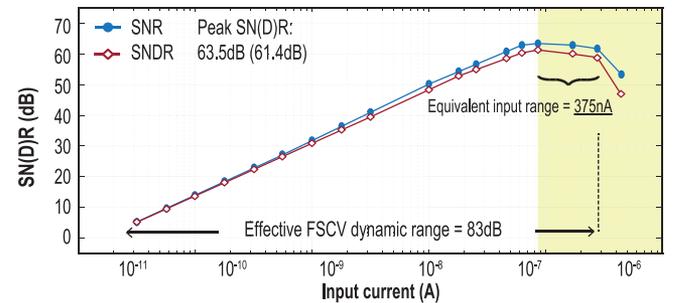


Fig. 17. Measured dynamic range vs. input current.

For ac measurements, a sinusoidal input current was generated by connecting a low-distortion function generator (SRS DS360) in series with a large resistor for  $V$ -to- $I$  conversion. The resistor introduces a negligible current noise while significantly attenuating the instrument's voltage noise. The series resistance and the AFE's input capacitance also low-pass filter the instrument noise. With a 100 M $\Omega$  input resistance, the IRN is comparable to the floating input configuration. Fig. 16 shows measured spectra from the front-end with a -2 dBFS sinusoidal differential-mode (DM) and CM input at 469 Hz. The peak SNDR measured in DM and CM are 61.4 and -9.98 dB, respectively, thus achieving a common-mode rejection ratio (CMRR) of 71.4 dB. The measured spurious-free dynamic range (SFDR) is 71.8 dB. Fig. 17 shows the measured SNDR versus the input amplitude where a 300 Hz CM signal was superimposed on the maximum DM

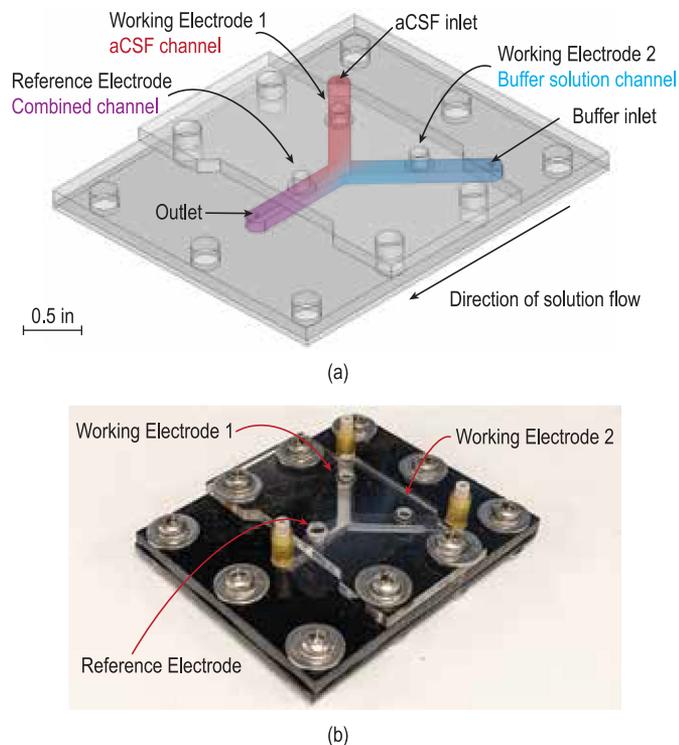


Fig. 18. Flow cell (a) rendering and (b) photograph.

signal, and no SNDR degradation was observed up to 290 nA<sub>pp</sub>, effectively extending the DR from 70 to 83 dB.

### B. In-vitro Measurements

Electrochemical measurements were performed with CFMs (BASi, MF-2007) in a custom fabricated Y-channel flow cell, as shown in Fig. 18. The flow cell is composed of two milled acrylic plates bolted together. A rubber gasket between the plates creates a seal and prevents leaks. The channels are 4 mm wide to accommodate the CFM and Ag/AgCl electrodes. Rubber o-rings were placed around the electrodes to create a seal. The Y-channel design was specifically chosen to isolate the two working electrodes from each other while still being electrically referenced to the same reference electrode. An Ag/AgCl reference electrode was used in an artificial CSF solution composed of 140 mM NaCl, 5 mM KCl, 2.5 mM CaCl<sub>2</sub>, 1 mM MgCl<sub>2</sub>, and 10 mM HEPES (pH 7.4) [27]. A dopamine and buffer mixture was pumped through one inlet, while buffer solution was pumped through the other so that each WE was submerged in either background solution or analyte. The two solutions were combined at the output to flow past the RE, linking the two WEs to the same reference while keeping each working electrode separate. The solution was pumped in at 2 mL/min using LabSmith valves and a syringe pump. The tubing lengths were matched so that both solutions would reach the flow cell and thus each WE simultaneously. LabSmith valves were used to switch analyte or buffer into the analyte side of the flow cell. Continuously moving the solutions through the flow cell allowed for the exposure of both WEs to their corresponding solutions.

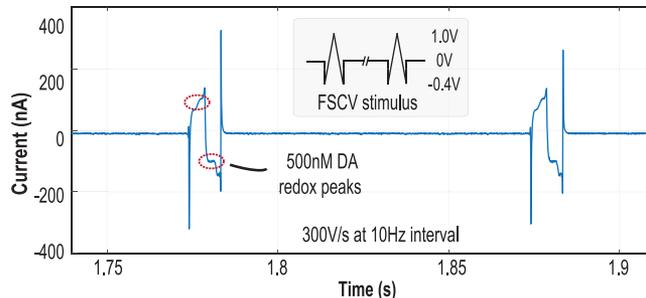


Fig. 19. *in-vitro* FSCV measurement results with 500 nM dopamine.

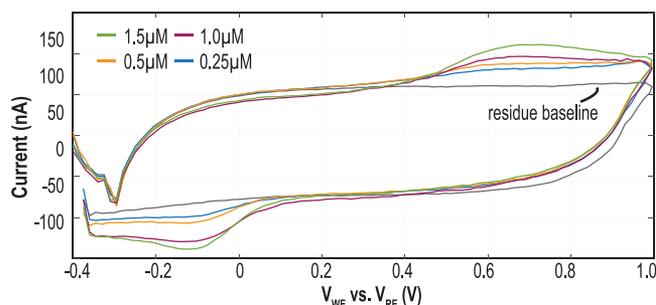


Fig. 20. Reconstructed FSCV waveforms at various dopamine concentrations without background subtraction.

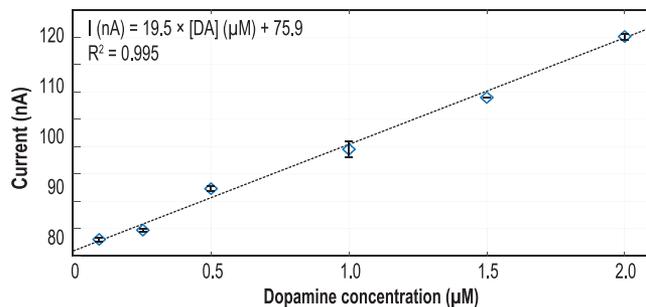


Fig. 21. Measured dopamine sensitivity curve.

Due to the laminar flow, there is little to no mixing once the flows are combined and no backflow.

A 300 V/s triangular waveform was generated using a Keysight Trueform 33622A waveform generator. The waveform spanned from  $-0.4$  to  $1$  V and was pulsed at 10 Hz. Dopamine and buffer solutions were pumped through the flow cell for 30 seconds, over which voltammograms were recorded. Fig. 19 shows a real-time recording of 500 nM dopamine without post-processing. Redox peaks were visible even in the raw recording due to the low-noise front-end with CM rejection. Dopamine measurements were taken at 100, 250, 500, 750, and 1000 nM to characterize the response. Post-processing averaged 20 scans and reconstructed the voltammograms, as shown in Fig. 20. The peak current versus concentration is shown in the calibration curve in Fig. 21, where the error bars were calculated from 20 consecutive scans. The measured sensitivity was 19.5 nA/ $\mu$ M.

TABLE I  
COMPARISON TO PRIOR FSCV AFES

	[36] Nasri TBCAS'17	[35] Zamani MWCAS'20	[34] Lu TBCAS'21	[27] Dorta TBCAS'16	[26] Bozorgzadeh TBCAS'16	[25] Bozorgzadeh JSSC'14	<b>This work</b>
Process (nm)	65	180	180	65	350	350	180
Topology	Dual slope	1 <sup>st</sup> -ord. $\Delta\Sigma$	I-to-F + TDC	TIA + SAR	3 <sup>rd</sup> -ord. $\Delta\Sigma$	3 <sup>rd</sup> -ord. $\Delta\Sigma$	CC + 1 <sup>st</sup> -ord. IIR- $\Delta\Sigma$
Scan rate (V/s)	400	400	0.008 - 400	300	400	400	300
Sample freq. (Hz)	5k	1.6M	50k	10k	625k	625k	1.28M
Bandwidth (Hz)	2.5k	5k	25k	2k	4.88k	5k	5k
Background cancellation	Constant offset subtraction	Two-step cyclic	-	Two-step cyclic	On-chip DSP	-	Class AB CMR
Input range (nA)	165	1000	10000	430	900	950	375
CMRR (dB)	-	-	-	-	-	-	71.4
Sensitivity (nA/ $\mu$ M)	10	35.9	-	8.6	23.3	52.2	19.5
Avg. power* ( $\mu$ W)	3.1	14.1	1.77	14.4	9.5	9.3	3.7
Resolution (pA <sub>rms</sub> )	125.2 <sup>†</sup>	710 <sup>†</sup>	25000	92 <sup>†</sup>	68.2 <sup>†</sup>	55 <sup>†</sup>	26.5 (open) 39.2 (1 nF)
FoM** (pA <sup>2</sup> $\mu$ J)	19.4	1422	425000	60.9	9.05	5.6	0.52

\*Average power during 10 Hz scan.

\*\*FoM=resolution<sup>2</sup>×energy/conversion.

<sup>†</sup>Input loading not explicitly stated.

Table I compares this work to the state-of-the-art FSCV front-ends. This work achieves the lowest input-referred current noise (26.5 pA<sub>rms</sub>) with an open input due to the low input impedance input structure. Even with 1 nF of input capacitance, this work achieves excellent noise performance at 39.2 pA<sub>rms</sub>. The resolution-to-power tradeoff is captured by the resolution-FoM, which is widely used to characterize the power efficiency of sensor front-ends [45]–[47]. This work achieves an FoM of 0.52 pA<sup>2</sup> $\mu$ J, which is >10× better than the state-of-the-art.

## V. CONCLUSION

This paper presents an FSCV front-end that achieves 26.5 pA sensitivity while consuming an average power of 3.74  $\mu$ W and an active area of 0.256 mm<sup>2</sup>. A differential sensing scheme and analog background subtraction were proposed to effectively extend the DR by canceling a large portion of the non-faradaic current before it sees the front end. A 1<sup>st</sup>-order IIR- $\Delta\Sigma$  quantizes the dopamine signal with a digital IIR filter, turning single-bit quantization into multi-bit feedback to improve resolution at negligible power overhead. An inherently linear tri-level PWM DAC closes the loop while preserving a single-bit design complexity. The resulting architecture is a compact, low-power FSCV AFE used to measure dopamine at physiological levels with a sensitivity of 19.5 nA/ $\mu$ M.

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