A 22.3-nW, 4.55 cm^2 Temperature-Robust Wake-Up Receiver Achieving a Sensitivity of −69.5 dBm at 9 GHz

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***Abstract*— This article presents a miniaturized wake-up receiver (WuRX) that is temperature-compensated yet still consumes only 22.3 nW (7.3 nW excluding the temperature-compensation blocks) while operating at 9 GHz (*X*-band). By moving the carrier frequency to 9 GHz and designing a high impedance, passive envelope detector (ED), the transformer size is reduced to 0.02 cm^2 while still achieving 13.5 dB of passive RF voltage gain. To further reduce the area, a global common-mode feedback (CMFB) technique is utilized across the ED and baseband (BB) amplifier that eliminates the need for off-chip ac-coupling components. Multiple temperature-compensation techniques are proposed to maintain constant bandwidth of the signal path and constant clock frequency. The WuRX was implemented in 65- (RF) and 180-nm (BB) CMOS and achieves −69.5- and −64-dBm sensitivity with and without an antenna, respectively. Importantly, the sensitivity is demonstrated to vary by only 3 dB from −10 to 40 °C. This article demonstrates state-of-the-art performance for WuRXs operating at >1 GHz while achieving the smallest area and best temperature insensitivity.**

***Index Terms*— Near-zero power, temperature compensation, wake-up receivers (WuRXs), *X*-band.**

I. Introduction

MANY emerging Internet-of-Things (IoT) devices require persistent operation, yet they wirelessly communicate very infrequently in an event-driven manner. Rather than using conventional wake-on radios that require periodic and energy-expensive turn-on synchronization routines (despite there being no data to relay), wake-up receivers (WuRXs) offer a low-power way to continuously monitor the spectrum for pre-specified asynchronous wake-up signatures [1, p. 137], [2]–[6].

Manuscript received July 4, 2019; revised September 26, 2019; accepted October 16, 2019. Date of publication November 4, 2019; date of current version May 27, 2020. This article was approved by Associate Editor Pui-In Mak. This work was supported in part by the Defense Advanced Research Projects Agency (DARPA) under Contract HR0011-15-C-0134 and in part by the DURIP Award from the Office of Naval Research under Award N00014-18-1-2350. *(Corresponding author: Patrick Mercier.)*

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Digital Object Identifier 10.1109/JSSC.2019.2948812

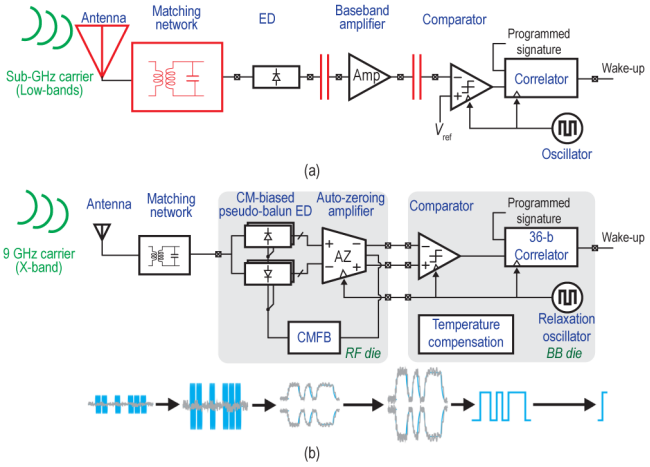


Fig. 1. Block diagram of (a) conventional ac-coupled WuRX and (b) proposed WuRX.

Since a WuRX is always on, its power consumption often dominates the total average power consumption of an IoT device, and therefore, it must be minimized. However, this should not come with a compromise in sensitivity because if the sensitivity of the WuRX is less than that of the "main" radio that is being woken up, achievable network deployment distances will be compromised. Thus, power and sensitivity are the two most important metrics for a WuRX [4]. Recent work has shown that a direct envelope detector (ED)-based receiver architecture with a high passive voltage gain impedance transformer, as shown in Fig. 1(a), can, along with relaxed wake-up latency, yield remarkably high sensitivity at nanowatt power levels. For example, sensitivities of −76 dBm at 7.6 nW [6], −80.5 dBm at 6.1 nW [7], and −79.1 dBm at 0.42 nW [5] have recently been reported.

At such low power levels, the battery volume may not be the limiting factor in overall device miniaturization. Instead, the size of the antenna, transformer, and other off-chip components often dominate, especially in size-conscious applications (*e.g.*, surveillance and tracking). For example, achieving 0.7-dBi peak gain at 433 MHz requires a 50 × 100 mm^2 patch antenna [8], which alone is on the same size as a 1.5-V, 90-mAh printed battery (72 × 60 mm^2) [9]. The area of the impedance matching network (MN) at such frequencies also occupies a significant area (*e.g.*, >6 cm^2 in [7]). To make matters worse, such designs typically ac-couple the ED output

to the baseband (BB) amplifier to ease biasing and thus require either off-chip nF-size capacitors or suffer from ac-coupling distortion due to the low data rate (<1 kb/s) [5], [9], [7].

Since achieving such low power levels typically requires low-voltage and/or subthreshold operation, such designs are usually quite sensitive to temperature variation; even a few degrees of temperature variation can adversely affect the performance of several key blocks, leading to unacceptable sensitivity degradation. Unlike conventional "main" radios, which derive frequency references from temperature-stabilized crystals and can support the power overhead of temperature compensation of RF and analog circuits, it is not straightforward to compensate nanowatt-level WuRXs without significant power overhead.

To minimize area and impart temperature-robust operation without a large compromise in power or sensitivity, this article presents a WuRX operating at *X*-band, as shown in Fig. 1(b). The design utilizes a pseudo-balun passive ED with high input impedance at 9 GHz to facilitate the design of a small microstrip line transformer with 13.5 dB of passive voltage gain at 9 GHz. To eliminate off-chip ac-coupling, a replica ED and autozeroing (AZ) BB amplifier with a global common-mode feedback (CMFB) loop are proposed. Temperature robustness is achieved using temperature-compensation techniques applied to the ED, BB amplifier, and relaxation oscillator to maintain a constant signal bandwidth. The proposed WuRX is implemented in a heterogeneous stack of 65- and 180-nm CMOS directly mounted on a PCB with a custom antenna and microstrip line transformer. The entire design, including the antenna, fits within 4.55 cm^2.

This rest of this article is organized as follows. The system requirements and architecture are presented in Section II. Section III presents the RF design and Section IV describes the BB circuits. Section V presents the temperature-compensation techniques, followed by measurement results in Section VII. Section VIII concludes this article.

II. System Design Considerations

A. Carrier Frequency and Architecture Selection

Recent WuRX work has greatly benefited from the combination of a passive direct ED architecture coupled to a passive impedance transformation network enabling high-voltage gain with zero power [see Fig. 1(a)]. By operating at sub-500 MHz (*e.g.*, 109 MHz in [7] and 434 MHz in [5]), high-voltage gain (>23 dB), and therefore high sensitivity (better than −79 dBm), was achieved. However, the impedance transformer in such designs requires large, off-chip, high-Q inductors for high parallel resistance. For instance, a 1320-nH inductor and a 50-nH inductor were used in the 109- and 434-MHz designs, respectively. More importantly, the area of antennas that efficiently operate at these frequencies can be extremely large, for example, as the nominal size of patch and loop antennas, scales quadratically with the carrier wavelength [11, p. 95]. Thus, the MN and the antenna consume >50 mm^2 in such prior work, preventing use in area-constrained applications.

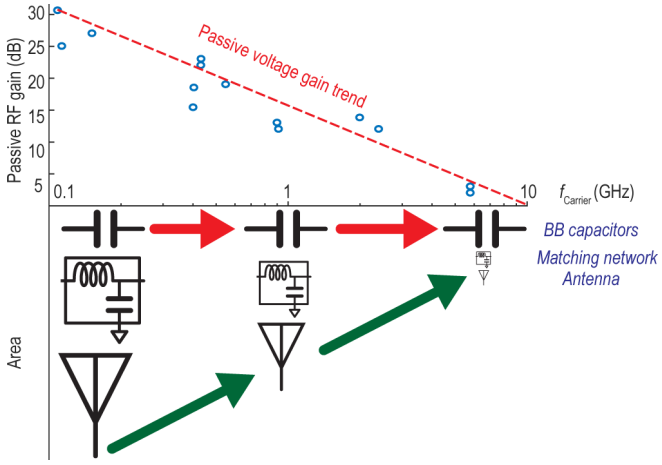


Fig. 2. MN voltage gain and component size versus carrier frequency.

Operating at higher frequencies (*e.g.*, 2.4 GHz) can enable a dramatic area reduction, for example, down to <2 cm^2 in [12], at the expense of reduced sensitivity (−61.5 dBm) due to low antenna and MN gains. Alternatively, ultrasound can also enable miniaturization, but requires custom transducers that are not compatible with existing radios [13], [14]. Furthermore, ultrasound is easily blocked by obstacles and thus only suitable for short-range applications.

To enable miniaturization, this design targets *X*-band operation. Compared to other adjacent bands, such as *C*-, *Ku*-, and *Ka*-bands, the *X*-band (9 GHz) has high link availability and is virtually weatherproof due to the low rate of atmospheric attenuation. Moreover, it is reserved exclusively for government users, and thus there is less interference, which relaxes the requirement on interference rejection [15]. However, any RF active amplification or local oscillator (LO) generation at such frequency would consume several milliwatts—$10^6\times$ larger than the nanowatt target. As such, a direct ED architecture is the only suitable architecture. A passive ED was chosen over an active or self-mixing architecture due to its higher input impedance, higher conversion gain, and $1/f$ noise-free nature. To maximize conversion gain, the pseudo-balun passive ED architecture first described in [7] is employed, with modifications, as discussed in Section IV.

B. RF Circuit Design Challenges

Moving to higher frequency reduces the size of the antenna and MN, as shown in Fig. 2. However, this comes with a tradeoff in the achievable passive gain. According to recent literature, the passive voltage gain scales monotonically with frequency, from 30.6 dB at 109 MHz to 2 and 3 dB at 5.8 GHz [11], [12]. Since the direct-ED WuRX sensitivity is typically limited by the BB noise [18], every dB lost in the MN gain directly reduces the sensitivity. This indicates that simply moving a prior design from 109 MHz to 9 GHz would lose ∼30 dB in sensitivity, which is unacceptable. Thus, the first challenge is to break the trend shown earlier and maintain high passive gain while moving to *X*-band. This requires the co-design of a high-impedance ED and a high-Q MN at 9 GHz to maximize the RF and conversion gain, which will be discussed in Section III-B.

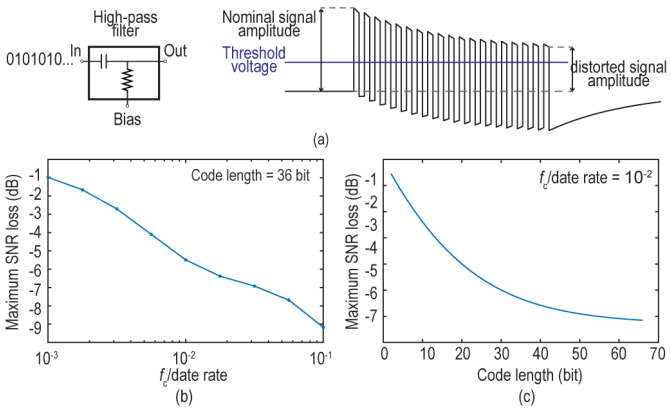


Fig. 3. (a) Simulated waveform output when f_c/data rate is 0.01 and simulated maximum SNR loss versus (b) f_c/data rate and (c) code length.

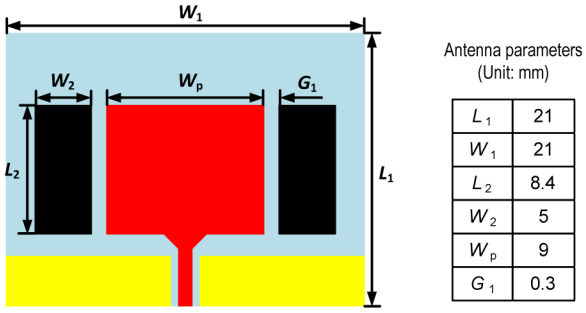


Fig. 4. 9-GHz patch antenna layout.

C. BB Circuit Design Challenges

As described in [7], after fixing the architecture and frequency, the only design parameter that can be traded for sensitivity is latency. With 20-dBm output power from a transmitter, better than −65-dBm sensitivity is required to achieve a reasonable coverage range (∼50 m). To achieve this sensitivity, a low WuRX data rate (33.3 b/s), a low BB bandwidth (33.3 Hz), and a long code sequence (18 bit) are chosen. This results in a latency of 540 ms, which is acceptable in many, though not all, low-average throughput IoT applications.

However, the low data rate and the long code sequence impose a challenge on the conventional ac-coupled BB amplifier [Fig. 1(a)]. Prior work used either nF off-chip capacitors [7] or a 20-pF on-chip capacitor but incurred an SNR penalty [5]. While the RF components (*i.e.* antenna and MN) scale with the carrier frequency, the BB ac-coupling capacitors are unchanged and only implementable with lumped components (see Fig. 2).

Fig. 3(a) shows the effect on the signal distortion due to the ac-coupling. When a signal passes through the high-pass filter, its dc level shifts toward the bias voltage gradually, which manifests as a distortion. Since the comparator threshold voltage is preset to achieve the required false-alarm rate and is constant during the sequence, the signal amplitude with respect to the threshold voltage decreases with each "1" bit. The minimum signal amplitude (*i.e.* the maximum SNR loss) happens at the end of the last "1" bit. This distortion depends on the filter corner frequency f_c and the code (sequence and length). For example, consider the code consisting of repeating "10" for simplicity. The maximum SNR loss is plotted against f_c normalized to the data rate and code length in Fig. 3(b) and (c), respectively. The plots show that the distortion is more serious when lower data rates and longer code sequences are used assuming a fixed f_c. To bound the distortion to less than 1 dB, f_c must be $<0.001\times$ data rate. A similar conclusion has been drawn in [19, p. 183]. Thus, the 33.3-b/s data rate needs $f_c \leq 33.3$ mHz, which is not possible to reasonably implement on-chip.

To address this challenge, dc-coupling should be used between the ED and BB amplifiers. However, this leads to issues around biasing (*i.e.* the preceding stage sets the following stage's operating point) and offset. Section IV proposes an ED-amplifier co-design scheme where a global CMFB, an AZ network, and a replica ED are used to address this collectively.

III. RF Circuit Design

A. Antenna

A patch antenna is a popular choice at high frequency due to its low cost, high gain, and small form factor that is compatible with a PCB design. They also have a relatively narrow bandwidth, which is beneficial for interference resilience, though in some cases, the bandwidth is so narrow that lining up the antenna's frequency with the desired frequency band and the MN can be difficult. To slightly ease this constraint, the proposed design employs a conventional patch antenna next to a pair of parasitic patches, as shown in Fig. 4, which extends the matching bandwidth from 3% to 5%. The main patch is 9×8.4 mm^2 and feeds the following impedance transformer via a grounded coplanar waveguide (GCPW). The simulated antenna gain is 5.5 dB.

B. Transformer and Pseudo-Balun ED Co-Design

Prior sub-gigahertz WuRXs utilize discrete components (inductors and/or MEMS resonators) to implement the MNs due to their high Q (>100). However, these high-Q passives become inaccessible as the carrier frequency increases. This design instead uses distributed components and a bond wire in the arrangement shown in Fig. 5 to form a transformer. The T-shaped inductor network (L_1, L_2, and L_{bond}) is equivalent to a pair of coupled inductors. No additional capacitance is used to avoid extra loss. The ground inductance is carefully modeled by L_{gnd}, as it can significantly affect the performance at 9 GHz. Specifically, L_{gnd} limits the highest operation frequency since it creates a transmission zero at

$$f_{z,\text{gnd}} = \frac{1}{2\pi\sqrt{L_{\text{gnd}}C_{\text{in}}}} \tag{1}$$

where C_{in} is the ED input capacitance. As shown later, C_{in} is estimated to be 115 fF, and thus, $f_{z,\text{gnd}}$ should be >15 GHz so as to not impair the voltage gain at 9 GHz. Thus, L_{gnd}

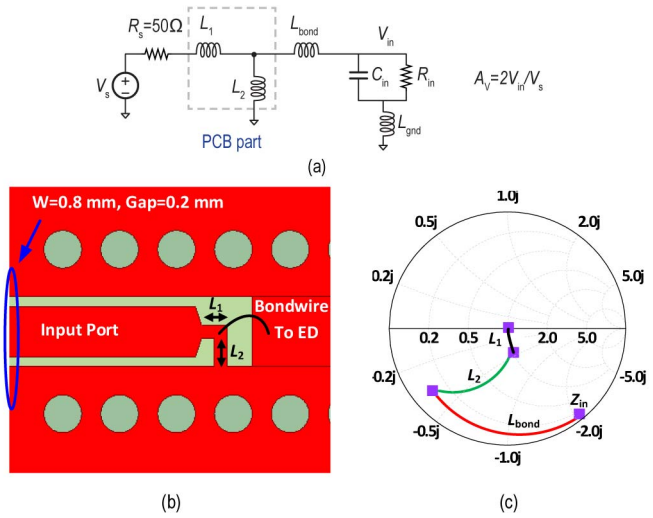


Fig. 5. (a) Schematic of the 9-GHz transformer. (b) Layout of the transformer. (c) Matching procedure.

must be <0.74 nH. Several approaches are utilized to reduce L_{gnd} below this value. First, instead of using microstrip line to connect the transformer, a GCPW is used. Thus, the ground is a continuous plane, which reduces L_{gnd}. Second, four ground pads are down-bonded to the ground paddle beneath the chip to minimize the wirebond inductance, though it should be noted that the mutual inductance limits this technique from further improvement. Third, a thin substrate with a via array is used to connect the top and bottom grounds. Note that there is a tradeoff here as too thin of a substrate results in low Q for the distributed inductors, which reduces the voltage gain. In this article, a 20-mil Rogers 4003C substrate is used to meet both gain and L_{gnd} requirements. These techniques reduce L_{gnd} from 1 to 0.2 nH.

The transformer voltage gain A_V is defined as the ratio between the ED input voltage, V_{in}, and the transformer input voltage and can also be expressed as 2 $\times V_{in}$ over the signal source voltage, V_s, when the transformer is matched to the 50-Ω source impedance [see Fig. 5(a)]. A_V is primarily limited by the effective parallel resistance of the secondary side transformer. To maximize this resistance, a bond wire inductor is used as the second stage since it has the highest Q (∼100) at this frequency. The bond wire length is estimated to be 1.8 mm with an inductance of 1.8 nH. Fig. 5(b) shows the transformer layout. Inductors L_1 (0.3 nH) and L_2 (0.35 nH) are realized by short stubs that directly connect to the input port and top ground, respectively. The high-Q transformer occupies only 0.02 cm^2—300× smaller than prior work [7]. Fig. 5(c) shows the impedance matching contour from the high-impedance ED to the 50-Ω antenna on a Smith chart.

The passive ED is arranged in a pseudo-balun topology to perform single-ended to differential conversion and improve the conversion gain by 2× (1.5-dB sensitivity improvement) compared with a single-ended version for a given input capacitance [7]. Since the ED input capacitance directly affects the transformer performance, it needs to be minimized to maximize both L_{bond} (for maximum A_V) and $f_{z,gnd}$ (to avoid the transmission zero). On the other hand, the ED k factor,

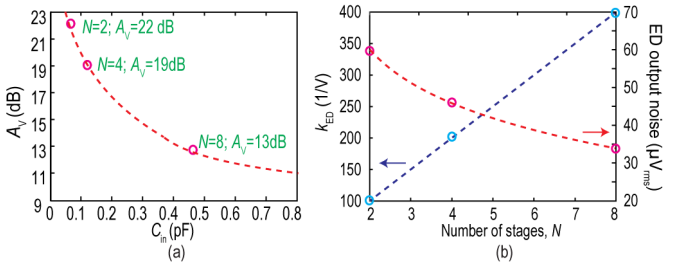


Fig. 6. Simulated (a) transformer gain versus C_{in} and (b) kED and ED noise versus N.

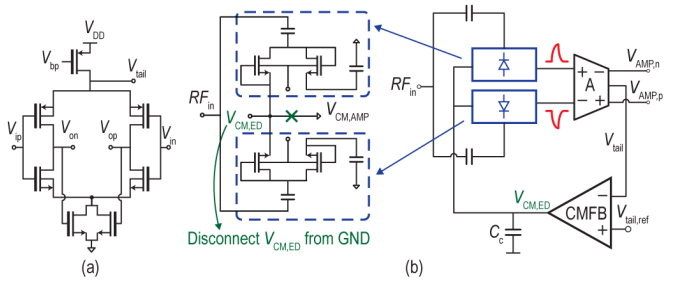


Fig. 7. Proposed (a) core amplifier and (b) CM-biased ED using global CMFB.

which sets its conversion gain for a given input amplitude, is proportional to the number of stages N and therefore proportional to the ED's C_{in}. This imposes a direct tradeoff. In this article, N was chosen to optimize the overall sensitivity by balancing the ED conversion gain, transformer gain (limited by increased capacitance with more stages), and ED noise, as shown in Fig. 6. By applying the SNR-oriented optimization method proposed in [7], the normalized SNR is calculated to be 0.264, 0.353, and 0.235 for $N = 2$, 4, and 8, respectively. Thus, an optimal design with $N = 4$ stages was chosen, resulting in $A_V = 19$ dB and an ED k factor of ∼200 V^{-1}. Compared with prior art operating at 5.8 GHz with an active ED that consumed 25.2 μW [16], the RF front-end and passive ED, in this article, achieves 3-dB better conversion gain with no power consumption and no $1/f$ noise.

IV. Baseband Circuit Design

A. Baseband Amplifier

Due to the lack of sufficient RF amplification prior to demodulation by a passive-gain-based ED-first architecture, sensitivity is not typically determined by RF noise, but rather by BB noise from the ED and BB amplifier [18]. In this article, a BB amplifier with a low (<1 dB) noise figure (NF) is required to maximize the sensitivity. The BB amplifier must also have low input capacitance and high input impedance (>10 GΩ) since the ED output impedance is proportional to its input impedance (>100 MΩ). Fortunately, linearity is generally not an issue in WuRXs that utilize binary modulation [*e.g.*, on-off keying (OOK)].

The core BB amplifier is implemented using a single-stage current-reuse inverter-based amplifier with a local CMFB circuit that sets the NMOS transistor source bias by sensing its output CM voltage [see Fig. 7(a)]. Due to the 2× current

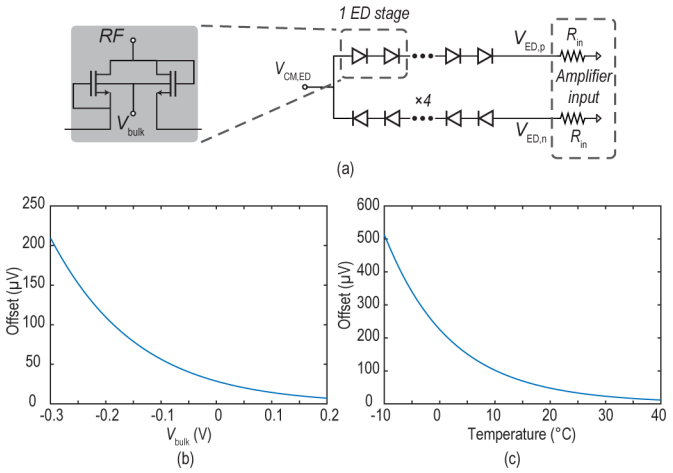


Fig. 8. (a) Circuit model showing the ED offset issue and simulated offset versus (b) ED bulk bias and (c) temperature.

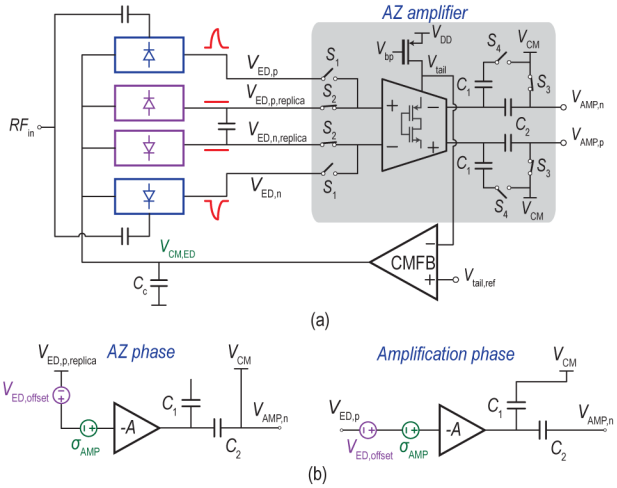


Fig. 9. Schematic of the proposed (a) replica ED and AZ network and (b) half-circuit model during the AZ phase and amplification phase.

reuse, the core amplifier is designed to have a 0.4-dB NF while only consuming 3.2 nW. To remove the ac-coupling capacitors, a global CMFB around the ED is proposed to properly bias the BB amplifier. This is accomplished by driving the CM node of the pseudo-balun ED, $V_{\mathrm{CM,ED}}$, with an auxiliary amplifier. The auxiliary amplifier closes the loop by sensing the tail node voltage from the core amplifier, as shown in Fig. 7(b). Thus, by adjusting $V_{\mathrm{CM,ED}}$, the dc-coupled current-reuse amplifier is biased to the desired operating point and is insensitive to process, voltage, and temperature (PVT) variation.

However, this architecture is sensitive to the dc offsets of the ED and the BB amplifier. Specifically, the pseudo-balun architecture has a systematic offset that can overload the comparator, which would desensitize the WuRX without special design consideration. Fig. 8 shows this issue where the positive branch 8× forward-biased diode-connected NMOS transistors are connected in series with the BB amplifier's input resistance R_{in}. In contrast, the negative branch consists of 8× reverse-biased diodes in series with R_{in}. The forward- and reverse-biased diodes have different channel resistances, which results in a non-zero ED offset voltage between $V_{\mathrm{ED}p}$ and $V_{\mathrm{ED}n}$. Unfortunately, the diode resistance is a function of bulk bias voltage V_{bulk} and temperature, as shown in Fig. 8(b) and (c), respectively. Based on the simulation, the offset voltage varies from 10 to 500 μV, which is significantly larger than the minimum detectable signal at the ED output. Due to the bias voltage and temperature dependence, the offset is difficult to calibrate out. Furthermore, the core BB amplifier can easily yield >1-mV input-referred offset due to device mismatch, even with large transistors (>50 $\mu\mathrm{m}^2$) and careful layout. For these reasons, careful considerations are required to enable robust operation over PVT variation.

B. Autozeroing Network

Rather than degrading the ED input impedance with chopping at the RF input, an output-sampled AZ network and a replica ED architecture are proposed. Fig. 9(a) shows the schematic of the proposed scheme. All the ED bulks are tied together, and the replica ED is matched to the signal path ED through common layout techniques; thus, they should generate the same dc output voltage (*i.e.* $V_{\mathrm{ED}p,n} = V_{\mathrm{ED}p,n,\mathrm{replica}}$). The signal path ED (blue) connects to the RF input via small, on-chip, RF ac-coupling capacitors, whereas the replica ED (purple) does not connect to the RF input. Thus, the only signal content exists at $V_{\mathrm{ED}p,n}$. An on-chip 10-pF capacitor is placed between the outputs of the replica ED to bandlimit the noise without affecting the CM loop stability.

The AZ network shown in Fig. 9 works as follows. During the AZ phase, S_2 and S_3 are closed, whereas S_1 and S_4 are open. The replica ED offset $V_{\mathrm{ED,offset}}$ and the amplifier error σ_{AMP}, specifically $1/f$ noise and offset, are amplified by gain A and sampled on C_2 with respect to the CM voltage V_{CM}. During the amplification phase, S_2 and S_3 are open, whereas S_1 and S_4 are closed. The ED output and offset along with the amplifier error are amplified and sampled onto C_1 ($= C_2$) with respect to V_{CM}. The voltage stored on C_2 is in series and thus subtracted, thereby removing the ED offset, amplifier $1/f$ noise, and amplifier offset. Folding of wideband white noise is a typical drawback of AZ since the amplifier has a bandwidth that is greater than the sampling frequency, f_{s} [20]. There are two noise sources in this design that could potentially fold: the ED and the amplifier noise. The ED noise folding is solved by bandlimiting it to the data rate and employing 2× oversampling. The amplifier noise folding is inevitable since the signal path is on for only half of the period and the amplifier bandwidth needs to be 2× higher than the equivalent continuous-time amplifier. Consequently, a minimum of 2× noise folding is expected. An explicit sampling capacitor C_1 is added to the amplifier output during the amplification phase to limit the noise bandwidth. In the AZ phase, C_1 is floating and does not load the amplifier. With $C_1 = C_2$, the amplifier bandwidth during each phase is the same, both 2× higher than the data rate, and thus the minimum 2× noise folding is achieved. Simulation shows ∼7× lower noise by adding C_1 compared to not having it.

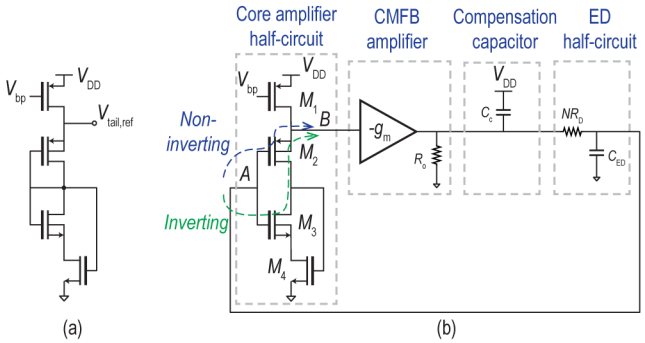


Fig. 10. Schematic of (a) replica bias and (b) CMFB loop.

With the low supply voltage ($V_{DD} = 0.4$ V), the switches in the AZ network require extra attention. The input switches (S_1 and S_2) are driven by a clock booster that generates $2V_{DD}$ to reduce the ON-resistance and thus their noise power spectral density (PSD). On the other hand, the leakage of the output switches is more important, and thus minimum size transistors with the nominal V_{DD} are used. Simulation shows that all switches contribute <3% of the total noise and switch imperfections (*i.e.* charge injection, clock feedthrough, and leakage) having minimal effect on the amplifier performance across mismatch and PVT variation.

The switched-capacitor operation and large input Miller capacitance of the BB amplifier can lead to an unacceptably low input resistance (∼2.4 GΩ) that loads the ED. To solve this, neutralization capacitors are connected between the amplifier input and output, thus canceling the input Miller capacitance. The neutralization capacitors are implemented with half-sized input transistors for matching. Simulation shows that the input resistance increases to 28 GΩ, which is >50× the ED output resistance.

C. Common-Mode Feedback

As a differential, dc-coupled system, the ED and BB amplifiers require a CMFB network to operate correctly. This is accomplished in the proposed design via a global CMFB loop that senses the amplifier tail node V_{tail} (shown in Fig. 7) and compares it with a replica bias circuit, which is implemented the same as the core amplifier, though in this case shorting the input and output and scaling the current by 8× to reduce power consumption [see Fig. 10(a)]. The diode-connected architecture ensures proper operating points with self-bias and adjust $V_{tail,ref}$ dynamically to accommodate PVT variation. This approach, coupled with the AZ network described earlier, makes dc coupling between the ED and BB amplifier possible.

However, there is a potential start-up issue with this global CMFB loop due to the CM input voltage of the inverter-based core amplifier. Since M_2 works as a source follower in the global CMFB during normal operation and the CMFB amplifier provides a 180° phase shift at dc, the loop gain is nominally negative. However, there exists an inverting path via M_3 and M_2, which forms a positive feedback loop. During start-up, node A in Fig. 10(b) stays near ground, while node B is charged to V_{DD} quickly through M_1 and M_2. Thus, M_3 is in sub-threshold saturation and M_2 is in triode. The inverting path can overpower the non-inverting path and prevent the amplifier from starting up successfully. To remedy this, a compensation capacitor C_c is added between V_{CM} and V_{DD}. This serves two purposes—it sets the dominant pole of the CMFB loop and it pulls up node A to V_{DD} during start-up, which drives M_3 into triode and kills the inverting path gain.

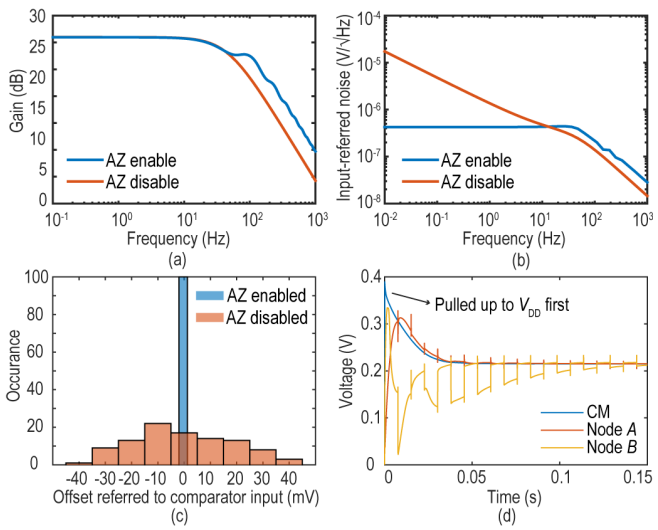


Fig. 11. Simulated BB amplifier (a) gain, (b) noise PSD, and (c) offset. (d) Start-up transient simulation.

Fig. 11 shows the simulated BB amplifier gain. As expected, a sinc-shaped foldover component appears after enabling the AZ [20]. Fortunately, this is not an issue since the ED output is bandlimited to eliminate the noise aliasing. The total input-referred integrated noise drops from 8.1 to 7.2 μV due to the reduced $1/f$ noise [see Fig. 11(b)]. A 100-point Monte Carlo simulation shows that the offset is attenuated by 50× due to the AZ [see Fig. 11(c)]. The residue offset (<500 μV) is due to switch mismatch and amplifier nonlinearity. Finally, Fig. 11(d) shows that the circuit starts up properly after V_{CM} and node A are pulled up to V_{DD}.

D. Comparator, Correlator, and Oscillator

The sampled output of the BB amplifier is digitized by a comparator, which serves as a 1-bit quantizer. A double-tail dynamic comparator with threshold voltage tuning is implemented [4]. Since the comparator noise and threshold voltage are attenuated by the BB amplifier gain when referred to the ED output, its noise and tuning step requirements are greatly relaxed.

A self-timed co-clocking scheme is proposed in Fig. 12 to coordinate the comparator and AZ amplifier. The comparator fires after a half-cycle long amplification phase, then resets the comparator, and starts the AZ phase immediately after the comparison is done. This avoids comparator metastability while ensuring maximum time for both phases, which minimizes settling error. It also reduces the comparator power by ∼30% by turning off the comparator early and preserving the charge on the dynamic preamplifier integration capacitors [4].

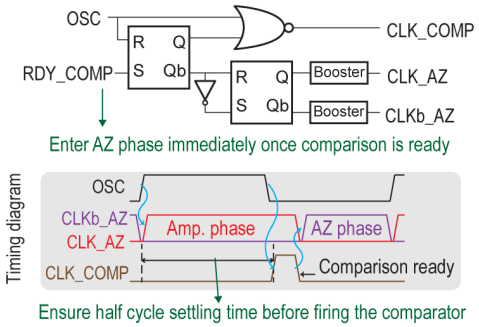


Fig. 12. Schematic and timing of the AZ and comparator clock generator.

A 36-b digital correlator implemented with custom digital cells for minimum leakage current processes the incoming data at the comparator output. Prior work has demonstrated that it can effectively overcome transmitter asynchronization with a 2× oversampling rate [2], [6], [7], [15].

The AZ amplifier, comparator, and correlator are clocked by an *RC* relaxation oscillator with an on-chip resistor and capacitor. A similar architecture proposed to the one shown in [22] is implemented. It has sub-100 ppm/°C temperature stability and ∼1-nW power consumption.

V. Temperature Compensation Techniques

Prior-art nanowatt-level WuRXs were not temperature-compensated, yet the implemented architectures have obvious places where temperature variation can adversely affect the performance. For example, without proper compensation, temperature variation can affect the proposed system performance in the following ways.

1) If the clock frequency deviates from the nominal 2× data rate, it is possible that the received sequence could be greater or less than 36 bits, which reduces the ability of the correlator to accurately identify the correct sequence.
2) If the RF or conversion gain drops, the ED and the BB amplifier NFs increase.
3) If the ED or BB amplifier bandwidth drifts too low, this could introduce settling errors and inter-symbol interference, whereas if they drift higher, this leads to excess noise.

All these effects lead to sensitivity degradation. It should be noted that the gain of the BB amplifier also depends on the temperature; however, as long as the BB gain does not fall below 12 dB, there is minimal degradation in SNR and thus not a compelling reason to compensate it over PVT. Thus, for a WuRX system to operate robustly across temperature variation, the following blocks must be compensated for their temperature dependences: the relaxation oscillator, the RF/conversion gain, the ED bandwidth, and the BB amplifier bandwidth.

A. Relaxation Oscillator

To avoid the missing bit or redundant bit, the accumulated frequency error over 36 cycles needs to be less than 1-bit length. Thus, the oscillator frequency must have

$$\left|\frac{36}{f_{\text{osc}}}-\frac{36}{f_{\text{nominal}}}\right|<\frac{1}{f_{\text{osc}}} \tag{2}$$

where f_{osc} is the oscillator frequency and f_{nominal} is the nominal clock frequency, which is equal to 2× data rate. By solving (2), the oscillator frequency error must be $< \pm 1/36$, *i.e.* $\pm 2.77\%$. This can be easily achieved with the relaxation oscillator in Section IV-E, which ensures $< \pm 1\%$ frequency error across temperature after a one-point trim.

B. RF/Conversion Gain

The passive RF gain does not exhibit significant temperature dependence since it is comprised of passive elements that themselves do not have large temperature coefficients (TCs). Thus, no explicit compensation is required. However, the ED k factor depends on the sub-threshold slope factor, n, and the thermal voltage V_{T} [10]

$$k \propto N\left(\frac{1}{n}-\frac{1}{2}\right)\frac{1}{V_{\text{T}}}. \tag{3}$$

Simulation shows that the k factor changes by 25% from −10 to 40 °C, which corresponds to a sensitivity loss of only 1.2 dB. This was deemed to be acceptable, in part because the relatively low loss, and further compensation would incur a significant power penalty.

C. ED Temperature Stabilization via a CTAT Bulk Bias

The ED bandwidth exhibits a strong temperature dependence and must be compensated. The proposed solution is straightforward; since the ED output bandwidth is set by its output impedance, the bandwidth can be fixed by directly adjusting the output impedance via a bulk-biasing technique. Specifically, for the diode-connected transistors of the ED shown in Section III, the diode channel resistance r_{d} is temperature dependent because of the threshold voltage, which is given by

$$V_{\text{t}} = V_{\text{t}_0}+\gamma\left(\sqrt{|2\emptyset_{\text{F}}+V_{\text{SB}}|}-\sqrt{|2\emptyset_{\text{F}}|}\right)\approx V_{\text{t}0}+\frac{\gamma\, V_{\text{SB}}}{4\emptyset_{\text{F}}} \tag{4}$$

where V_{t_0} is the threshold voltage for zero substrate bias, γ is the body effect parameter, V_{SB} is the source-to-body substrate bias, and $\emptyset_{\text{F}}$ is half surface potential. This approximation is valid given $|V_{\text{SB}}| < |2\emptyset_{\text{F}}| \approx 0.7\ V$. To compensate the complementary-to-absolute-temperature (CTAT) V_{t_0}, and the proportional-to-absolute temperature (PTAT) $2\emptyset_{\text{F}}$, V_{SB} needs to be PTAT as well to keep V_{t} and r_{d} constant. Based on the simulation for the 65-nm CMOS process, a +10-mV/C change compensates the threshold voltage change.

To accomplish this, the bulk voltage of the ED's transistors is fed by a CTAT voltage to generate the desired PTAT V_{SB}. Fig. 13 shows the schematic of the CTAT bulk voltage generator, which consists of a PTAT three-transistor temperature-sensing element and a PTAT-to-CTAT amplifier. The PTAT element is similar to the work in [23] and [24] and generates a 1.2-mV/C PTAT voltage. The PTAT element is biased between V_{DD} and $-V_{\text{DD}}$, which is generated by an on-chip charge pump [2], to provide a negative output voltage

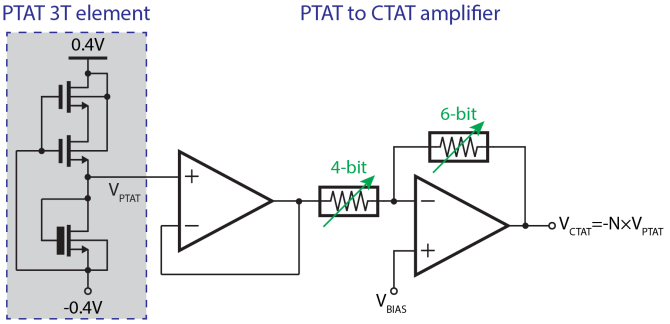


Fig. 13. Schematic of the ED bulk bias circuit.

covering −10 to 40 °C range. The PTAT voltage is converted to CTAT and the slope is corrected to cover the 500-mV difference in V_{SB} required for the range from −10 to 40 °C. Programmable resistors provide a tunable multiplication ratio to overcome process variation. Note that the multiplication ratio is independent of the resistor's TC. The entire ED compensation block consumes 11.8 nW at 20 °C.

D. BB Amplifier Temperature-Stabilization via a Constant-Current Bias

The BB amplifier's bandwidth also exhibits a strong temperature dependence. As shown previously, the BB amplifier is loaded by 10-pF MIM capacitors, which exhibits almost no temperature sensitivity. As a result, the temperature dependence of the bandwidth is dominated by the change of the amplifier output resistance

$$BW_{\mathrm{AMP}} \propto 1/r_{\mathrm{AMP}} \propto \lambda I_{\mathrm{AMP}} \tag{5}$$

where r_{AMP} and I_{AMP} are the output resistance and bias current of the BB amplifier, respectively, and λ is the channel length modulation parameter. It has been shown that λ exhibits no significant temperature variation, which means that if the amplifier bias current is constant, so would its bandwidth [20].

A regulated Beta-multiplier is employed to generate a temperature-insensitive current. As shown in [22], the bias resistor TC should be ∼1/300 (*i.e.* 3333 ppm/K) when compensating the system in the vicinity of 300 K. This led to choosing to implement the biasing resistor as a P+ polysilicided resistor with a TC of ∼2880 ppm/K, which is close to the optimal value. The residue TC of the bias current (∼500 ppm/K in simulation) corresponds to a 2.5% variation in BW over the range from −10 to 40 °C.

VI. Measurements

The RF die (which contains the ED, CMFB, and BB amplifier) was fabricated in a 65-nm CMOS process to minimize ED parasitics, while the BB die (comparator, correlator, and oscillator) was fabricated in a 180-nm CMOS process to minimize leakage. The dies were stacked on top of each other during assembly to save area, as shown in Fig. 14. At room temperature, the system (excluding the temperature-compensation blocks) consumes 7.3 nW operating from a 0.4-V supply, with most of the power (4.4 nW) devoted to the BB amplifier for noise reasons. The temperature-compensation blocks consume an additional 15 nW. To test the chips across

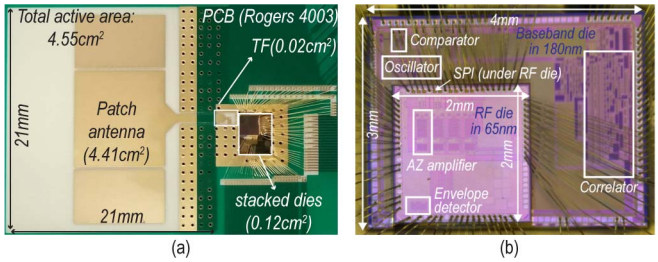


Fig. 14. Annotated photograph of (a) PCB and (b) stacked die.

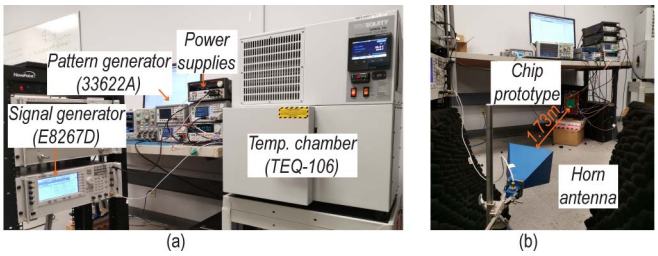


Fig. 15. Photographs of (a) temperature test setup and (b) wireless test setup.

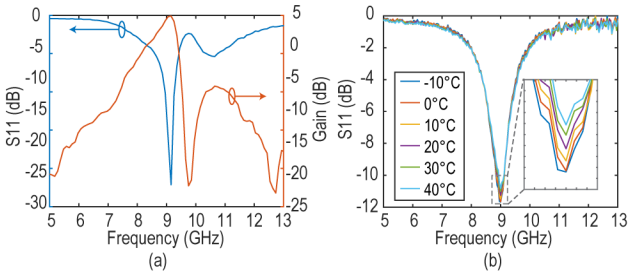


Fig. 16. Measured (a) antenna S_{11} and gain and (b) transformer S_{11}.

temperature, they were placed in a temperature chamber [see Fig. 15(a)], while the wireless link test was done at room temperature by separating the horn transmitter 1.73 m (56.3-dB loss) away from the receiver [see Fig. 15(b)].

As shown in Fig. 16, the patch antenna had a peak gain of 5 dB, and < −10-dB S_{11} between 8.95 and 9.27 GHz, covering the desired 9-GHz band. The gain had a zero at 9.7 GHz, which helps with out-of-band rejection. The MN's S_{11} was characterized over temperature (−10 to 40 °C) with no significant change in center frequency or bandwidth, as shown in Fig. 16(b). This suggests that both the bond wire inductor Q and the ED input resistance are temperature-insensitive. The MN's gain was measured at the BB amplifier output by de-embedding the ED and BB amplifier gain. The MN alone showed a gain of 13.5 dB, which is lower than 19 dB expected from simulations. This was caused by lower than expected ED input resistance due to the substrate dielectric losses, as confirmed post-layout extraction simulations using EMX. The gain loss can be remedied by shielding the ED's RF input trace in future work.

The BB amplifier was characterized by applying an external signal at its input and digitizing the output with an external analog-to-digital converter (ADC) synchronized to the AZ clock. The PSD was calculated based on a 1-h long measurement. As shown in Fig. 17(a), the amplifier PSD was flat

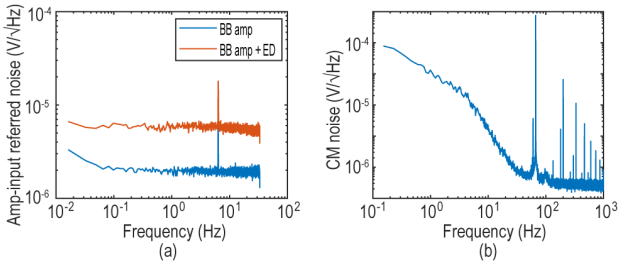


Fig. 17. Measured noise PSD in (a) differential mode and (b) common mode.

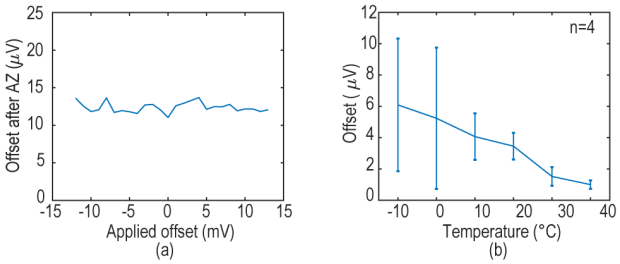


Fig. 18. Measured AZ amplifier (a) input-referred offset and (b) offset over temperature.

down to ∼20 mHz due to the $1/f$ noise reduction of the AZ operation. The PSD from both the ED and BB amplifier was flat since the passive ED does not introduce any $1/f$ noise. The tone at 6.6 Hz was due to intermodulation between the 66.6-Hz on-chip clock and the 60-Hz powerline interference, which would be reduced in a battery-powered implementation. The CM PSD is shown in Fig. 17(b), where it can be observed that the CMFB loop bandwidth is ∼4 Hz, set by the CMFB amplifier output resistance and C_c.

To illustrate the effectiveness of the offset-canceling capability, an external dc voltage was applied between the amplifier replica inputs and signal inputs to mimic ED offset. As shown in Fig. 18(a), the amplifier can tolerate ±13-mV offset, which is much greater than the actual ED offset, based on the simulation. After connecting the ED and amplifier, the overall offset was measured across temperature [see Fig. 18(b)]. Since the offset is largely determined by random mismatch, four chips were measured, and the results are consistent.

The performance of the temperature-compensation blocks was characterized from −10 to 40 °C. The ED bulk bias showed CTAT behavior with a −10-mV/°C TC [see Fig. 19(a)], and the amplifier bias current was almost temperature-insensitive with only a 2.6% change across the temperature range [see Fig. 19(b)]. The relaxation oscillator frequency dropped from 67.1 to 66.1 Hz, which is stable enough to avoid a missing bit or redundant bit given the 540-ms sequence.

The overall BB bandwidth and integrated noise of the whole system were both measured across temperature, as shown in Fig. 20(a). The bandwidth was nearly constant between 0 and 30 °C due to the bias techniques applied to ED and BB amplifier. The bandwidth dropped at −10 °C since the amplifier PMOS tail transistor was at the edge of saturation, resulting in less current. The bandwidth increased at 40 °C

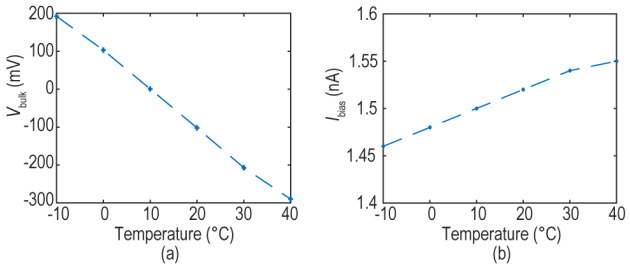


Fig. 19. Measured (a) ED bulk bias and (b) BB amplifier current reference.

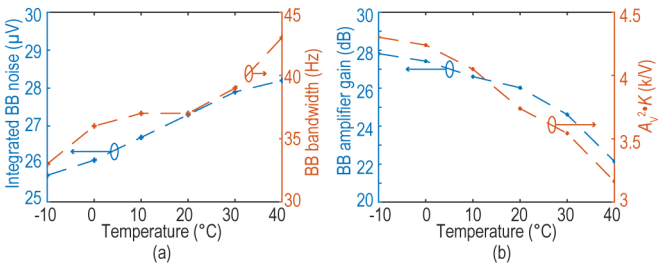


Fig. 20. Measured (a) BB bandwidth and noise and (b) BB gain and RF/conversion gain.

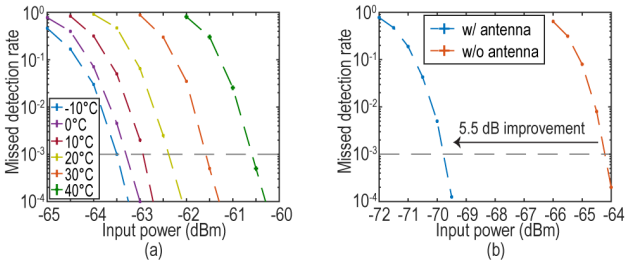


Fig. 21. Measured MDR curves (a) over temperature without antenna and (b) with and without antenna at uncontrolled room temperature.

because the amplifier's input transistors were at the edge of saturation, thereby exhibiting lower output impedance. Both could be overcome with a larger supply voltage, at the expense of higher quiescent power. As expected, the integrated noise slightly increased with the temperature [see Fig. 20(a)] since the noise is mostly determined by the ED output integrated noise, which is PTAT given a fixed ED output capacitance. The combined MN gain, ED k factor ($= A_V^2 k$), and amplifier dc gain are plotted in Fig. 20(b). Across temperature, the gain dropped by 29%, which matches the simulation. The amplifier gain dropped by 6 dB because of the open-loop, uncompensated architecture.

Fig. 21(a) shows the waterfall curves for the wake-up signature missed detection rate (MDR) over temperature without the antenna. The system configurations (*e.g.*, bias settings and comparator threshold setting) were fixed during the temperature sweep. Since the amplifier gain increases as the temperature decreases, the comparator sees a larger signal and noise amplitude at lower temperature. With a fixed threshold voltage, the worst false alarm rate (FAR) happens at the low temperature (−10 °C), while the worst MDR occurs at high temperature (40 °C). This explains the shifting of the

TABLE I
COMPARISON TO STATE-OF-THE-ART WURXS

	[25] ESSCIRC'17	[6] JSSC'19	[7] SSCL'18	[5] ISSCC'19	[12] RFIC'17	[15] ISSCC'12	[16] ASSCC'12	**This Work**
	N-ZERO WuRX (<100 nW)				GHz WuRX			**N-ZERO & GHz**
RF frequency (MHz)	405	151.8	109	434.4	2,400	5,800	5,800	**9,000**
Technology	180 nm	130 nm	180 nm	65 nm	65 nm	130 nm	180 nm	**65/180 nm**
Power supply (V)	0.4	1/0.6	0.4	0.4	0.8/0.5/0.1	3	1/0.5	**0.4**
Correlator depth (bit)	32	8	36	22	32	32	16	**36**
Clock source	Relax. osc.	Ring osc.	Relax. osc.	Ring osc.	Relax. osc.	No	No	**Relax. osc.**
MN gain (dB)	18.5	27	30.6	23	N/A	3	2	**13.5**
Antenna gain (dB)	N/A	N/A	N/A	N/A	N/A	N/A	N/A	**5**
Demodulator	Pseudo-balun CG	Single-ended Dickson	Pseudo-balun Dickson	Single-ended Dickson	Cross-coupled rectifier	Pseudo diff. CG	Pseudo diff. CG	**Pseudo-balun Dickson**
BB Coupling type	DC	AC	AC	AC	DC	DC	AC	**DC**
Wu-latency (ms)	53.3	>80	180	110	12.8	1.14	0.16	**540**
Sensitivity (dBm)	-63.8	-76	-80.5	-79.1	-61.5[c]	-45	-50	**-64/-69.5[c]**
Normalized sensitivity[a] (dB)	-70.2	-81.5	-84.2	-81.0	-71[c]	-59.7	-69	**-65.3/-70.8[c]**
Temperature Range (°C)	N/A	N/A	N/A	N/A	N/A	N/A	N/A	**-10 ~ 40**
Lumped components	LC MN, capacitors	LC MN, capacitors	LC MN, capacitors	LC MN, resistor	None	LC MN	LC MN	**None**
Total area (cm^2)	>2.4	N/A	>6	N/A	1.875[c]	N/A	N/A	**0.14/4.5[c]**
Power (nW)	4.5	7.6	6.1	0.42	365	30,000	10,000	**7.3[d]/22.3**
FoM[b] w/o TC (dB)	-123.7	-132.7	-136.4	-148	-105.4[c]	-73.2	-89.0	**-116.7/-122.2[c]**
FoM[b] w/ TC (dB)	N/A	N/A	N/A	N/A	N/A	N/A	N/A	**-111.9/-117.4[c]**

[a] $P_{SEN,norm}$ (dB)= P_{SEN}+5log(latency). [b] Sensitivity-power-latency FoM (dB)= $P_{SEN,norm}$−10log(power/1mW). [c] Including antenna. [d] Excluding temperature compensation blocks.

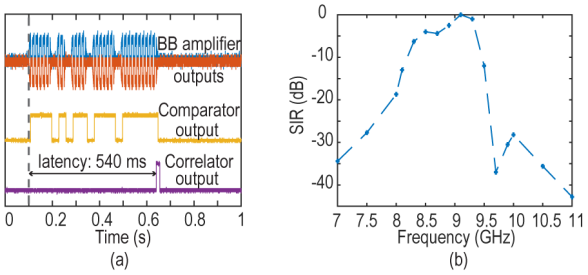


Fig. 22. Measured (a) transient waveform and (b) SIR versus frequency.

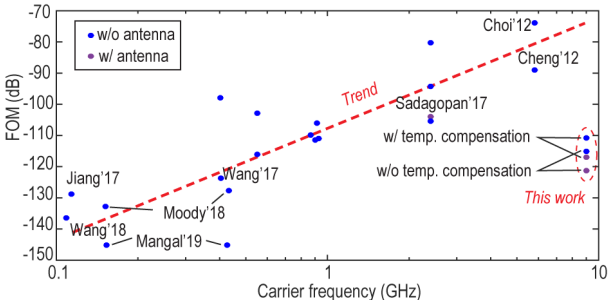


Fig. 23. Landscape of WuRXs.

MDR curves over temperature. The worst case FAR is 0.08/h. (one in a 12-h measurement at −10 °C). It should be noted that the ∼3-dB MDR shift matches with the 6-dB amplifier gain reduction. Due to the ED squaring function, the RF input signal needs to be 3 dB larger to have 6 dB higher swing at the BB. Fig. 21(b) shows the MDR curve with the antenna. Operating with the antenna had a 5.5-dB sensitivity improvement compared to without the antenna (−69.5 versus −64 dBm), which closely matches with the antenna gain measurement result.

Fig. 22(a) shows the transient waveforms demonstrating a wake-up event when the correct code is transmitted. A modulated signal tone along with a pseudorandom binary sequence (PRBS) modulated at a frequency offset Δf to the center frequency was used to test the WuRX performance under interference. The input signal power was set to 1 dB higher than the power where MDR = 10^{-3} (*i.e.* at −68.5 dBm), and the interferer power was swept until the MDR = 10^{-3}. The signal-to-interferer ratio (SIR) versus interference frequency is shown in Fig. 22(b). The notch at 9.7 GHz was due to the zero in the antenna gain.

Table I summarizes the system performance and compares it with prior art. The proposed design is the first-reported sub-100-nW WuRX that operates at gigahertz frequencies. The WuRX requires no off-chip lumped components and occupies only 4.55 cm^2 of area, including the antenna. It is also the first WuRX that employs temperature compensation and reports the temperature stability.

Fig. 23 plots the figure of merit (FoM) from [4] of the proposed WuRX alongside prior work versus carrier frequency. There is a clear trend of FoM degradation at higher frequencies, largely due to the reduced passive RF gain, while operating at 9 GHz, this article demonstrates an FoM (excluding the temperature -compensation blocks) of −116.7 and −122.2 dB without and with antenna, respectively, which is higher than prior-art gigahertz-range WuRXs.

VII. Conclusion

A 22.3-nW power, 9-GHz WuRX was designed for area-constrained, ultra-low-power applications. By adaptively biasing the ED with a CMFB loop around the BB amplifier, and AZ the BB amplifier offset, the ac-coupling capacitors were removed. These techniques avoid any off-chip BB components while achieving narrow BB bandwidth to minimize noise. Due to the offset-free architecture and temperature-compensated blocks (ED, amplifier, and oscillator), this receiver performance only degrades 3 dB over a 50 °C temperature range. Due to the high ED input impedance, this article achieves a state-of-the-art FOM compared to high frequency (>1 GHz) WuRXs.

References

[1] P. P. Mercier and A. P. Chandrakasan, Eds., *Ultra-Low-Power Short-Range Radios*. Cham, Switzerland: Springer, 2015.

[2] N. M. Pletcher, S. Gambini, and J. Rabaey, "A 52 μW wake-up receiver with −72 dBm sensitivity using an uncertain-IF architecture," *IEEE J. Solid-State Circuits*, vol. 44, no. 1, pp. 269–280, Jan. 2009.

[3] N. E. Roberts *et al.*, "A 236 nW −56.5 dBm-sensitivity Bluetooth low-energy wakeup receiver with energy harvesting in 65 nm CMOS," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Jan. 2016, pp. 450–451.

[4] P. P. Wang *et al.*, "A near-zero-power wake-up receiver achieving −69-dBm sensitivity," *IEEE J. Solid-State Circuits*, vol. 53, no. 6, pp. 1640–1652, Jun. 2018.

[5] V. Mangal and P. R. Kinget, "A 0.42 nW 434 MHz −79.1 dBm wake-up receiver with a time-domain integrator," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 2019, pp. 438–440.

[6] J. Moody *et al.*, "Interference robust detector-first near-zero power wake-up receiver," *IEEE J. Solid-State Circuits*, vol. 54, no. 8, pp. 2149–2162, Aug. 2019.

[7] P. P. Wang, "A 6.1-nW wake-up receiver achieving −80.5-dBm sensitivity via a passive pseudo-balun envelope detector," *IEEE Solid-State Circuits Lett*, vol. 1, no. 5, pp. 134–137, May 2018.

[8] *Molex-204287: ISM 433 MHz Flex Antenna*. Accessed: May 8, 2019. [Online]. Available: https://www.molex.com/molex/products/datasheet.jsp

[9] *Molex-13299: Thin-Film Battery, 3.0V Plus*. Accessed: May 8, 2019. [Online]. Available: https://www.molex.com/molex/products/datasheet.jsp?part=active/0132990001_ACCESSORIES.xml

[10] J. Moody *et al.*, "A −76 dBm 7.4 nW wakeup radio with automatic offset compensation," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 2018, pp. 452–454.

[11] C. A. Balanis, *Antenna Theory: Analysis and Design*, 3rd ed. New York, NY, USA: Wiley, 2005.

[12] K. R. Sadagopan, J. Kang, S. Jain, Y. Ramadass, and A. Natarajan, "A 365 nW −61.5 dBm sensitivity, 1.875 cm^2 2.4 GHz wake-up receiver with rectifier-antenna co-design for passive gain," in *Proc. IEEE Radio Freq. Integr. Circuits Symp. (RFIC)*, Jun. 2017, pp. 180–183.

[13] K. Yadav, I. Kymissis, and P. R. Kinget, "A 4.4-μW wake-up receiver using ultrasound data," *IEEE J. Solid-State Circuits*, vol. 48, no. 3, pp. 649–660, Mar. 2013.

[14] A. S. Rekhi and A. Arbabian, "Ultrasonic wake-up with precharged transducers," *IEEE J. Solid-State Circuits*, vol. 54, no. 5, pp. 1475–1486, May 2019.

[15] *The Advantages of X-Band*, XTAR, Ashburn, VA, USA, 2019. Accessed: Sep. 4, 2019. [Online]. Available: https://xtar.com/x-band/

[16] J. Choi, K. Lee, S. Yun, S. Lee, and J. Ko, "An interference-aware 5.8 GHz wake-up radio for ETCS," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 2012, pp. 446–448.

[17] K. W. Cheng, X. Liu, and M. Je, "A 2.4/5.8 GHz 10 μW wake-up receiver with −65/−50 dBm sensitivity using direct active RF detection," in *Proc. IEEE Asian Solid State Circuits Conf. (A-SSCC)*, Nov. 2012, pp. 337–340.

[18] X. Huang, G. Dolmans, H. de Groot, and J. R. Long, "Noise and sensitivity in RF envelope detection receivers," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 60, no. 10, pp. 637–641, Oct. 2013.

[19] B. Razavi, *RF Microelectronics*, 2nd ed. Upper Saddle River, NJ, USA: Prentice-Hall, 2011.

[20] C. C. Enz and G. C. Temes, "Circuit techniques for reducing the effects of op-amp imperfections: Autozeroing, correlated double sampling, and chopper stabilization," *Proc. IEEE*, vol. 84, no. 11, pp. 1584–1614, Nov. 1996.

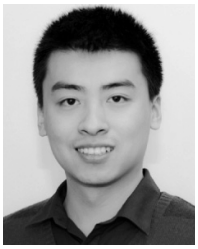
[21] H. Jiang *et al.*, "A 4.5 nW wake-up radio with −69 dBm sensitivity," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 2017, pp. 416–417.

[22] H. Jiang, P.-H. P. Wang, P. P. Mercier, and D. A. Hall, "A 0.4-V 0.93-nW/kHz relaxation oscillator exploiting comparator temperature-dependent delay to achieve 94-ppm/°C stability," *IEEE J. Solid-State Circuits*, vol. 53, no. 10, pp. 3004–3011, Oct. 2018.

[23] M. Seok, G. Kim, D. Blaauw, and D. Sylvester, "A portable 2-transistor picowatt temperature-compensated voltage reference operating at 0.5 V," *IEEE J. Solid-State Circuits*, vol. 47, no. 10, pp. 2534–2545, Oct. 2012.

[24] H. Wang and P. P. Mercier, "A 420 fW self-regulated 3 T voltage reference generator achieving 0.47%/V line regulation from 0.4-to-1.2 V," in *Proc. 43rd IEEE Eur. Solid-State Circuits Conf. (ESSCIRC)*, Sep. 2017, pp. 15–18.

[25] P.-H. P. Wang *et al.*, "A 400 MHz 4.5 nW −63.8 dBm sensitivity wake-up receiver employing an active pseudo-balun envelope detector," in *Proc. 43rd IEEE Eur. Solid State Circuits Conf. (ESSCIRC)*, Sep. 2017, pp. 35–38.



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