

A 2.5-20kSps in-pixel direct digitization front-end for ECoG with in-stimulation recording

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Closed-loop neuromodulation promises to enhance treatment for movement disorders, pain, and epilepsy. Advancements in low-impedance, high-density recording grids [1] have paved the way for low-noise neural recording systems with high spatial and temporal resolution. However, a conventional high-density neural recording signal path with programmable gain amplifiers (PGAs) and a shared ADC [2] saturates during stimulation because of the high amplifier gain. Due to a fundamental trade-off with the input high-pass cutoff frequency (for dc electrode offset elimination), it takes hundreds of ms to recover, leading to critical data loss. Recent advances in direct digitization-based analog front-ends (AFE) overcome this limitation by forgoing the amplifier and directly connecting the electrode to a high dynamic range ADC. Directly using a continuous time $\Delta\Sigma$ modulator (CTDSM) for this application has several notable challenges: slow recovery/instability during artifacts beyond the input range, power and area limitations, and low input impedance (Z_{in}). We report a $4\times$ array of per-pixel 2^{nd} -order $\Delta\Sigma$ ADCs (including the decimation filter) for ECoG with the fastest (sub-ms) artifact recovery time, enabling in-stimulation recording and power-efficient bandwidth scaling.

The 2^{nd} -order $\Delta\Sigma$ ADC architecture is shown in Fig. 1. While time-domain-only ADC architectures, such as voltage-controlled oscillator (VCO)-based ADCs, are popular for their ability to run off a low supply voltage and process scalability, they contend with issues such as VCO flicker ($1/f$) noise and compromised noise efficiency when utilized as the first integrator [3]. This system instead uses a G_m -C filter as the first integrator, utilizing chopping to reduce the flicker noise and a complementary input stage to double the noise efficiency. The second stage is an area-efficient time-based integrator realized by a G_m -current-starved current-controlled oscillator (CCO) with a counter. The 4-bit feedback capacitive DAC (CDAC) is mismatch-shaped with a 1^{st} -order shaped tree-structured dynamic element matching (DEM) encoder and resampled with a delay of 6.25% of the modulator sampling period to account for the quantizer and DEM delay. The pseudo-virtual ground feedforward architecture [3] allows the modulator to have high linearity and a compact area since it only needs a single feedback DAC despite being a 2^{nd} -order cascade of integrators feedback (CIFB) modulator. Deadband (DB) switches suppress the differential chopping artifacts at the G_m input; however, they must be large for low input-referred noise applications [4]. To remedy this, the DB switches are strategically moved from the sensitive input node to the G_m -C output and the feedforward input. Finally, an auxiliary-amplifier-based impedance booster [5] increases Z_{in} to $>30M\Omega$.

In theory, direct digitization offers uninterrupted monitoring; however, the modulator oscillates when overloaded if the phase difference at the n -bit counter output wraps modulo 2^n and is fed back into the loop. The stimulation artifacts in this application are large enough to momentarily over-range the ADC. This phase wrapping-induced instability requires resetting the modulator, leading to recording data corruption. Fig. 2 shows the fast-recovery, over-range detecting phase quantizer implementation. We introduce a saturation detector and expand the counter depth by two additional bits for faster recovery. The first additional bit detects saturation, while the second bit allows for reaction time without phase wrapping and loss of dynamic range (DR). The counters are implemented with a Gray code to minimize asynchronous sampling errors. The added bits are clocked at a fraction of the CCO frequency, f_{CCO} , and thus require negligible additional power. Recovery is nearly instantaneous after the artifact, with the delay determined by the decimation filter.

Neural signals are categorized by their frequency band and require an AFE with scalable power based on the operation mode. This design supports four modes covering 2.5–20kSps recording through a power-efficient bandwidth-scalable CTDSM. Fig. 3 shows the implementation of the G_m -C integrator with transconductance-based coefficient scaling, comprising four parallel G_m branches with drive strength ratios 1:1.2:4, which are turned on/off through the cascode

bias nodes to maintain a constant input capacitance. This switching is more power efficient than scaling the integration capacitor, C_i , and scaling the bias current alone is inaccurate. Each branch comprises a dual-tail, complementary-input transconductor biased in sub-subthreshold with a G_m/I_D of 40S/A for high noise efficiency.

Since this block's power efficiency is essential, medium V_t (MVT) devices were used to reduce the supply to 0.9V. With a 3.2fF unit CDAC element, the input devices are near minimum size to preserve SNR against input capacitive network attenuation. The G_m is cascoded to reduce leakage and enable downmodulation at a low-impedance node for faster settling. A triode-based common-mode feedback (CMFB) topology was chosen for its high input-linear range and stability. To minimize area, C_i uses anti-parallel NMOS varactors to cancel the even-order nonlinearity. The high capacitor density and differential topology save $4\times$ area over MIM or MOM caps. The second integrator comprises a CCO that combines the G_m -cells of the direct and feedforward paths. Its gain is scaled across modes through the number of CCO stages, which saves 2–8 \times power compared to frequency divider-based scaling. Part of the current is bled off to reduce f_{CCO} , reducing the counter's power by 2 \times , which is important as f_{CCO} is $\sim 10\times$ the sampling frequency, f_s . The CCO uses a pseudo-differential NMOS cross-coupled inverter architecture for noise efficiency.

Several system-level decisions were implemented to array this design and allow it to be scalable to thousands of channels on a chip. First, the decimation filter is implemented within each pixel, substantially reducing the datalink power, which is proportional to the oversampling ratio (OSR). This also offers stronger anti-aliasing rejection of out-of-band signals compared to the PGA+shared ADC architecture. Finally, for improved noise immunity, the serial data clock frequency, f_{DL} , is an integer multiple of f_s (across all modes), thus placing the energy in a null of the modulator's signal transfer function.

This 8-channel chip is fabricated in 180nm CMOS, with each channel occupying 0.09mm², including the digital blocks (decimation filter (18%), DEM (13%), and clock generation (3%)). Each channel consumes 14 μ W from 0.9V and 0.7V supplies for analog (53%) and digital (47%), respectively, where the latter can be reduced with technology scaling. This technology provides a cost-effective path for scaling to a 1024-channel array with bumped die chip-scale packaging. Fig. 4 shows a measured spectrum with and without decimation for a 125mV_{pp} full-scale (FS) sinusoidal input where the ADC achieves a 78.6dB SNDR and DR in a 10kHz bandwidth and an SFDR of 97.7dB with $f_s=1.28$ MHz and an $f_s/2$ chopping clock. The characteristic 40dB/decade noise-shaping from a 2^{nd} -order modulator is apparent in the spectrum. Due to the scalable architecture, the integrated input-referred noise is constant across the different modes. Channel-to-channel isolation of >60 dBc was measured by injecting a full-scale input on one channel while shorting the inputs of the others. The ADC output recovers in one decimated sample (50 μ s for BW=10kHz) with a 250mV (4x over-range) input. Fig. 5 compares this work with state-of-the-art neural recording front-ends.

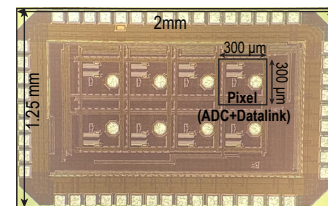
An *in vivo* whisker barrel rat experiment was performed to compare the performance with and without stimulation against a commercial chip [6]. Platinum-nanorod (PtNR) electrodes [1] captured ECoG activity (70–200Hz) simultaneously across all 8 channels, as shown in Fig. 6. During monopolar stimulation (500 μ A at 100Hz), the Intan chip saturated beyond its input range (~ 5 mV), resulting in data loss. In contrast, this chip outperformed by recovering with immediate observation of neural activity. This work showcases a scalable 2^{nd} -order $\Delta\Sigma$ ADC featuring the fastest in-pixel artifact recovery backed by *in vivo* data and unique power-efficient bandwidth scaling.

Acknowledgment:

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References:

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- [6] Intan RHD2164, https://intantech.com/files/Intan_RHD2164_datasheet.pdf.



Die micrograph.

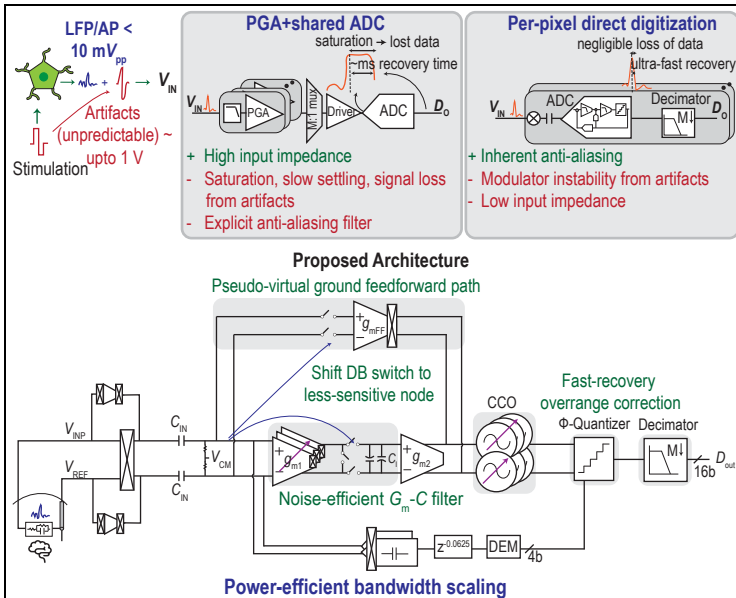


Fig. 1. Prior art and proposed neural recording AFE architecture.

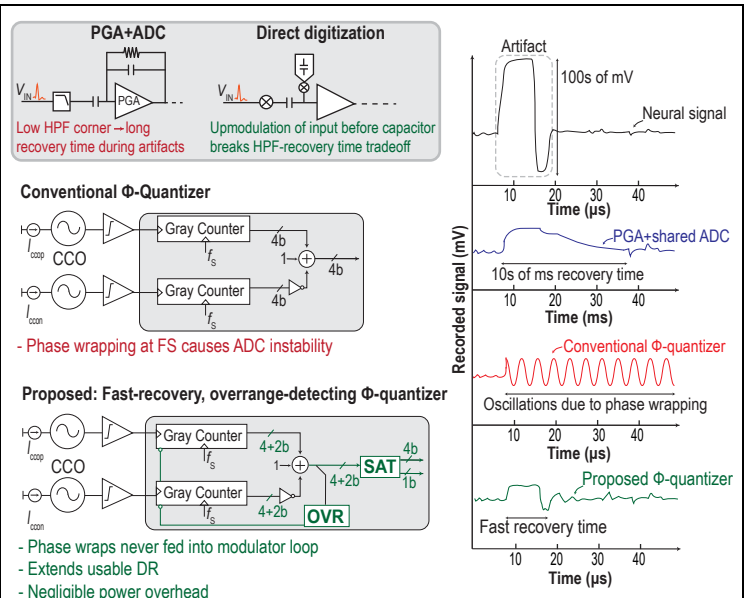


Fig. 2. Details of proposed phase quantizer.

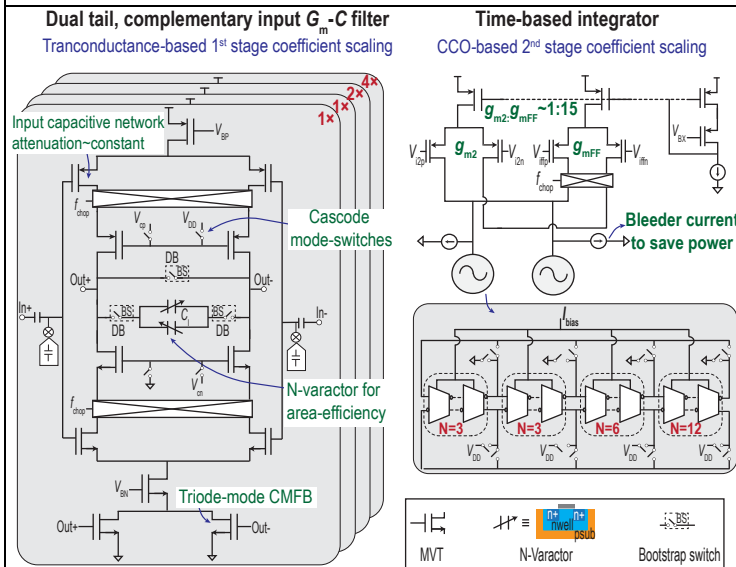


Fig. 3. Circuit implementation of power and G_m scalable 1st and 2nd integrator with feedforward (FF) path.

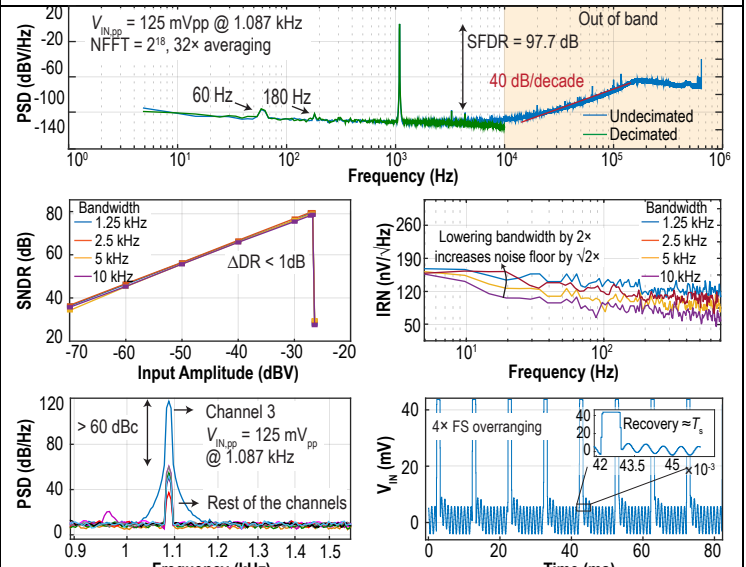


Fig. 4. Measured spectrum, SNDR versus input amplitude, input-referred noise, crosstalk, and artifact recovery.

Parameter	RHD 2164	Lopez TBCAS '17	Yoon VLSI '21	C Lee ISSCC '22	Wendl. ISSCC '21	X Yang VLSI '22	This Work
Topology	PGA + shared ADC		CT-DSM				CT-DSM
Input-type	Cap.	Cap.	Cap.	G_m	G_m	Cap.	Chopped Cap.
Tech. (nm)	500	130	65	180	180	22	180
# Channels	64	384	1024	4	8-24	128	8
Input FS (mV _{pp})	10	5	4.87	300	7	21.5	125
BW (kHz)	20	10	10	10	10	10	1.25 10
Power/ch. (μ W)	830	49	2.72	8.6	-	3.67	3.2 11.7
Power/ch. with decimator (μ W)	-	-	-	-	8.59	6.02	3.5 14
FoM _{SNDR} (dB)	137	-	162.4	178.1	147	157.2	163* 166*
SFDR (dB)	-	-	-	94.2	62	59.49	97 97.7
IRN (μ V _{rms})	2.4	6.36	8.98	6.6	4.37	7.71	5.9* 6*
Z _{IN} at DC (M Ω)	∞	∞	∞	∞	∞	∞	304 38
Crosstalk (dBc)	-	58	>60	-	72	-	>60
Stim. Artifact Tolerance	No		Yes	No		Yes	
Recovery Time (ms)	>> 100		-**	-	-	-	0.4 0.05

* Averaged over 12 chips **Unstable beyond input range

Fig. 5. Summary of performance and comparison to the state-of-the-art.

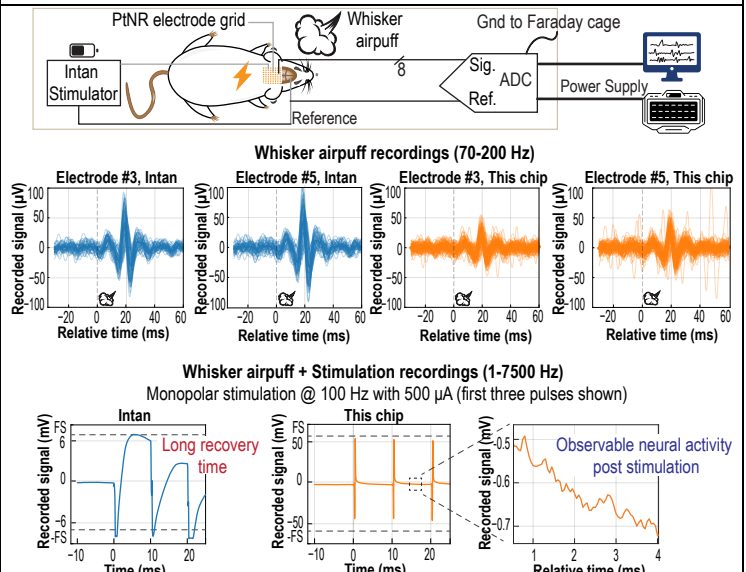


Fig. 6. In vivo experiment setup and neural recording comparison with commercial Intan chip.