CICC

IEEE Custom Integrated Circuits Conference

# 27-3: A 2.5-20kSps In-Pixel Direct Digitization Front-End for ECoG with In-Stimulation Recording

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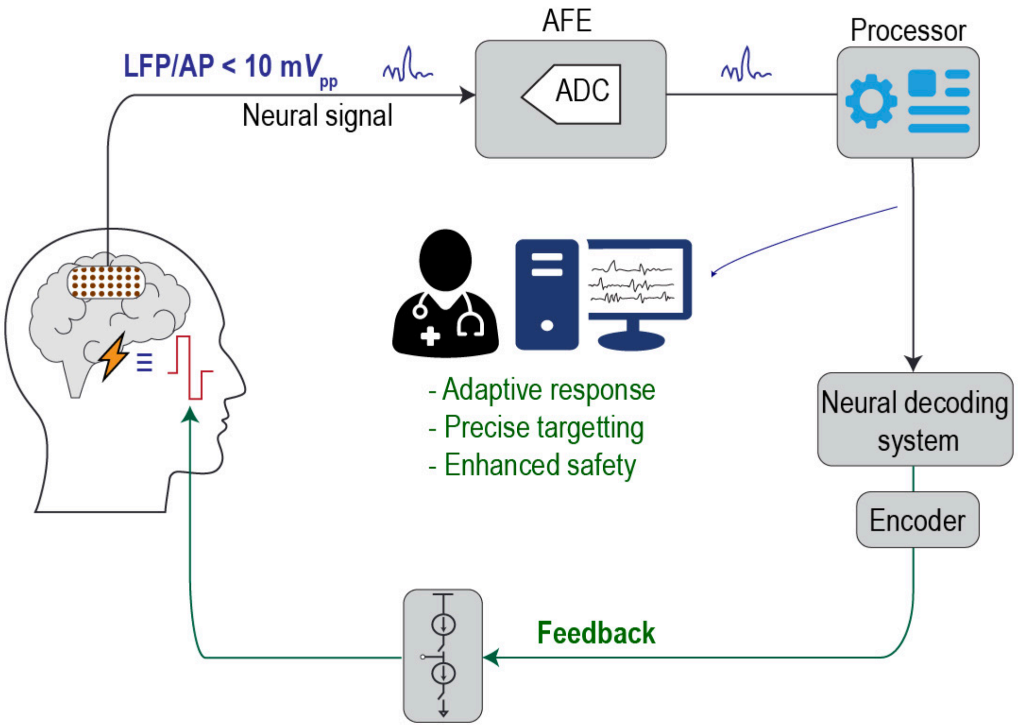
April 24th, 2024

# Closed-Loop Neuromodulation

- Real-time neural feedback guides stimulation
- Improves treatment for movement disorders, pain, and epilepsy
- High spatial and temporal resolution, low-noise neural recording

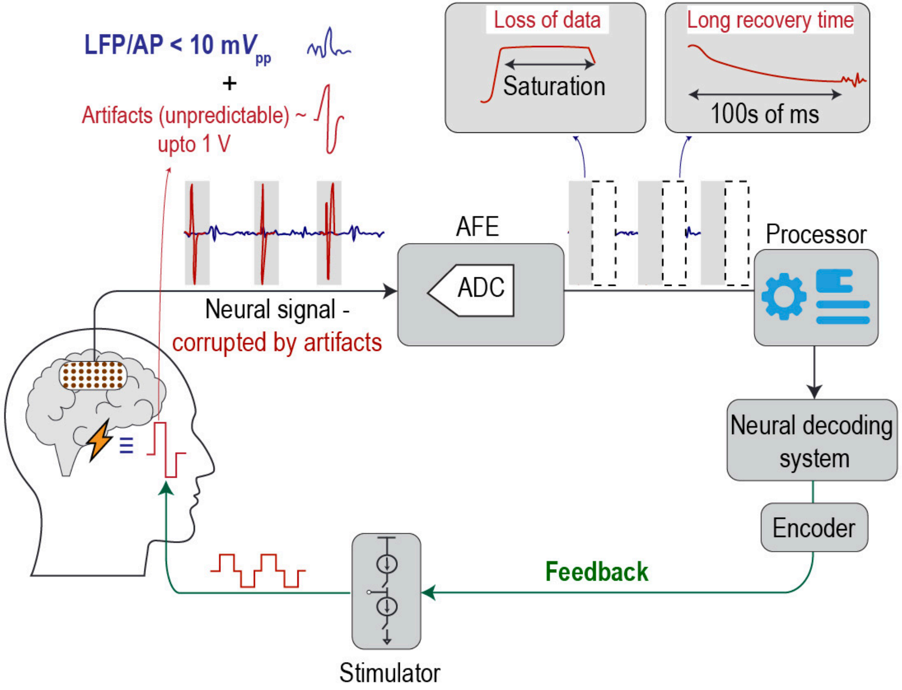



**Closed-loop neuromodulation improves therapy with precision and adaptability**

# Closed-Loop Neuromodulation: Stimulation Artifacts

Stimulation artifacts complicate signal acquisition:

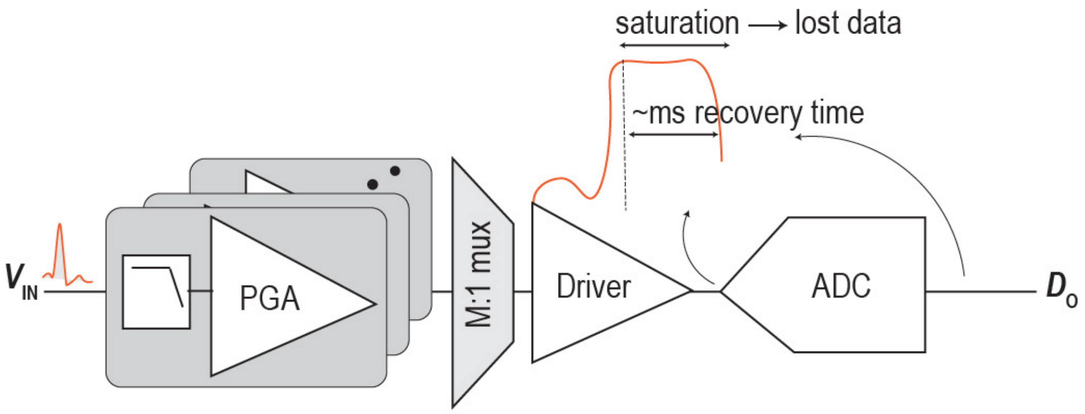
- Unpredictable shape, strength and duration
- Loss of neural data
- Long AFE recovery time




**Stimulation artifacts can result in critical neural data loss in closed-loop neuromodulation**

# Prior Neural recording AFE architectures

PGA + Shared ADC (Yoon *VLSI'21*)



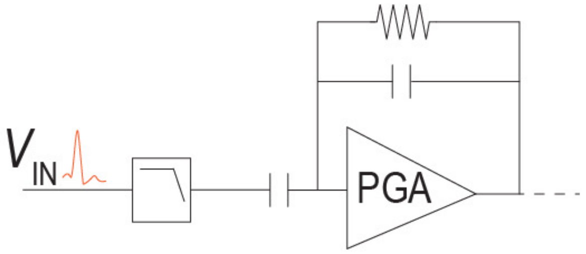

✓High input impedance

× Saturation, slow settling, signal loss from artifacts

× Explicit anti-aliasing filter

# Prior Neural recording AFE architectures

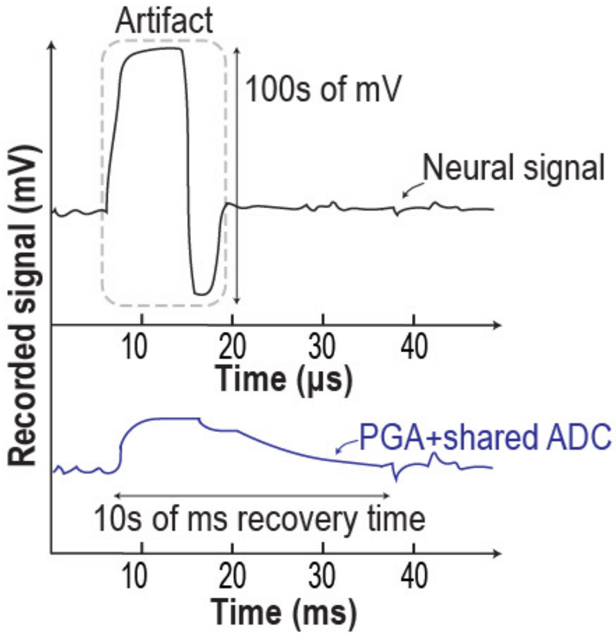
## PGA + Shared ADC (Yoon *VLSI'21*)




✓ DC electrode offset elimination ⇨ Low HPF corner

× Fundamental tradeoff with recovery time ⇨ slow settling

× Loss of neural data

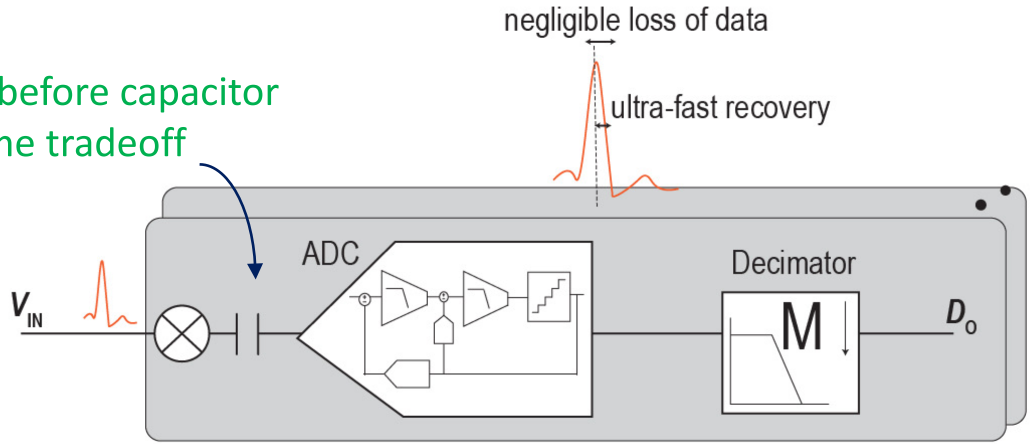



**PGA + Shared ADC saturates and recovers slowly from artifacts**

# Prior Neural recording AFE architectures

## Per-pixel Direct Digitization (Pochet *ISSCC'22*)

Upmodulation of input before capacitor breaks HPF-recovery time tradeoff

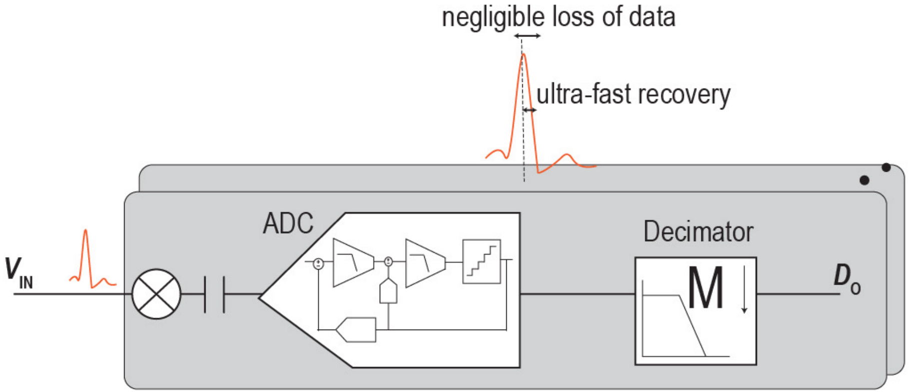



✓Higher DR to absorb DC electrode offset and artifacts

✓Inherent anti-aliasing

# Prior Neural recording AFE architectures

Per-pixel Direct Digitization (Pochet *ISSCC'22*)




✓Modulator instability/slow recovery from artifacts beyond input range

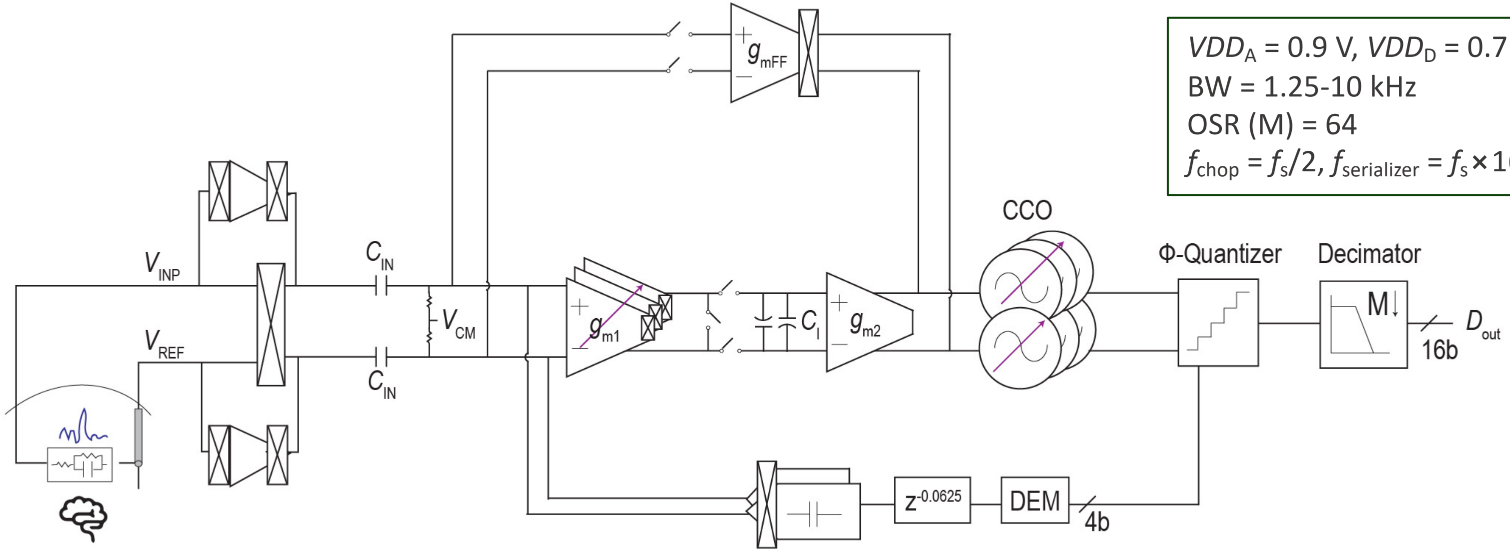
× Low input impedance

**2nd-order ΔΣ ADC with the sub-ms artifact recovery time and power-efficient bandwidth scaling is proposed**

# Outline

- Introduction
- System-level architecture
- Proposed solution for artifact recovery
- Circuit implementation
- Measurement results

# Proposed AFE System Architecture




$VDD_A$ = 0.9 V, $VDD_D$ = 0.7 V
BW = 1.25-10 kHz
OSR (M) = 64
$f_{chop} = f_s/2$, $f_{serializer} = f_s \times 16$

$G_{m,1}$ = 95 µS
$C_I$ = 9 pF

$G_{m,2}$ = 0.64 µS
$K_{CCO}$ = 27 MHz/µA

$G_{m,3}$ = 9.5 µS

$C_{DACu}$ = 3.2 fF
$C_{in}$ = 660 fF

CICC

# Proposed AFE System Architecture

$VDD_A$ = 0.9 V, $VDD_D$ = 0.7 V
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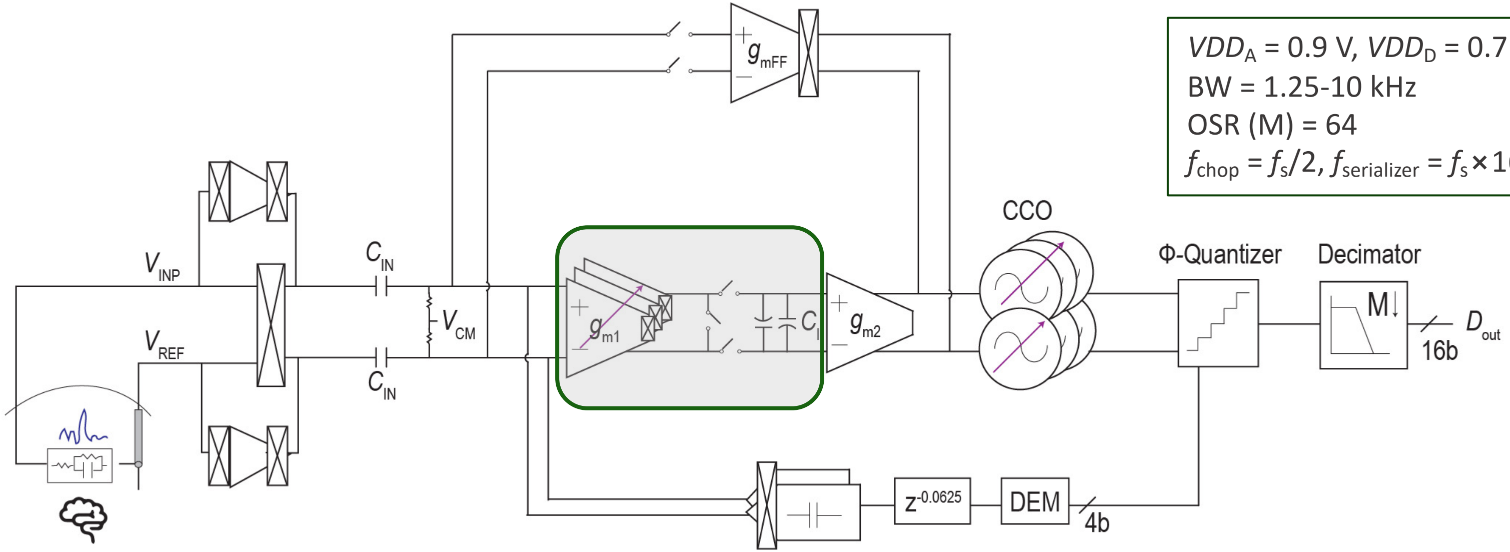
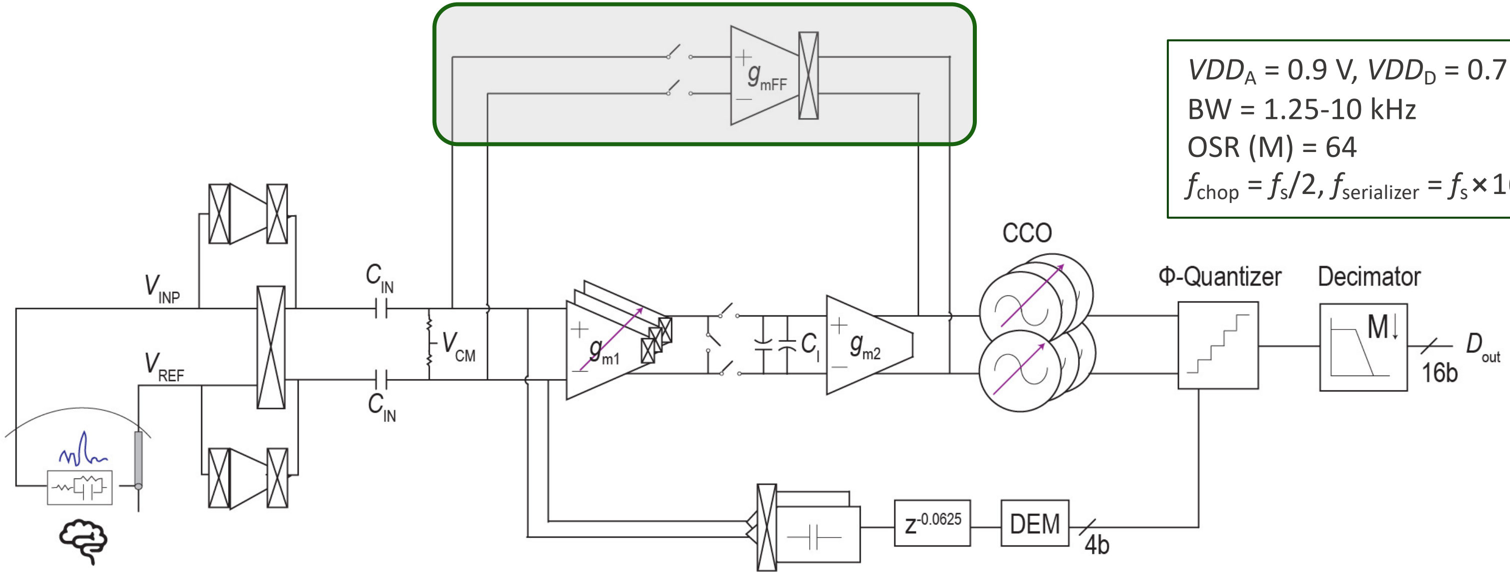



## 1. Noise-efficient Gm-C filter

- Chopping ⇨ Reduce flicker noise
- Complementary input stage ⇨ Higher noise efficiency

# Proposed AFE System Architecture

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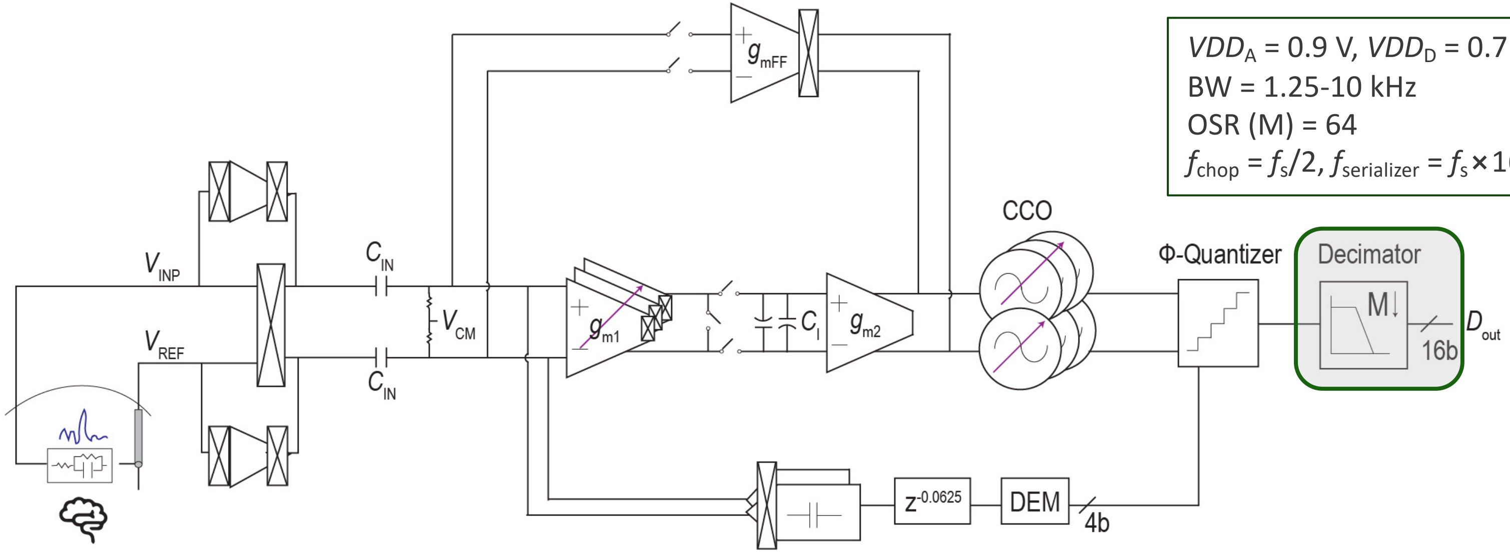
## 2. Pseudo-virtual ground feedforward path

- Requires single feedback DAC for a 2nd order CIFB modulator ⇨ Saves area
- 1st integrator is free of input ⇨ Higher linearity

# Proposed AFE System Architecture

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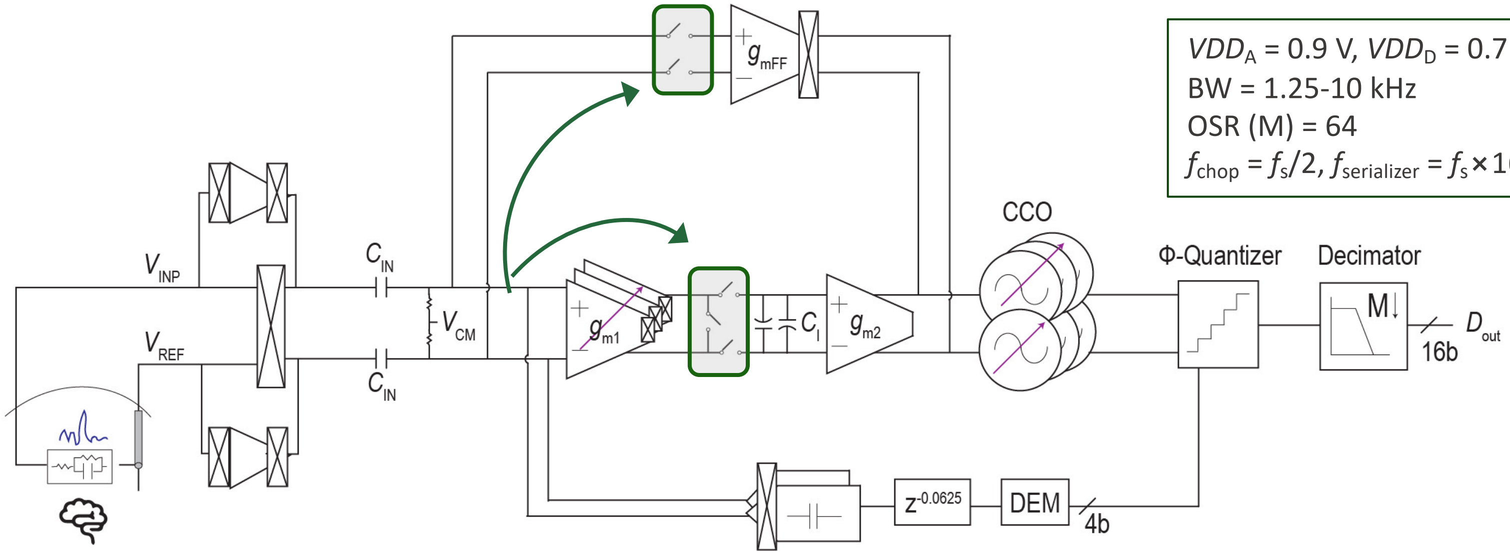
BW = 1.25-10 kHz
OSR (M) = 64
$f_{chop} = f_s/2$, $f_{serializer} = f_s \times 16$

## 3. Per-pixel Decimator

- Reduces the datalink power
- 3rd-order CIC filter ⇨ Stronger anti-aliasing rejection than PGA + shared ADC

# Proposed AFE System Architecture

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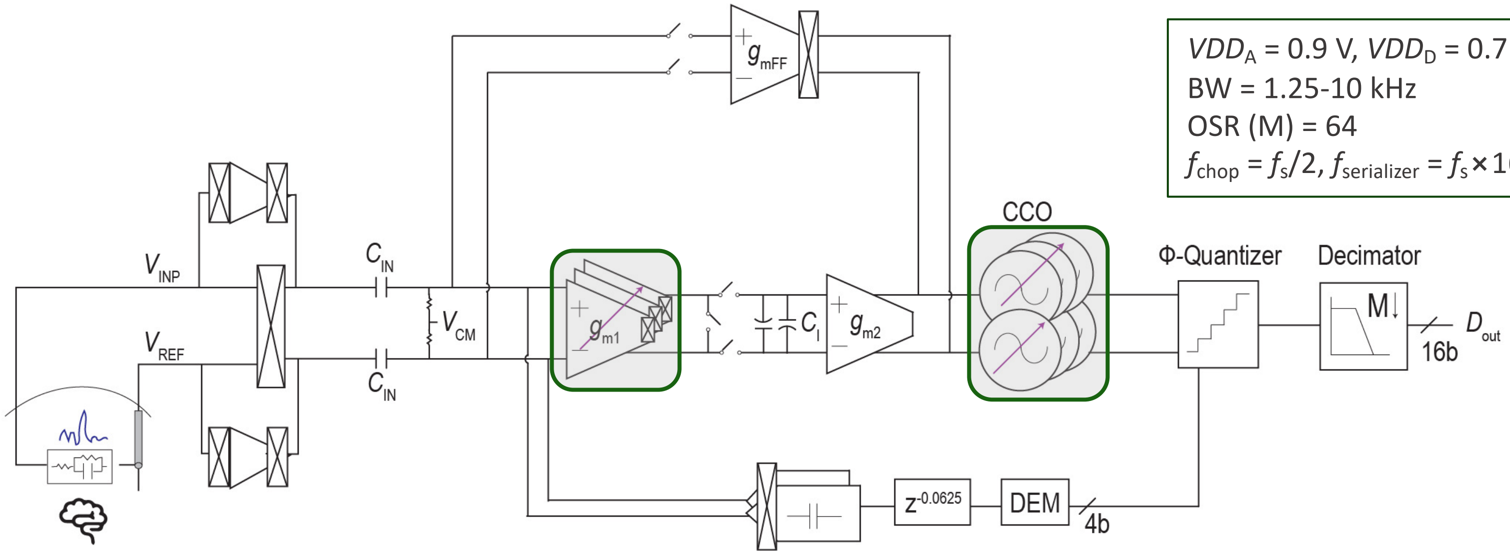
BW = 1.25-10 kHz
OSR (M) = 64
$f_{chop} = f_s/2$, $f_{serializer} = f_s \times 16$

## 4. Less-sensitive Dead Band (DB) switch

- Shifted to less-sensitive nodes ⇨ 1st-order noise-shaped
- > 10× smaller switch size ⇨ Reduces charge injection errors
- Anti-aliasing of CTDSM reduces to -21 dB at $f_s$ due to FF path and DB switch

# Proposed AFE System Architecture

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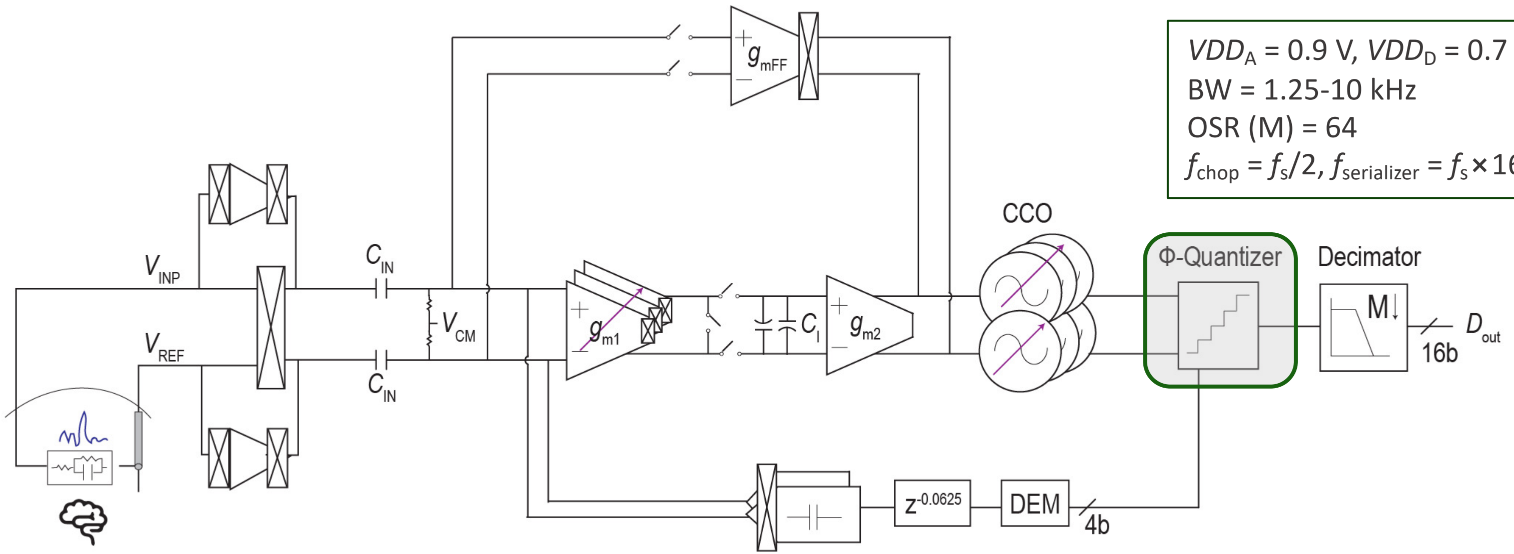
BW = 1.25-10 kHz
OSR (M) = 64
$f_{chop} = f_s/2$, $f_{serializer} = f_s \times 16$

## 5. Power-efficient bandwidth scaling

- Neural signals categorized by frequency band ⇨ require power-scalable AFE based on mode
- Supports four modes (2.5–20kSps) via power efficient bandwidth-scalable CTDSM

# Proposed AFE System Architecture

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BW = 1.25-10 kHz
OSR (M) = 64
$f_{chop} = f_s/2$, $f_{serializer} = f_s \times 16$

## 6. Fast-recovery overrange correction

- Sub-ms recovery time from stimulation artifacts
- Avoids modulator instability

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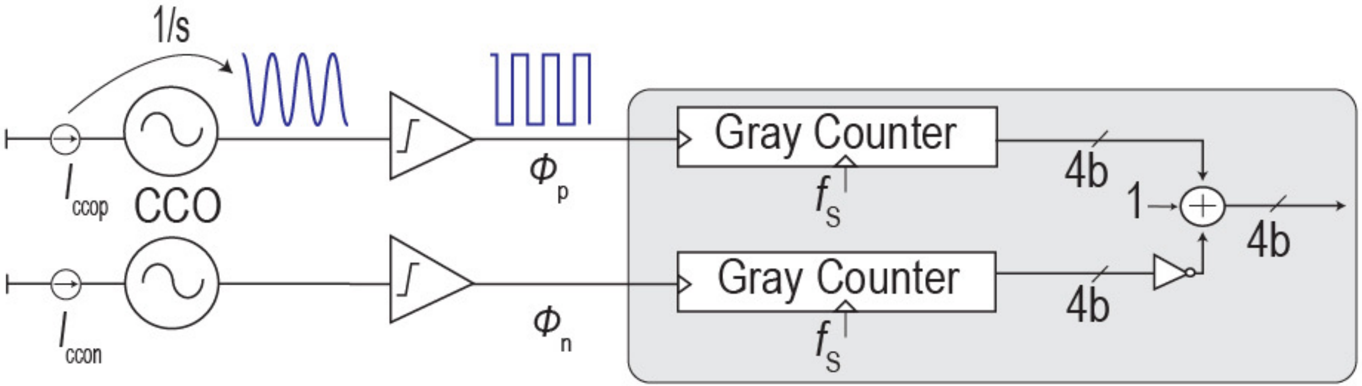
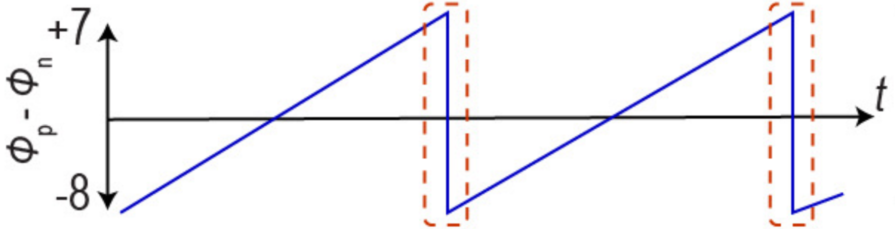
# Conventional ϕ Quantizer

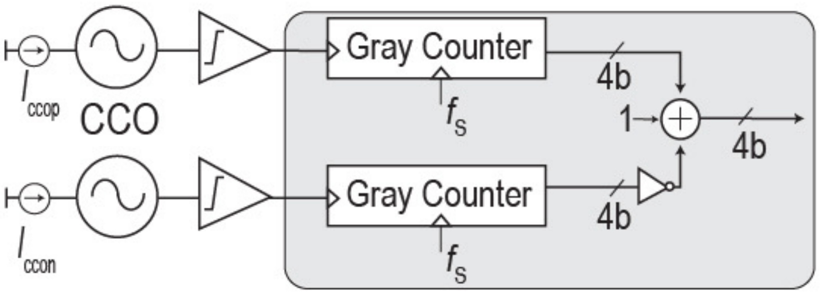



Highly variable (in amplitude) artifacts can over-range ADC

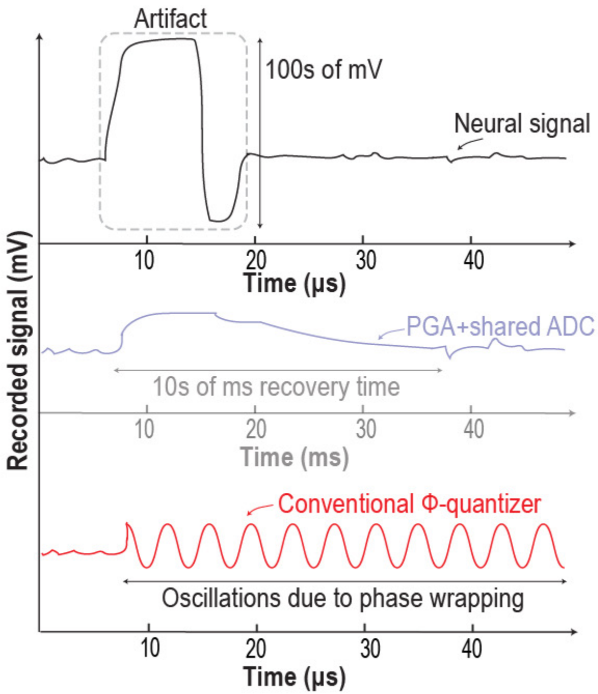



Large error fed into the modulator loop

# Conventional ϕ Quantizer

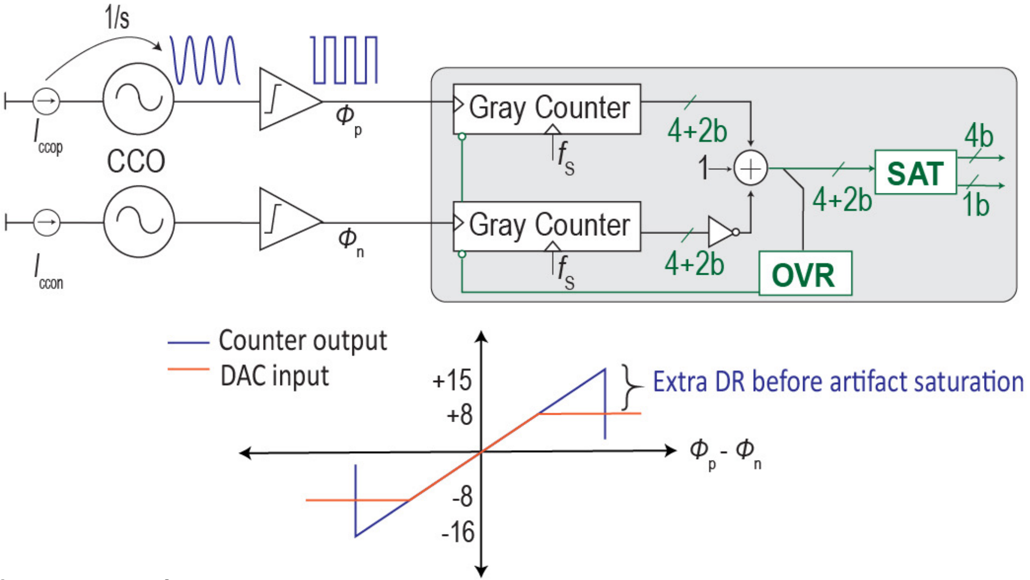



- Large errors fed into ADC during phase wrapping for input ≥ FS
- 2nd integrator rollover ⇨ modulator instability
- Modulator fails to recover without reset after input returns to normal




**Modulator instability/slow recovery from artifacts, which overrange the ADC**

# Proposed ϕ Quantizer




- Add a bit and reset the counters:

  Prevents modulator oscillation but offers lower DR than voltage quantizer DSM

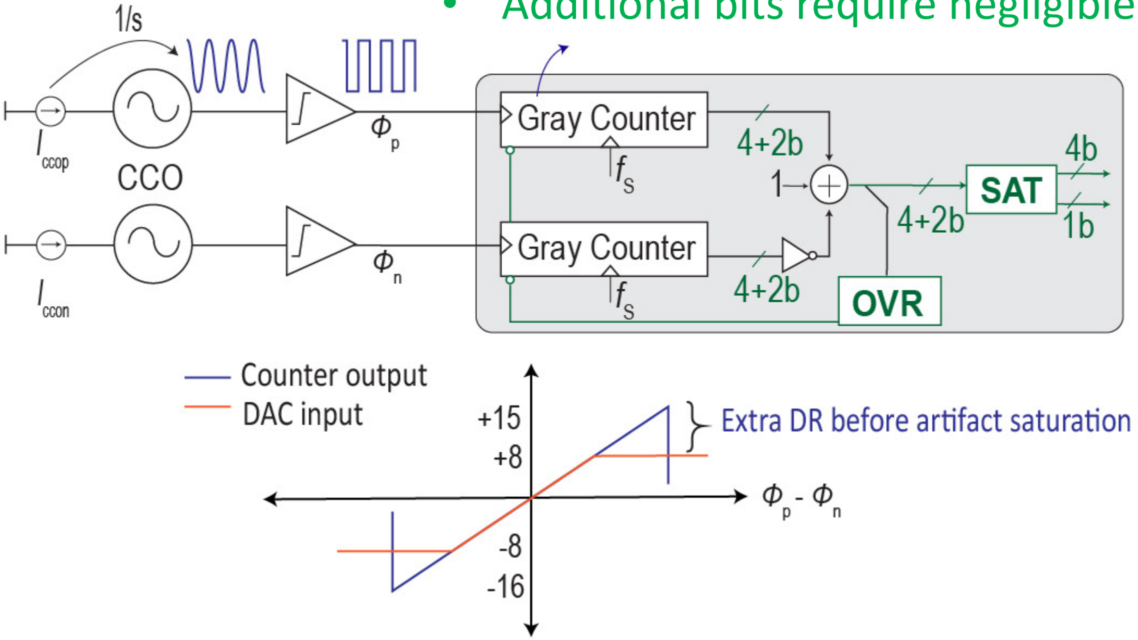
- Add second bit:

  First bit extends the DR through saturation, followed by second bit to reset

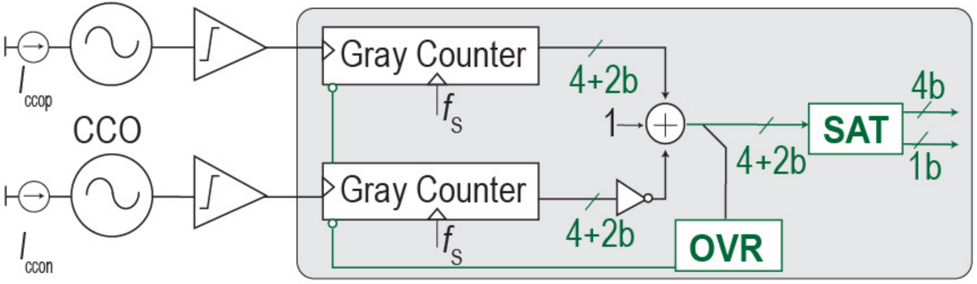
# Proposed ф Quantizer

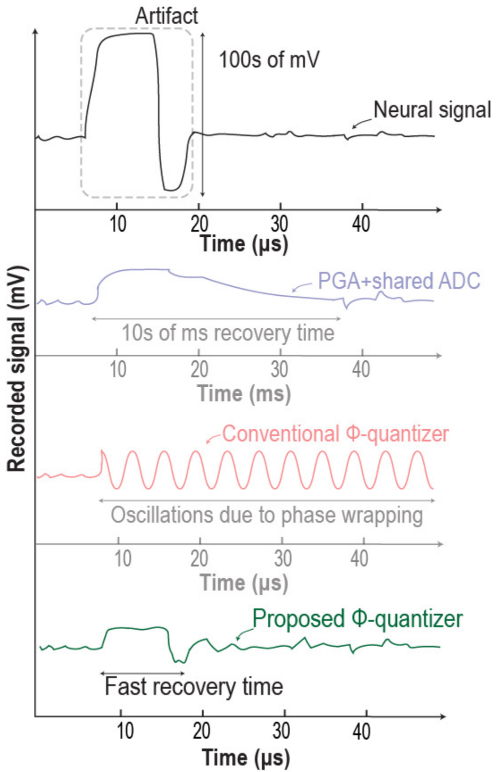
Minimize asynchronous sampling errors

- DFF-only counter which directly “counts” in gray code
- Additional bits require negligible (<10 %) extra power



# Proposed ϕ Quantizer




- ✓ Phase wraps never fed into modulator loop
- ✓ Extends usable DR
- ✓ Negligible power overhead

**Artifact recovery is nearly instantaneous, delay determined by decimation filter**

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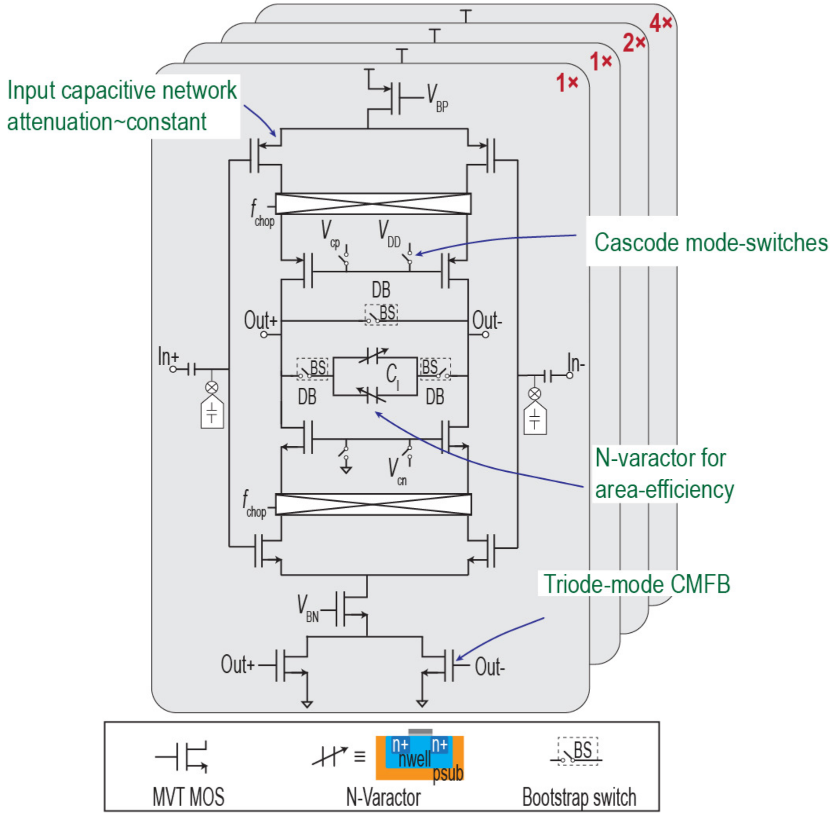
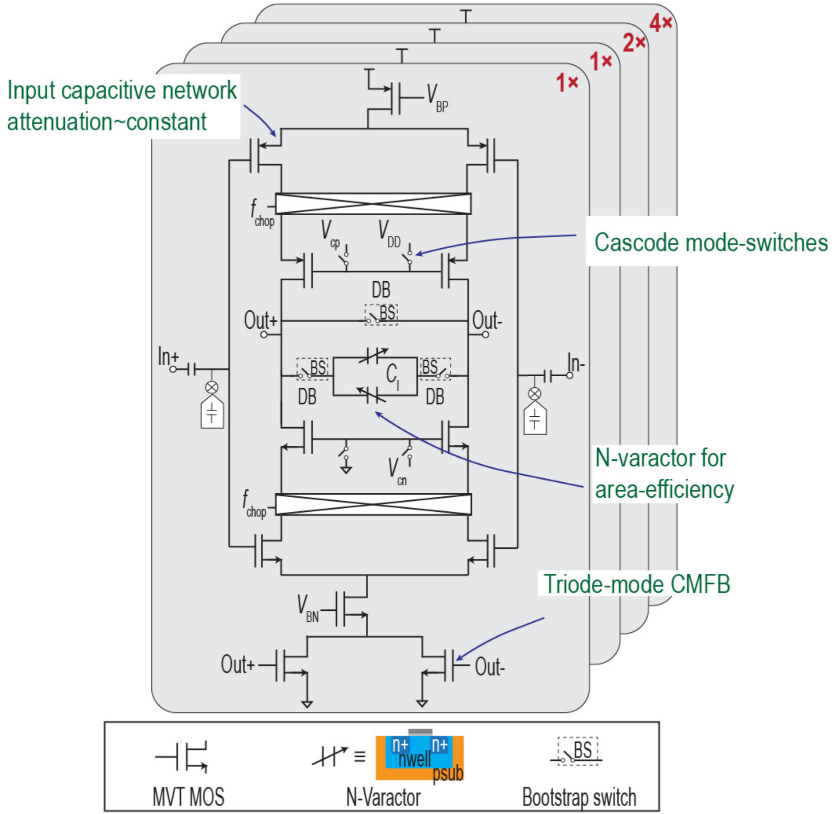
# $G_m$-$C$ Implementation

- Transconductance-based 1st stage coefficient scaling
  - Four parallel $G_m$ branches with drive strength ratios 1:1:2:4
  - Maintain ~constant input capacitance ⇨ Constant ~SNR due to input capacitive attenuation across modes
  - Power-efficient



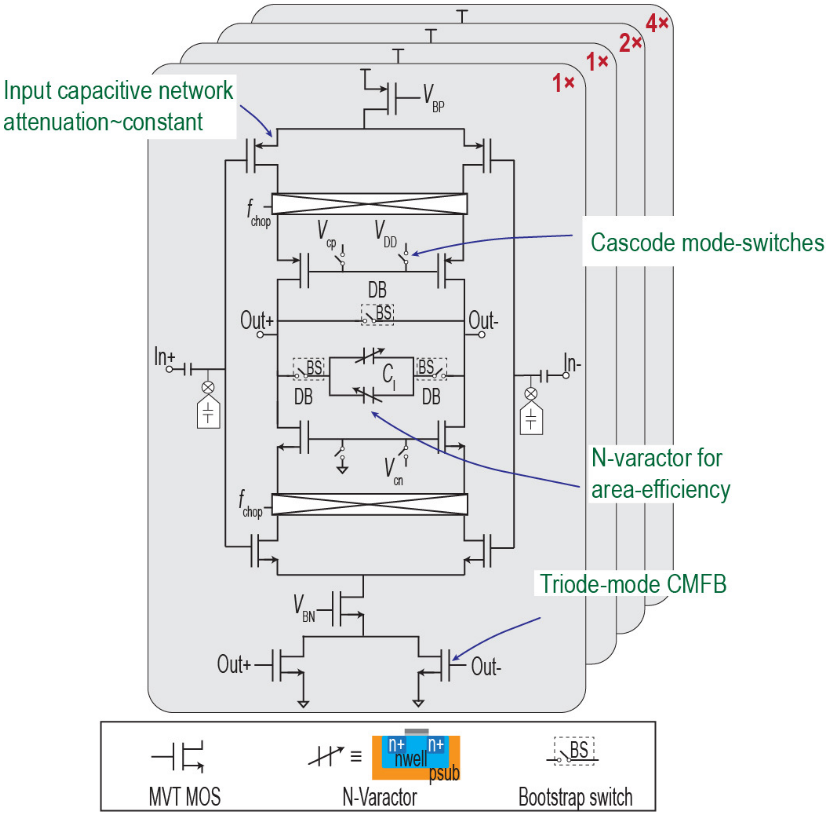
# $G_m$-$C$ Implementation

- Dual-tail, complementary-input transconductor
  - High noise-efficiency
  - Medium $V_t$ devices ⇨ power-efficiency



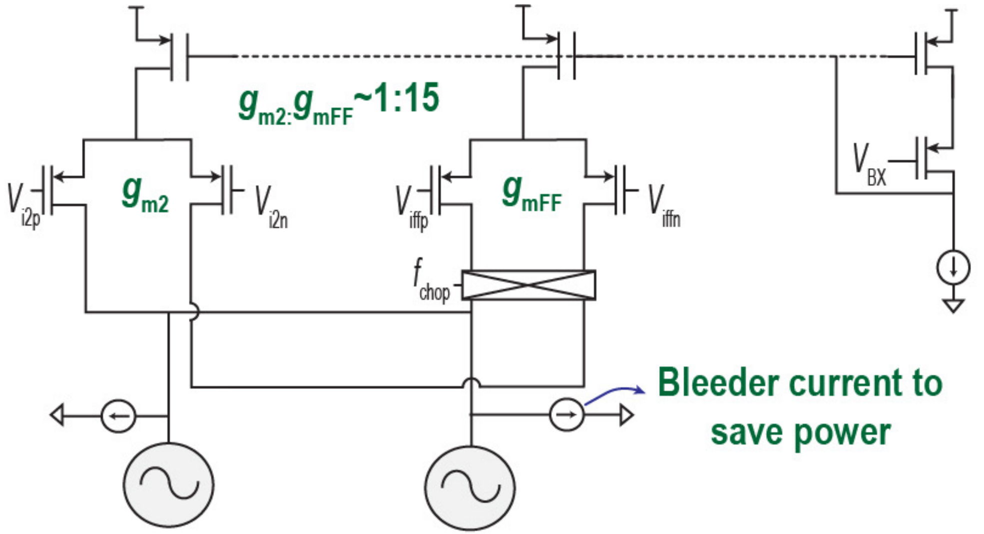
# $G_m$-$C$ Implementation

- $C_I$ composed of NMOS varactors
  - Save 4× area over MIM or MOM caps
  - Anti-parallel connection ⇨ cancels even-order nonlinearity
- Triode-based common-mode feedback (CMFB)



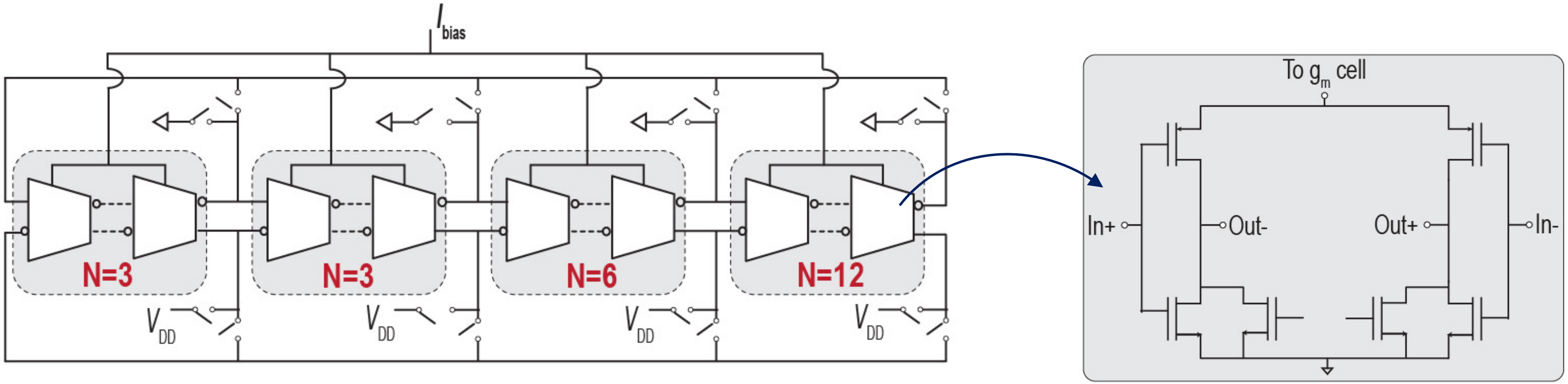
# 2nd $G_m$ cell and FF path Implementation

- 2nd Gm : FF Gm ~ 1 : 15
- ~50% current bled off ⇨ reduce $f_{CCO}$ ⇨ save digital power of ϕ quantizer



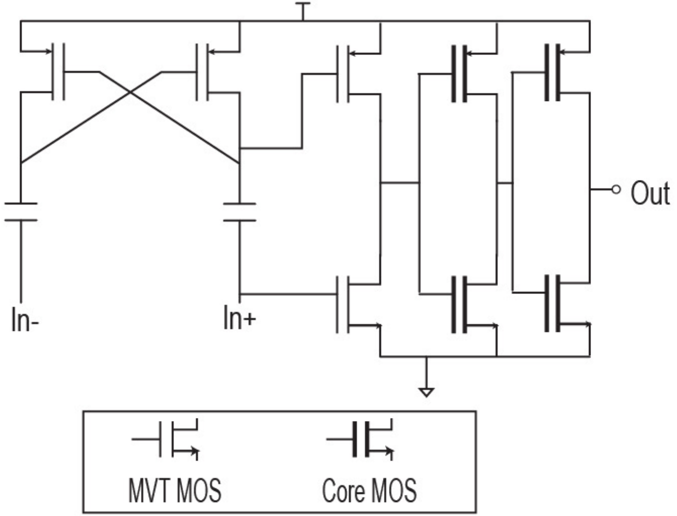
# CCO Implementation

- CCO-based 2nd stage coefficient scaling
  - Saves 2–8× power compared to frequency divider-based scaling
  - Pseudo-differential NMOS cross-coupled delay cell ⇨ noise efficiency



# Level Shifter Implementation

- Low latency to reduce signal-dependent loop delay
  - Reduce latch delay due to its signal dependency
  - Decouples the Nmos and Pmos driver with AC coupling
  - Reduces large delay from contention between pull–down and pull–up transistors in a conventional latch




Tan, S. C., and X. W. Sun. "Low power CMOS level shifters by bootstrapping technique." *Electronics letters* 38.16 (2002)

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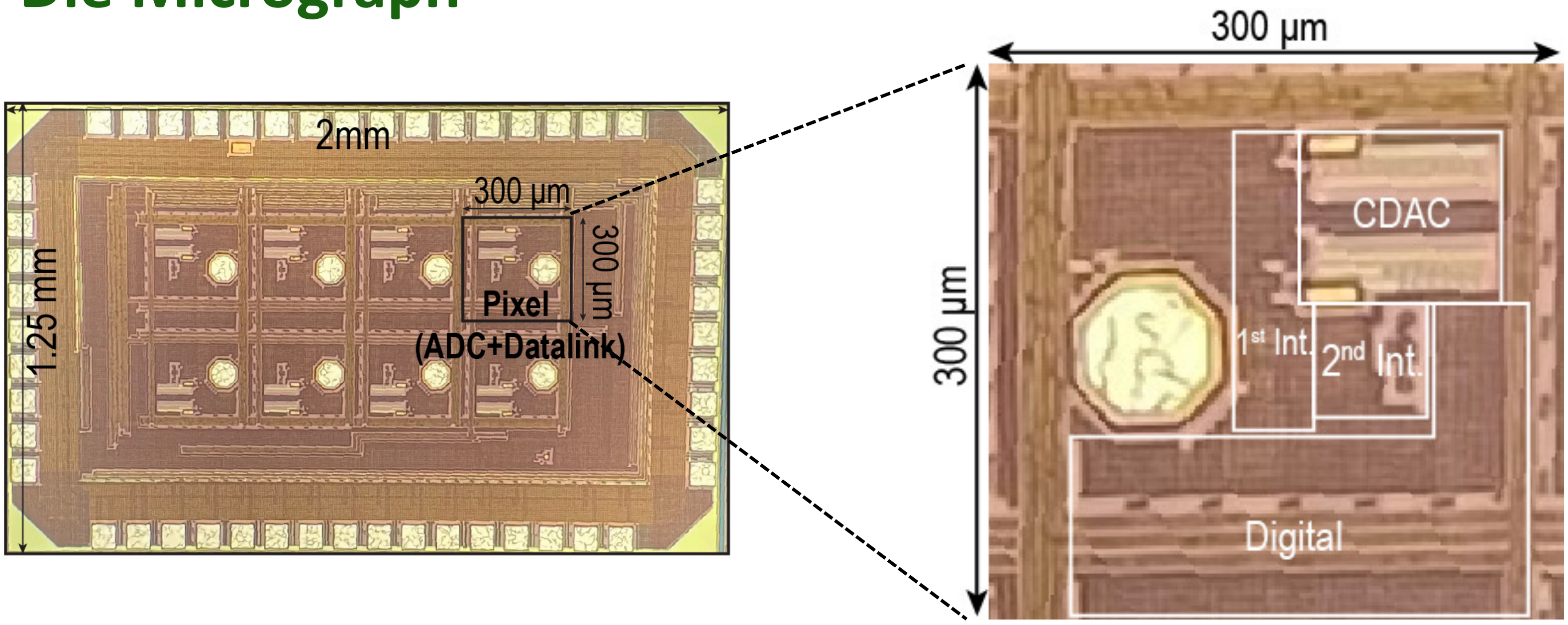
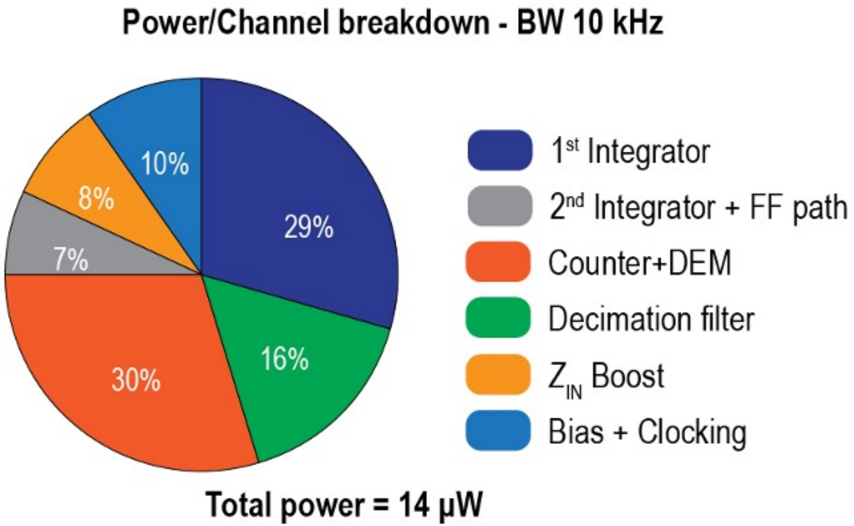
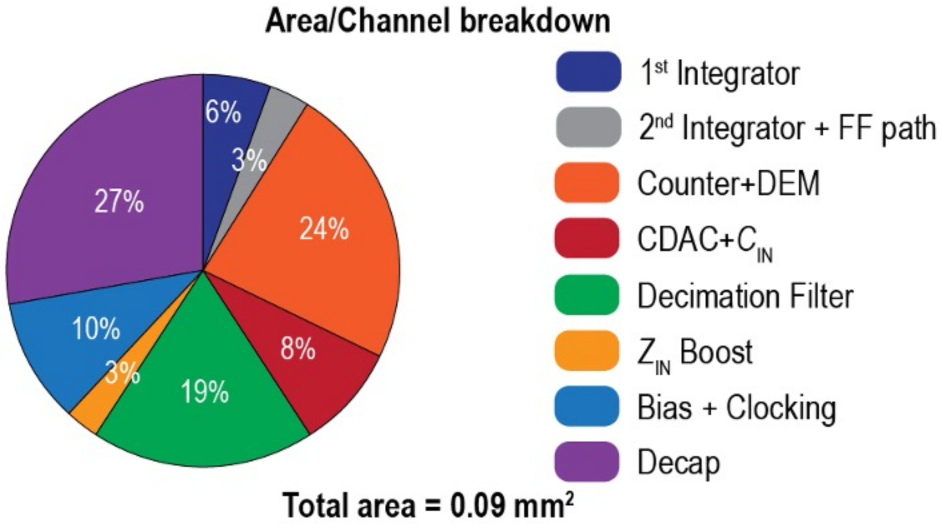
# Die Micrograph



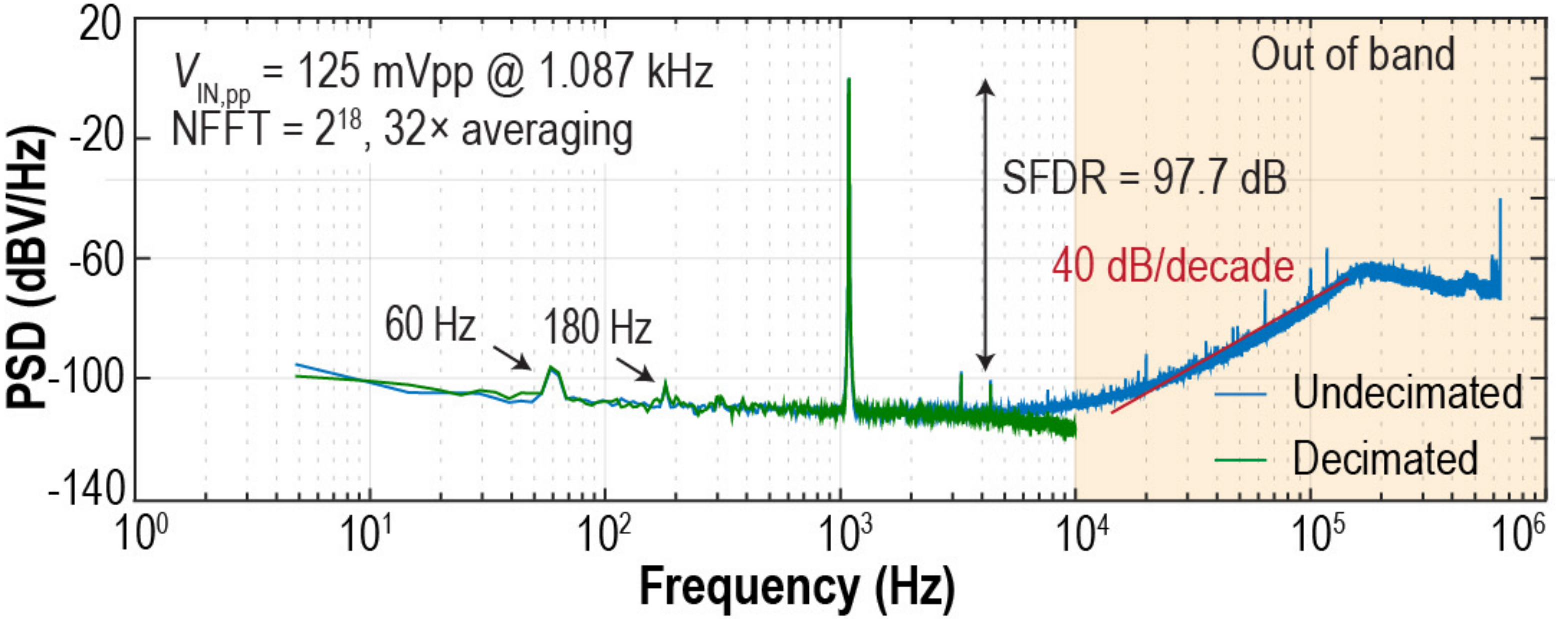

Chip designed in 180 nm with 0.09 $mm^2$/pixel

# Power and Area Breakdown

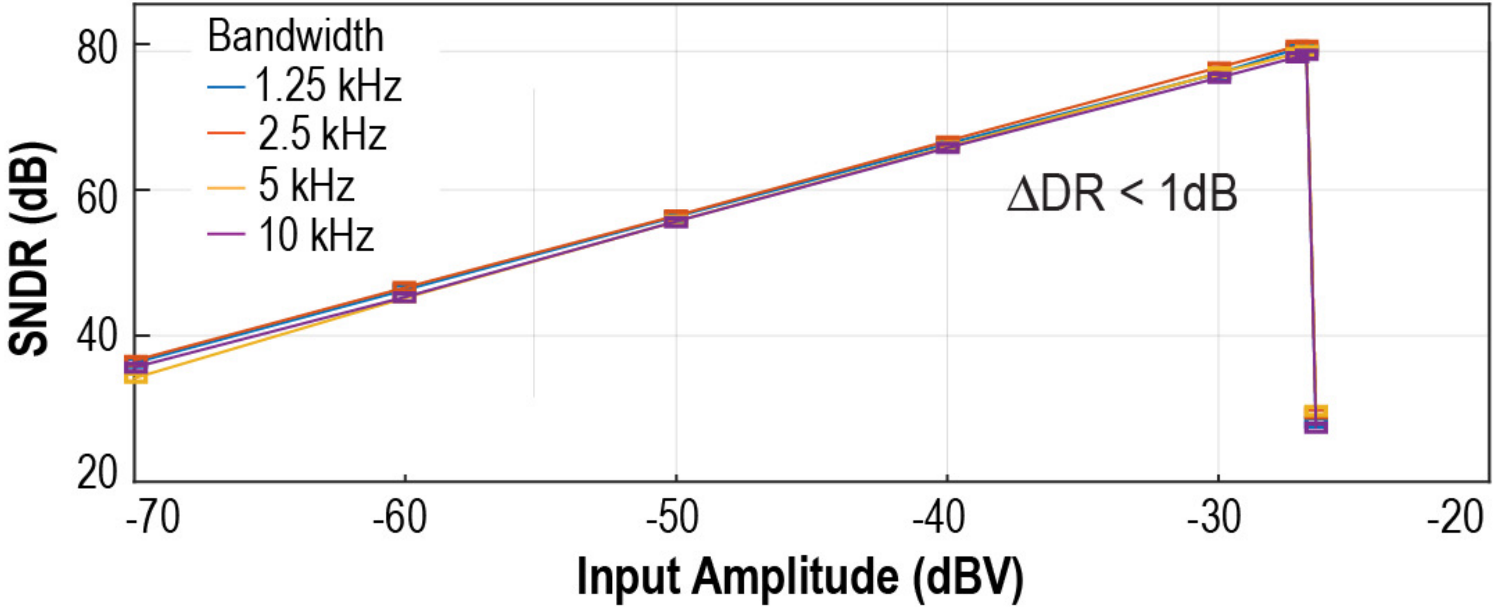


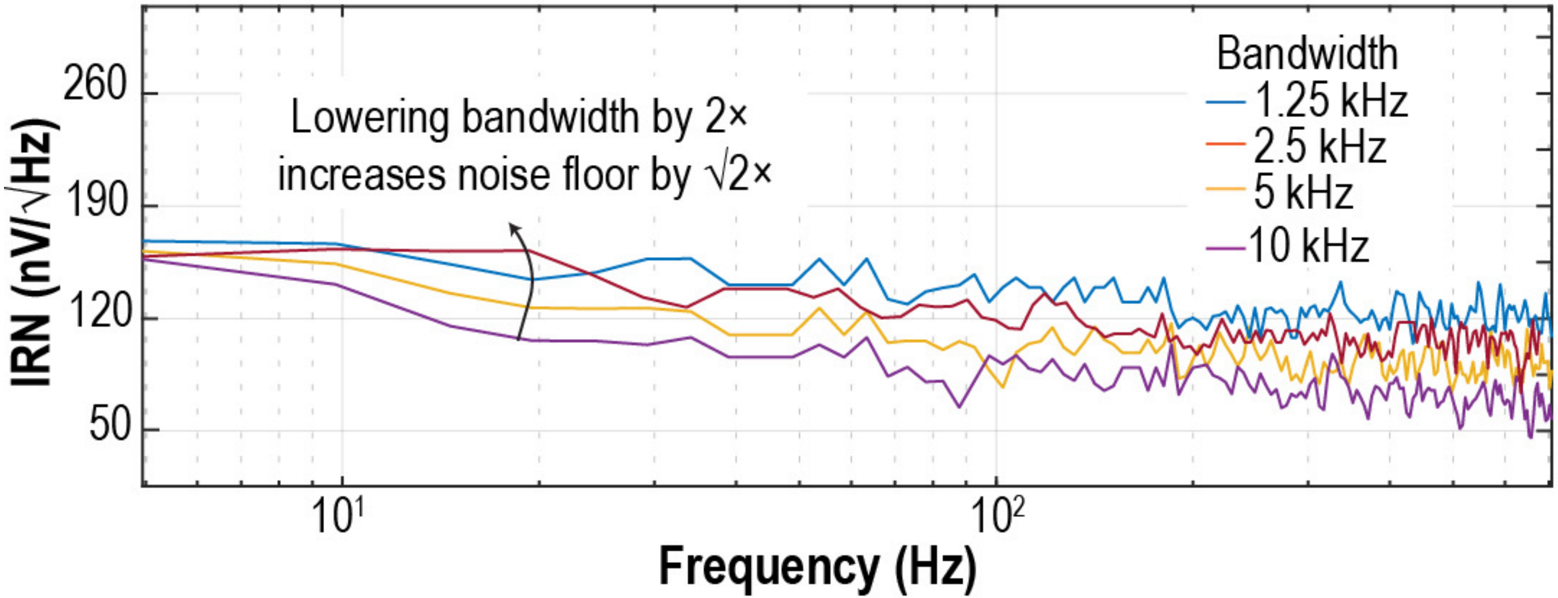
# Measured Spectrum



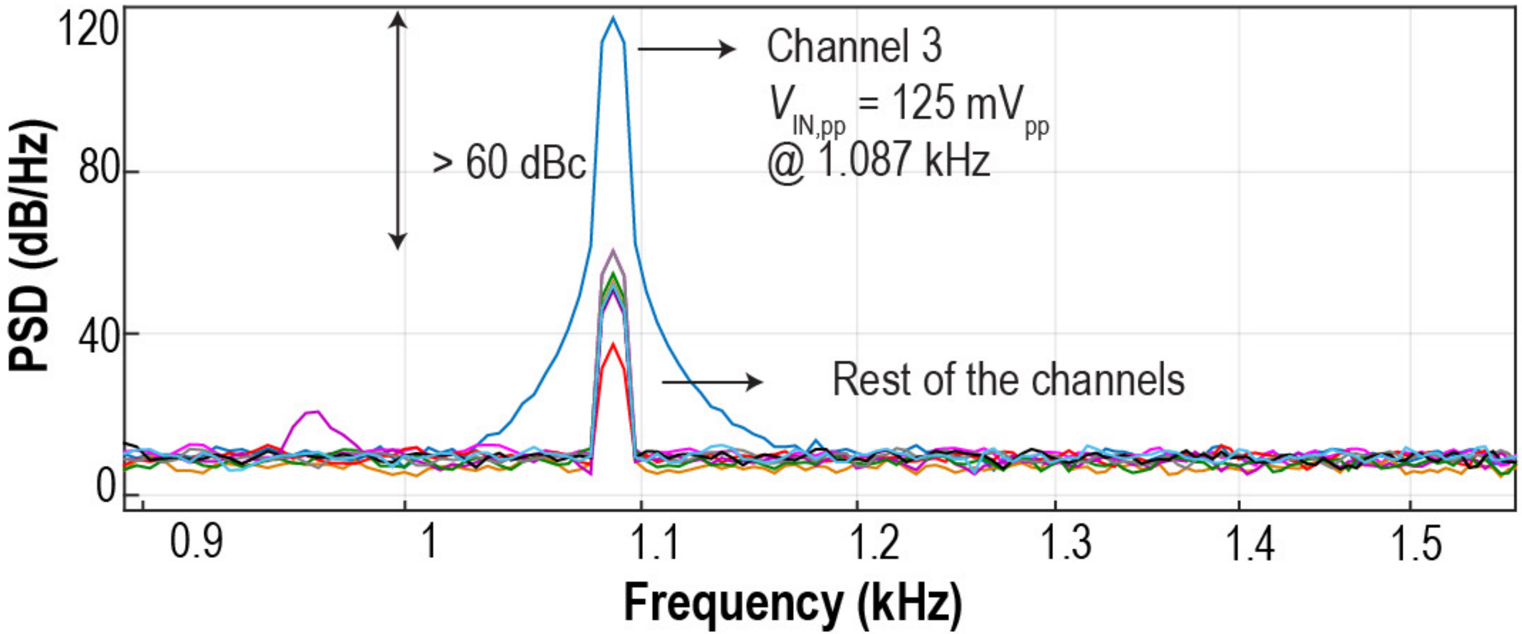
# SNDR vs Input Amplitude



# Input-referred noise

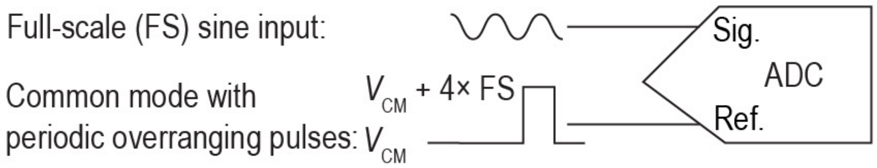


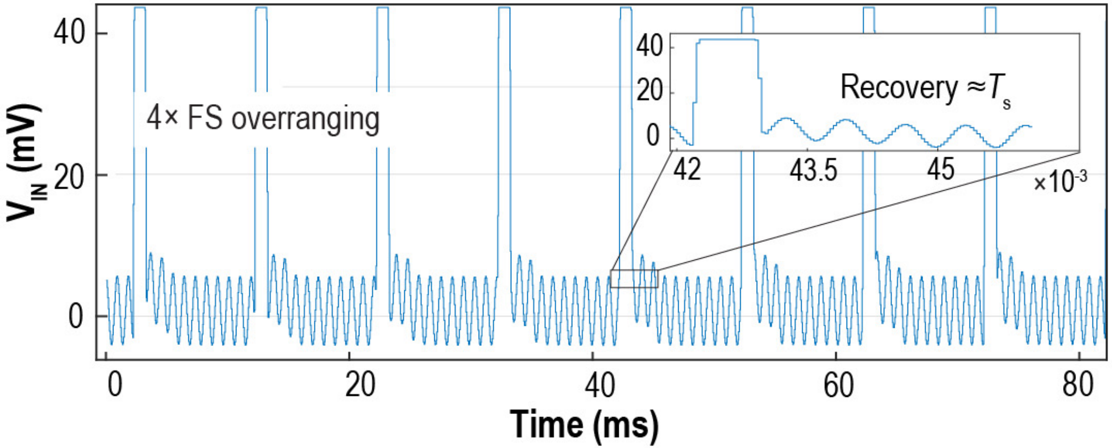
# Crosstalk



120
80
40
0
PSD (dB/Hz)
> 60 dBc
Channel 3
$V_{IN,pp}$ = 125 mV$_{pp}$
@ 1.087 kHz
Rest of the channels
0.9
1
1.1
1.2
1.3
1.4
1.5
Frequency (kHz)

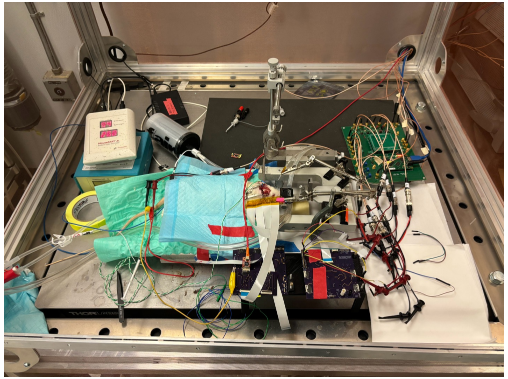
# Artifact Recovery

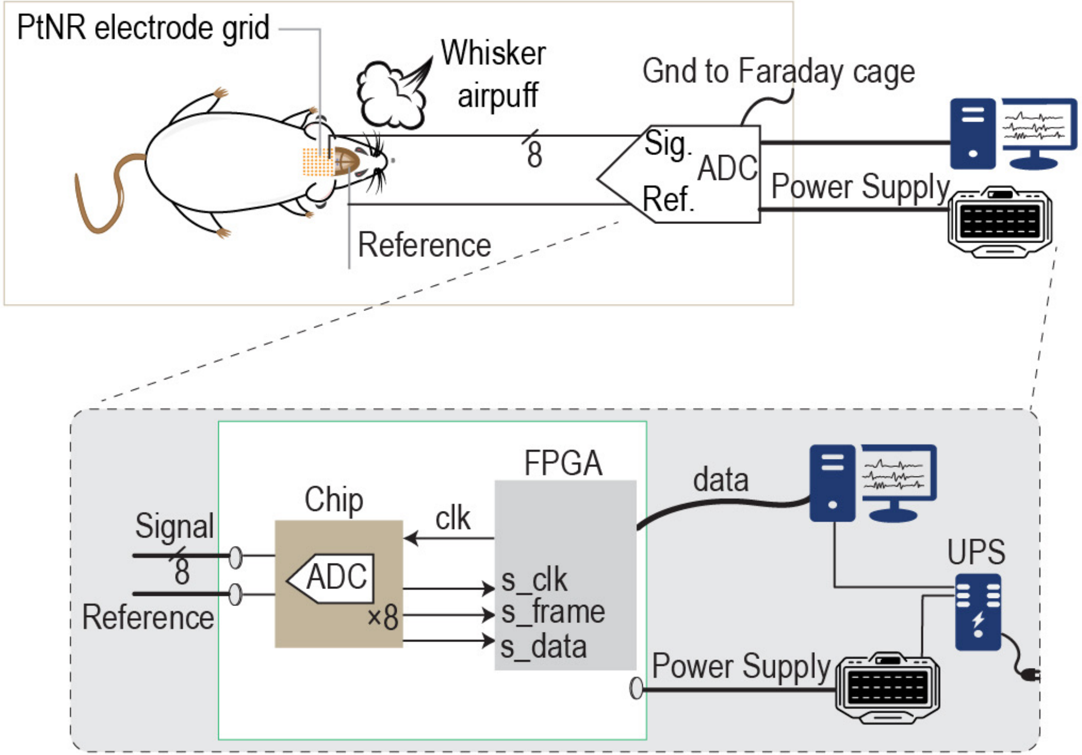



**Artifact recovery is nearly instantaneous, delay determined by decimation filter**

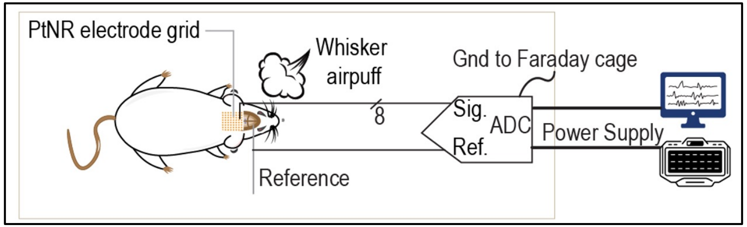
# *in-vivo*: Measurement setup

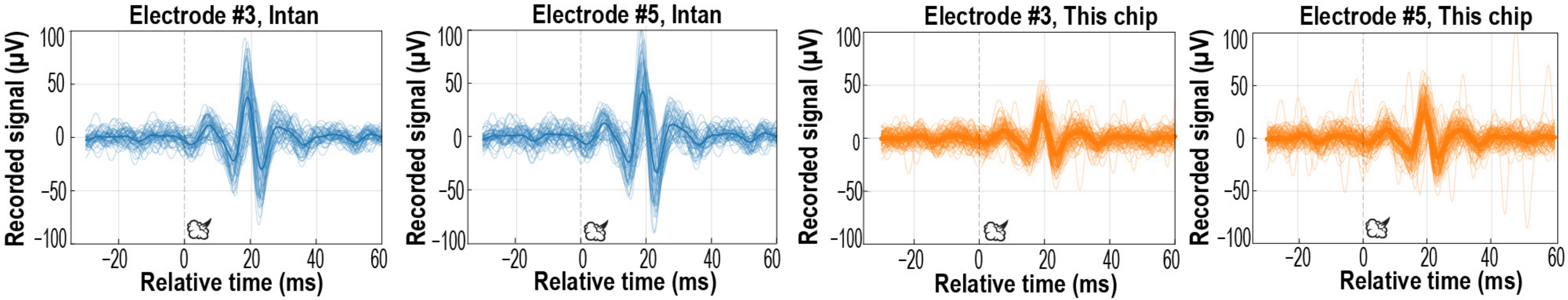




# *in-vivo*: Whisker Airpuff Neural Recording

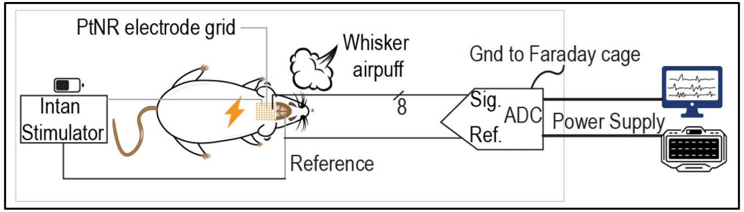
Measurement setup



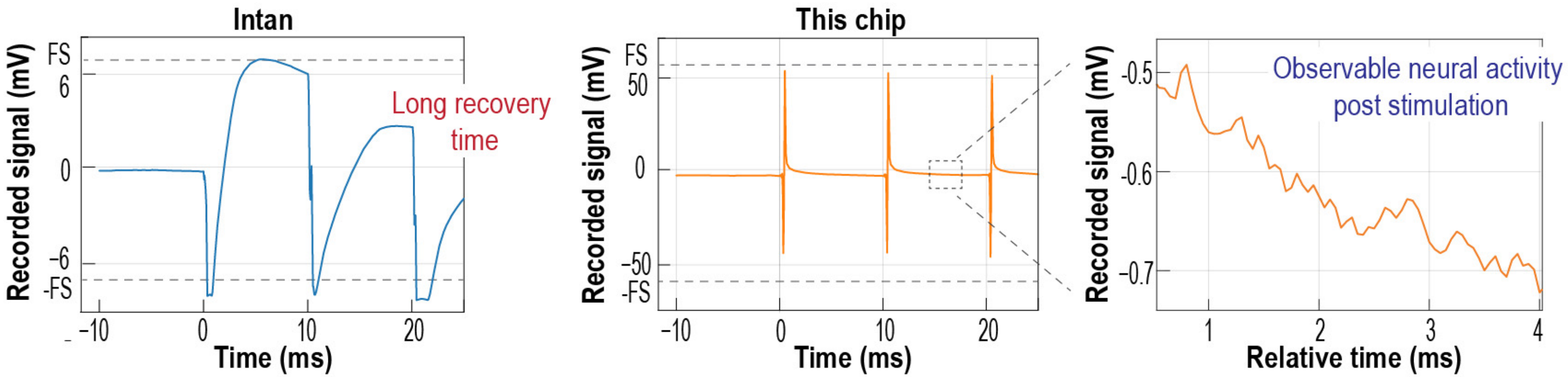



# *in-vivo*: Whisker Airpuff + Stimulation Neural Recordings

Measurement setup




Monopolar stimulation @ 100 Hz with 500 μA (first three pulses shown)



# Performance Summary

| Parameter | RHD 2164 | Lopez TBCAS'17 | Yoon VLSI'21 | C Lee ISSCC'22 | Wendl. ISSCC'21 | X Yang VLSI'22 | **This work** | |
|---|---|---|---|---|---|---|---|---|
| Topology | PGA + shared ADC | | | CT-DSM | | | **CT-DSM** | |
| Input-type | Cap. | Cap. | Cap. | $G_m$ | $G_m$ | Cap. | **Chopped Cap.** | |
| Technology [nm] | 500 | 130 | 65 | 180 | 180 | 22 | **180** | |
| Supply (A/D) [V] | 3.3 | 1.8/1.2 | 2.5 | 1 | 1.8 | 0.8 | **0.9/0.7** | |
| # Channels | 64 | 384 | 1024 | 4 | 8-24 | 128 | **8** | |
| Input FS [$mV_{pp}$] | 10 | 5 | 4.87 | 300 | 7 | 21.5 | **125** | |
| BW [kHz] | 20 | 10 | 10 | 10 | 10 | 10 | **1.25** | **10** |
| Power/channel [µW] | 830 | 49 | 2.72 | 8.6 | - | 3.67 | **3.2** | **11.7** |
| Power/channel with decimator [µW] | - | - | - | - | 8.59 | 6.02 | **3.5** | **14** |
| $FoM_{SNDR}$ [dB]*** | 137 | - | 162.4 | 178.1 | 147 | 157.2 | **163*** | **166*** |
| SFDR [dB] | - | - | - | 94.2 | 62 | 59.49 | **97** | **97.7** |
| IRN [$\mu V_{rms}$] | 2.4 | 6.36 | 8.98 | 6.6 | 4.37 | 7.71 | **5.9*** | **6*** |
| $Z_{IN}$ at DC [MΩ] | ∞ | ∞ | ∞ | ∞ | ∞ | ∞ | **304** | **38** |
| CMRR [dB] | 82 | >60 | 92 | 76 | - | - | **80** | |
| Crosstalk [dBc] | - | 58 | >60 | - | 72 | - | **>60** | |
| Stim. Artifact Tolerance | No | | | Yes | No | | **Yes** | |
| Recovery Time [ms] | >> 100 | | | -** | - | - | **0.4** | **0.05** |

* Averaged over 12 chips  **Unusable beyond input range  ***Schreier FoM [dB] = SNDR + $10\log_{10}$(BW/Power)

# Conclusion

Designed a 4×2 array of per-pixel, power-scalable 2nd-order ΔΣ ADCs for ECoG with in-stimulation recording

Key features:

- Fastest (sub-ms) artifact recovery time through overrange detecting phase quantizer
- Enables in-stimulation recording by avoiding modulator instability
- Power-efficient bandwidth scalable CTDSM tailored for different neural signal frequency bands (2.5-20 kSps)
- Supported by *in vivo* data and comparison with commercial part Intan RHD2164

# Acknowledgements

This work was supported by National Institutes of Health (UG3NS123723).

Thank You!