# A 2-in-1 Temperature and Humidity Sensor With a Single FLL Wheatstone-Bridge Front-End

Haowei Jiang, *Student Member, IEEE*, Chih-Cheng Huang, Matthew R. Chan, *Student Member, IEEE*, and Drew A. Hall, *Senior Member, IEEE*

***Abstract*— This article presents a CMOS 2-in-1 relative humidity (RH) and temperature (Temp) sensor. A single analog front-end (AFE) interfaces two on-chip transducers and converts the resistance ($\propto$ Temp) and capacitance ($\propto$ RH) into a time-based signal. This conversion occurs with high linearity ($\pm$10 ppm error) across the industrial temperature range ($-40$ to $+85$ °C) through a frequency-locked loop (FLL). An incomplete-settling, switched-capacitor-based Wheatstone bridge is proposed to sense the *R* and *C* transducers in a power-efficient fashion. The FLL output is digitized by a low-power, time-to-digital converter (TDC) that has high resolution due to the inherent quantization noise shaping. Implemented in a 0.18-$\mu$m CMOS process, this AFE consumes 15.6 $\mu$W achieving a 2-mK temperature resolution over the industrial temperature range and 0.0073% RH resolution from 10 to 95 %RH. This is the first reported *R*&*C*-to-digital converter (RCDC) with a single, unified AFE and achieves excellent resolution figure-of-merits (FOMs) when normalized to temperature (62 fJ·K$^2$) and RH [0.83 pJ·(%RH)$^2$].**

***Index Terms*— Analog front-end (AFE), capacitance-to-digital converter (CDC), frequency-locked loop (FLL), humidity, sensors, temperature.**

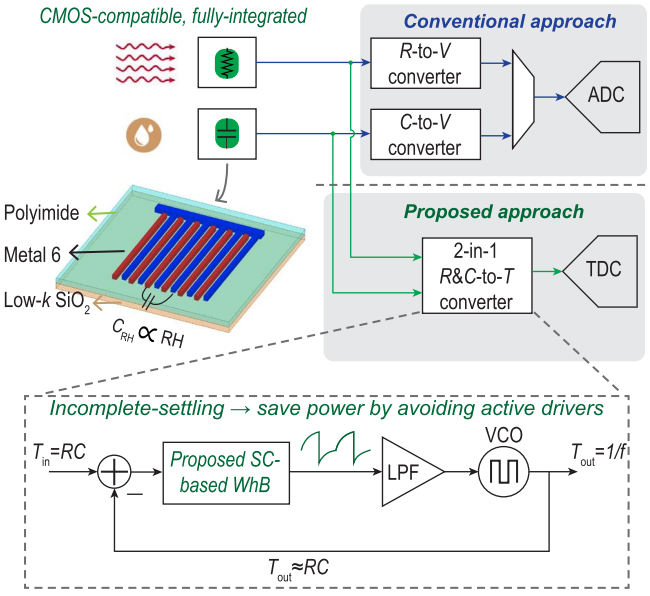


Fig. 1. Architecture of the 2-in-1 temperature and relative humidity sensor.

## I. Introduction

ENVIRONMENTAL monitoring plays a key role in industrial automation and human well-being, comfort, and productivity. For example, environmental data are required in applications ranging from micro-climate control, process control systems [1], [2], storage, and transportation [3], to climate/weather monitoring [4]. Multiple parameters, such as temperature and relative humidity (RH), are often collected together [3]–[6]. Wireless connectivity allows many such sensors to operate both independently and in a networked fashion. Taken together, these devices fit with the recent surge in Internet-of-things (IoT) applications that envision integrating trillions of sensors into one's daily life. However, to achieve such a massive deployment, there are stringent requirements on the sensor's cost, energy efficiency, and size.

A key challenge in this vision is to monolithically combine the sensors in a compact and power-efficient manner as they use fundamentally different transduction mechanisms, and therefore typically require different analog front-ends (AFEs), as shown in Fig. 1. For example, CMOS-compatible temperature sensors use resistors [7]–[12], MOSFETs [13]–[15], or BJTs [16] as the transducer. On the other hand, most RH sensors are based on a capacitive polymer where a moisture-induced dielectric constant change results in a change in capacitance [1], [2], [5], [17], [18]. Among the various polymers that exhibit this property, polyimide (PI) is the most popular because it is already used in CMOS foundries. While it is possible to co-integrate both transducers into a single CMOS chip, prior work has relied on separate AFEs for each transducer (*e.g.*, an instrumentation amplifier for the temperature sensor and a charge amplifier for the RH sensor) with only a few combining the two monolithically [5]. However, using separate AFEs and bias circuits doubles the power, complexity, and cost.

To integrate multiple environmental sensors in a power-efficient way, this article presents a resistive temperature transducer and a capacitive RH transducer combined with

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a 2-in-1 *R&C*-to-digital converter (RCDC) front-end that eliminates the need for two distinct AFEs, as shown in Fig. 1. The RCDC realizes an *R&C*-to-time conversion through a frequency-locked loop (FLL). Compared with prior art with open-loop voltage-controlled oscillator (VCO)-based conversion [19], the FLL suppresses the nonlinearity and process, voltage, and temperature (PVT) variation from the VCO to ensure high-linearity conversion. A highly digital counter-based time-to-digital converter (TDC) samples the FLL outputs in the phase domain and achieves high dynamic range (DR) due to the inherent noise shaping, obviating the need for a conventional voltage domain data converter, such as a $\Delta\Sigma$ modulator (DSM), resulting in lower power and area.

The key block in the loop, the *RC*-based time-to-voltage conversion, is realized by an incomplete-settling, switched-capacitor (SC)-based Wheatstone bridge (WhB). Compared with prior work (*e.g.*, frequency references in [20]–[23] and *C*-sensor in [24]) that drive the SC cell with integrators or low-dropout regulators (LDOs), an active driverless SC-based WhB is proposed to improve the noise and power efficiency. Without an active driver, incomplete settling is inevitable. This work demonstrates that by adding a charge-preserving capacitor, the incomplete-settling SC circuit still exhibits high accuracy (<10 ppm error) and PVT insensitivity at a lower power consumption than prior art. Furthermore, the WhB provides high immunity to supply variation (0.12 °C/V or 0.43 %RH/V) across a wide supply range (1.5–2 V), which is needed in battery-powered IoT devices. The proposed work achieves state-of-the-art RH sensitivity (0.0073 %RH) and high-temperature sensitivity (2 mK) while consuming only 15.6 pJ/meas.—20× lower than commercial RH/temp sensors [25]. It also achieves the best resolution figure-of-merit (FoM) among all compound sensors [5], [18].

The rest of this article is organized as follows: prior resistive and capacitive sensors are reviewed in Section II. The incomplete-settling, SC-based WhB concept is presented and analyzed in Section III followed by the system design in Section IV. Section V presents the circuit implementation followed by the measurement results in Section VI. Conclusions are drawn in Section VII.

## II. Prior R&C Interfaces

### A. R&C Only Interfaces

Resistive sensors are biased in either the voltage [9], [11] or current [26], [27] mode. The best resolution and FoM design uses a WhB-based front-end [11]. The high performance partly stems from the use of two resistive transducers with opposite temperature coefficients (TCs), which increases the transducer sensitivity resulting in a 3.6-dB better FoM compared with using a single transducer. Unfortunately, this interface does not scale to all technology nodes because a negative TC resistor is not always available (*e.g.*, TSMC 65 nm).

A capacitive sensor, often referred as a capacitance-to-digital converter (CDC), combines the capacitive transducer into a charge-redistribution ADC, such as a successive approximation register (SAR) ADC [28], DSM [1], or a hybrid structure [18], [29]. By referencing the capacitive transducer with respect to a capacitor bank, this architecture features high DR, low power consumption, and fast readout time. It should be noted that the conventional resistive sensors and CDCs are architecturally different, and there is no easy way to modify a CDC to support resistive sensing, or vice versa. Thus, it is necessary to develop a new architecture for a combined sensor.

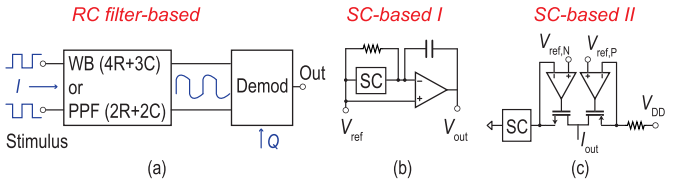


Fig. 2. Examples of prior work that could be used for *R&C* sensing, based on (a) *RC* filter, (b) SC integrator, and (c) SC resistor and LDO.

### B. Combined R&C Interfaces

Although there is no prior work using a unified AFE for both *R&C* sensing, there are *R&C* interfaces that are amenable for combined sensing (*e.g.*, prior temperature sensors [7], [8], [10], [12], [30]–[32], frequency references [21]–[24], [27], [28], and CDCs [24]). These works can be loosely categorized into either *RC*-filter-based or SC-based circuits.

As shown in Fig. 2(a), the *RC*-filter-based circuit typically requires multiple matched (*e.g.*, poly-phase filter (PPF) in [12]) or ratioed (*e.g.*, Wien bridge (WB) in [7], [8], and [10]) capacitors. However, duplicating the RH-sensitive film sensor requires large area (>0.2 $mm^2$) and the process variation is significant [1]. The parasitic capacitance of the floating capacitors and the mismatch result in nonlinear behavior that lowers the $Q$ of the BPF, thus reducing the sensitivity and accuracy. As such, it is less suitable for a *C*-based sensor than an *R*-based sensor. In addition, the inherent nonlinearity of the BPF and phase-domain readout could also be problematic if not taken care of because 1) the transducer's gain error and offset turn into nonlinearity at the output, which cannot be removed with a conventional two-point trim; 2) the sensitivity is maximal at the BPF center frequency and drops if the excitation frequency is misaligned due to PVT variation; and 3) it requires extensive, high-order linearity calibration. Furthermore, the high-voltage swing in the poly-phase-filter and voltage-mode Wien bridge, or the large resistive load in the current-mode Wien bridge complicate the design of a continuous-time readout circuit [8], [10].

An SC-based method is combined with a charge-balancing DSM for readout as shown in Fig. 2(b), where the SC circuit is driven by a closed-loop integrator [20], [23], [24], [35]. This method requires a high-bandwidth, high-output current amplifier to charge and discharge the capacitor during every clock cycle to achieve low settling error (*i.e.* <1/2 LSB). While it avoids the parasitic capacitance, matching, and nonlinearity issues compared with the BPF-based method, an accurate, low-impedance voltage reference is required that adds extra power and noise. An alternative SC-based method shown in Fig. 2(c) uses two matched, LDO-based voltage sources with one driving a resistor and the other a SC resistor that

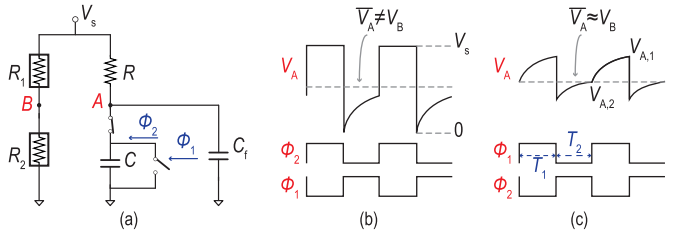


Fig. 3. (a) Schematic of an SC-based WhB and transient waveforms (not to scale) when $f_0 = 1/RC$ with (b) $C_f = 0$ and (c) $C_f \gg C$.

avoids the parasitic capacitance and capacitor matching issues with only one resistor and one capacitor (not floating) [21], [22]. However, it needs two active voltage sources and two references that add noise and power overhead. Recently, the LDO-based voltage sources have been eliminated by connecting the resistor and the capacitor directly in timer designs [33], [34], but the sensitivity and the accuracy are either not shown or compromised. Thus, there is a need for a new *R&C* interface for such RH/temp applications.

## III. Incomplete-Settling SC-Based WhB

To avoid active drivers, this article proposes an SC-based WhB for *R&C* sensing based on the previous SC method but using incomplete settling for power savings. The schematic of the SC-based WhB is shown in Fig. 3(a). In one branch of the WhB, a capacitor $C$ switched at frequency $f_0$ is connected to a voltage source $V_s$ through a series resistor $R$, whereas the other branch has two matched resistors in series. A shunt capacitor $C_f$ is placed at node $A$. It should be noted that unlike the well-known SC resistor where the charge transfer function is based on complete-settling, $V_A$ does not settle completely to $V_s$ due to the large $RC$ time constant relative to $f_0$. Therefore, the SC resistance equation (*i.e.* $R = 1/f_0C$) does not hold. To see this, assume $C_f = 0$, which results in the $V_A$ waveform shown in Fig. 3(b). $V_A$ is held at $V_s$ for during $\Phi_2$ because there is no path from node $A$ to ground; while $V_A$ exponentially increases from 0 during $\Phi_2$. When the bridge is balanced (*i.e.* the average output voltage equals zero), the SC must be clocked at

$$f_0 = \frac{(1+e)D}{e}\frac{1}{RC} \tag{1}$$

where $e$ is the base of the natural logarithm and $D$ is the clock duty cycle. With $D = 50\%$, $f_0 = 0.684/RC$—demonstrating that due to incomplete settling, the SC should be clocked slower than the fully settled case. If the switches are still clocked at $f_0 = 1/RC$, $\overline{V_A}$ settles below $V_B$ and the bridge is not balanced, as shown in Fig. 3(b). Like all incomplete-settling circuits, the settling error depends on the settling time and time constant, therefore $D$ and the parasitic capacitance at node $A$. As a result, although the error is deterministic, it is sensitive to the clock phase error and the parasitic capacitance, which is inevitable when connecting a readout circuit to the WhB output. Due to its susceptibility to phase noise and parasitic capacitance (consequently PVT variation), this SC-based WhB cannot be used directly as the $RC$ sensor front-end when $C_f$ is small.

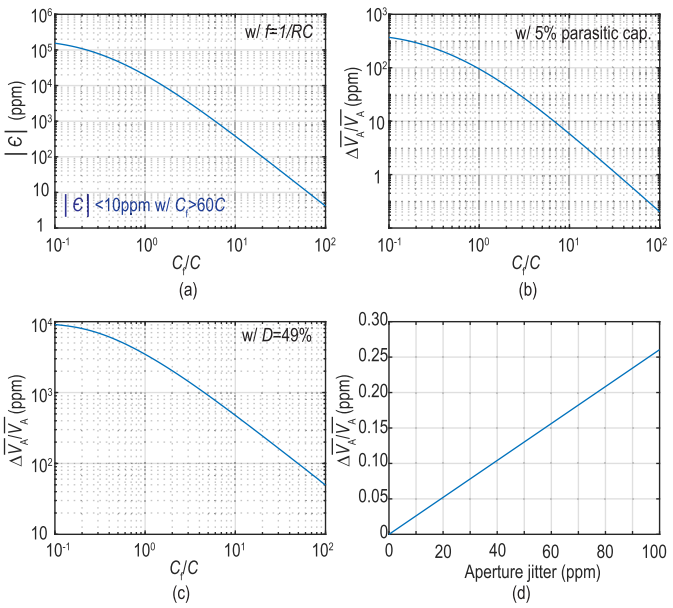


Fig. 4. Simulated (a) $|\epsilon|$ versus $C_f/C$, (b) WhB output change versus $C_f/C$ with 5% parasitic capacitance, (c) WhB output change versus $C_f/C$ with 49% duty cycle, and (d) WhB output with a clock phase error.

Instead of building a power-hungry circuit to minimize the settling error, a passive method is proposed using $C_f$. With proper sizing, the settling error can be minimized where $C_f$ essentially functions as a passive integrator. During $\Phi_2$, $C$ extracts charge from $C_f$ through charge sharing, which bypasses the slower path through $R$. During $\Phi_1$, $C$ discharges completely. Meanwhile, the lost charge on $C_f$ during $\Phi_2$ is supplemented from $V_s$ through $R$. If $C_f$ were infinitely large, node $A$ would stabilize to a constant voltage, like the virtual ground of an active integrator. With low enough switch on-resistance, $C$ settles completely to that constant voltage during $\Phi_2$, and its effective resistance is $1/f_0C$. Obviously, $C_f$ cannot be sized infinitely large due to the area, bandwidth, and start-up time constraints. To find the appropriate value for $C_f$, a time-domain analysis was done in our prior work [36]. The waveform at $V_A$ and the two-phase clock are shown in Fig. 3(c). The voltage at node $A$ at the end of the two clock phases, $V_{A,\Phi1}$ and $V_{A,\Phi2}$, is

$$V_{A,\Phi1} = V_s + (V_{A,2} - V_s)e^{-\frac{T_1}{RC_f}} \tag{2}$$

$$V_{A,\Phi2} = V_s + \left(\frac{C_f}{C+C_f}V_{A,1} - V_s\right)e^{-\frac{T_2}{R(C_f+C)}} \tag{3}$$

where $T_1$ and $T_2$ are the period of the two phases. During each cycle, the charge $Q$ being transferred is $CV_{A,2}$. Therefore, the average voltage at node $A$ is

$$\overline{V_A} = V_s - \frac{RQ}{T_1+T_2} = V_s - RQf_0. \tag{4}$$

With $D = 50\%$ and negligible deadzone between the two clock phases, substituting (2) and (3) into (4) with $f_0 = 1/RC$

$$\overline{V_A} = (1+\epsilon)\frac{1}{1+f_0RC}V_s \approx \frac{1}{1+f_0RC}V_s \quad \text{where}$$

$$\epsilon = 1.5\left(1 - \frac{1}{\frac{C_f+C}{C}e^{\frac{C}{C+C_f}} - \frac{C_f}{C}e^{-\frac{C}{C_f}}}\right) - 1. \tag{5}$$

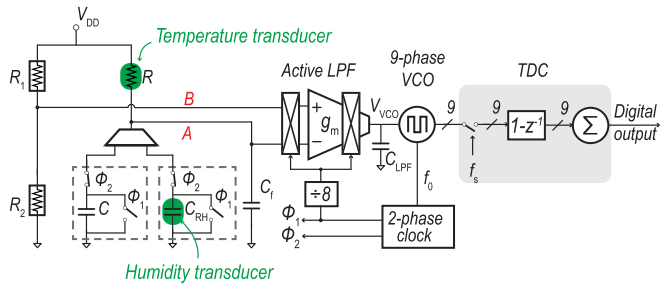


Fig. 5. System schematic of the RH/temp sensor using an RCDC.

Equation (5) shows that on average, node $A$ is the output of a voltage divider between an $R$ and SC resistor whose resistance is approximately $1/f_0C$ where $\epsilon$ is a parameter that evaluates the error, which depends on the ratio of $C_f/C$. As the ratio goes to infinity, $\epsilon$ approaches zero, which endorses the intuitive explanation. The calculated $\epsilon$ versus the $C_f/C$ ratio is plotted in Fig. 4(a), which can be used as a guidance how to choose $C_f$. For instance, $C_f$ should be greater than $60C$ to make the error negligible ($<$10 ppm) in this application. A large $C_f$ also attenuates the susceptibility to parasitic capacitance [Fig. 4(b)] and clock duty cycle [Fig. 4(c)]. In addition, this circuit is insensitive to the clock phase error; $\overline{V_A}$ deviates less than 0.3 ppm when the aperture jitter is 100 ppm [Fig. 4(d)]. The linear curve also suggests that even if there is a small linear phase error over temperature, the induced WhB output error is still linear. Therefore, the proposed approach robustly fixes the incomplete-settling issue in a passive manner. In contrast, without $C_f$ power-hungry active drivers are required to achieve the same result. Adding $C_f$ ($=60C$) improves the accuracy by $\sim$5200$\times$ without a power penalty in steady state. Note that the benefits of the incomplete-settling circuit are severely diminished if $C_f$ is not large enough as the error nonlinearly depends on $R$, $C$, and $C_f$. Thus, unlike an offset or a gain error, it cannot be removed with a linear calibration.

Compared with prior $RC$-based front-ends, this technique has several benefits, namely: 1) high linearity due to the passive settling error reduction; 2) inherent supply rejection due to the WhB structure; 3) insensitivity to the parasitic transducer capacitance and $C_f$ variation. Thus, $C_f$ can be implemented with a MOS capacitor; and 4) due to incomplete settling and large $C_f$, the swing at $V_A$ is $<$10 mV, relaxing the readout circuit linearity requirement. Switching imperfections (*e.g.*, clock feedthrough and charge injection) are attenuated by $C_f$.

## IV. System Design

### A. System Architecture

The preceding analysis shows that if the bridge is balanced (*i.e.* $\overline{V_{AB}} = 0$ V), the $R$ and $C$ information can be read out from the clock frequency. To that end, an FLL is built around the SC-based WhB to drive the bridge into the balanced condition. As shown in Fig. 5, two SC cells are connected to the bridge through a multiplexer where a silicided poly-resistor is used for temperature sensing and a PI film capacitor $C_{RH}$ for humidity sensing. A metal–insulator–metal (MIM) capacitor $C$ is used as a reference. As discussed in detail later, a 330-k$\Omega$ resistor (at room temperature) and 4-pF capacitors were chosen resulting in a nominal output frequency of $\sim$758 kHz, to optimize for power, sensitivity, and area. $C_f$ is $\sim$240 pF given the 60$\times$ ratio requirement. The WhB is driven directly by the supply (*i.e.* $V_s = V_{DD}$), departing from prior low-power timer works that implemented a separate voltage source [33], [34]. This maximizes the sensitivity and linearity while avoiding an additional noise source, as explained later.

$V_{AB}$ is amplified and filtered to attenuate ripple by an active low-pass filter (LPF). Chopping is used to remove temperature-dependent offset and the amplifier's $1/f$ noise. A VCO converts the LPF output voltage $V_{VCO}$ into $f_0$, with a nominal period of $t_0$. Because it is a linear signal transfer function (STF) from the RH/temp to $t_0$, $t_0$ instead of $f_0$ is taken as the output of the FLL. A two-phase non-overlapping clock generator closes the loop by feeding back the frequency to the SC cells in the WhB. The FLL output during the temperature and RH measurement modes is

$$t_{Temp} = RC \text{ and } t_{RH} = RC_{RH}. \tag{6}$$

The AFE measures temperature and RH in a time-multiplexed manner by selecting between $C_{RH}$ and $C$. Using the results from both the modes, the temperature dependence on the RH measurement is removed. To mitigate the cross-sensitivity, the AFE needs to re-settle fast enough to have the temperature be regarded as constant in the two measurements.

The 9-b VCO outputs are digitized by a counter-based TDC. By continuously digitizing, the TDC has first-order noise shaping [37], [38]. The TDC is clocked by an external frequency reference, $f_s$. Thus, the RH/temp information (*i.e.* $R$ and $C_{RH}$) are digitized with respect to $C$ and $f_s$.

### B. Dynamic Analysis

Aside from the settling error described in Section III, the finite loop gain of the FLL also affects the accuracy and linearity. Furthermore, the FLL dynamics require careful analysis to ensure stability over PVT variation. Thus, a small-signal model of the FLL is derived.

Assuming $C_f$ is large, the SC cell can be treated as a clock period-controlled resistor. Thus, the small-STF of the period-to-voltage conversion, $H_{WhB}(s)$, is derived by taking the derivative of the large-signal relationship within the SC-based WhB (assuming it is balanced)

$$H_{WhB}(s) = \frac{\partial}{\partial t_0}\left(\frac{V_{DD}}{1+CR/t_0}\right)\frac{1}{1+s\frac{RC_f}{2}} = \frac{V_{DD}}{4t_0}\frac{1}{1+s\frac{RC_f}{2}}. \tag{7}$$

Equation (7) indicates that the balanced SC-based WhB has a dc gain of $K_{WhB} = V_{DD}/4t_0$ and a pole at $\omega_{WhB} = -2/RC_f$. Similarly, the $R$- and $C$-to-voltage transfer functions are

$$\begin{aligned} H_{WhB,R2V}(s) &= Ct_0^2 H_{WhB}(s) \\ H_{WhB,C2V}(s) &= Rt_0^2 H_{WhB}(s). \end{aligned} \tag{8}$$

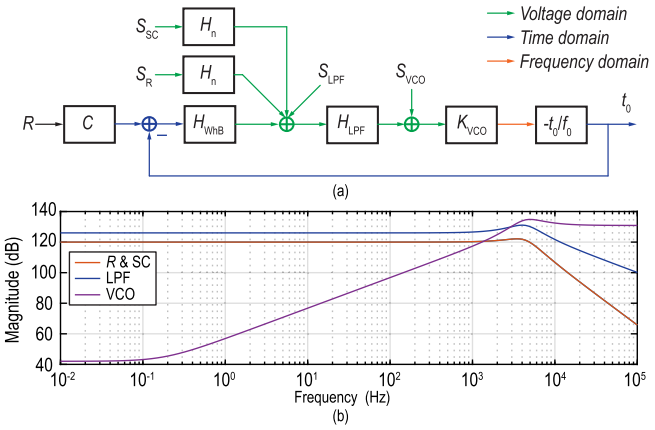


Fig. 6. (a) FLL block diagram and (b) NTFs of the different blocks.

The first-order active LPF can be modeled by

$$H_{\mathrm{LPF}}(s) = -A\frac{1}{1+\frac{s}{\omega_{\mathrm{LPF}}}} \tag{9}$$

where $A$ and $\omega_{\mathrm{LPF}}$ are the active LPF dc gain and pole, respectively. The VCO gain is $K_{\mathrm{VCO}}$, defined in Hz/V. Because the oscillation period is taken as the VCO output, the small-signal VCO voltage-to-period gain is

$$H_{\mathrm{VCO}}(s) = -\frac{t_0}{f_0}K_{\mathrm{VCO}}. \tag{10}$$

Combing the transfer functions derived above, the FLL block diagram for the temperature mode is obtained, as shown in Fig. 6(a). The loop gain is

$$L(s) = \frac{AK_{\mathrm{VCO}}V_{\mathrm{DD}}}{4f_0}\frac{1}{\left(1+\frac{s}{\omega_{\mathrm{LPF}}}\right)\left(1+\frac{s}{\omega_{\mathrm{WhB}}}\right)}. \tag{11}$$

This analysis shows that the FLL is a second-order system. By choosing $\omega_{\mathrm{LPF}}$ as the dominant pole, the active LPF requires lower bandwidth, power consumption, and integrated noise from the transducers and LPF, at the expense of larger area. Alternatively, pushing $\omega_{\mathrm{LPF}}$ to the non-dominant pole allows higher FLL bandwidth and has smaller area, but requires higher power to extend the active LPF bandwidth and suffers from worse linearity due to higher ripple at $V_{\mathrm{VCO}}$. Because this work is targeting IoT applications, the former is adopted. The gain error is inversely proportional to $L(s=0)$, and thus higher supply voltage, LPF dc gain, and VCO gain result in lower error. This justifies the design choice of using an active LPF with high dc gain and biasing the WhB directly from $V_{\mathrm{DD}}$ to maximize the loop gain.

### C. Sensitivity Analysis

Aside from the SC settling and loop gain errors, the noise affects the sensitivity and thus the inaccuracy. To quantify this, the STF and noise transfer function (NTF) from each block are analyzed. As derived from the block diagram shown in Fig. 6(a), the STFs are

$$\begin{aligned}\mathrm{STF}_{\mathrm{Temp}} &= \alpha t_0\frac{L(s)}{1+L(s)} \approx \alpha t_0\\ \mathrm{STF}_{\mathrm{RH}} &= \beta t_0\frac{L(s)}{1+L(s)} \approx \beta t_0\end{aligned} \tag{12}$$

where $\alpha$ and $\beta$ are the resistor's TC and the capacitor's RH coefficient, respectively.

The noise from the $R$ or SC can be modeled as a voltage noise source in series with a noiseless $R$ or SC. When the WhB is balanced, the noise power spectral density (PSD) from $R$ and SC is equal, $S_{\mathrm{R,SC}} = 4k_{\mathrm{B}}\mathrm{TR}$ where $k_{\mathrm{B}}$ is Boltzmann's constant and $T$ is the temperature. Both noise sources pass through the same transfer function, $H_{\mathrm{n}}(s)$ and sum at the WhB output where

$$H_{\mathrm{n}}(s) = \frac{1}{2\left(1+\frac{s}{\omega_{\mathrm{WhB}}}\right)}. \tag{13}$$

The noise from the reference branch can be made negligible if the reference branch output's bandwidth is limited.

The input-referred noise PSDs of the active LPF and VCO are $S_{\mathrm{LPF}}$ and $S_{\mathrm{VCO}}$, respectively. With that, the NTFs are

$$\begin{aligned}\mathrm{NTF}_{\mathrm{R}} &= \mathrm{NTF}_{\mathrm{SC}} = \frac{2t_0}{V_{\mathrm{DD}}}\frac{L(s)}{1+L(s)}\\ \mathrm{NTF}_{\mathrm{LPF}} &= \frac{H_{\mathrm{LPF}}(s)K_{\mathrm{VCO}}}{1+L(s)}\\ \mathrm{NTF}_{\mathrm{VCO}} &= \frac{K_{\mathrm{VCO}}}{1+L(s)}.\end{aligned} \tag{14}$$

The Bode plots of the NTFs are shown in Fig. 6(b). $\mathrm{NTF_R}$ and $\mathrm{NTF_{SC}}$ roll off at 40 dB/dec, while $\mathrm{NTF_{LPF}}$ rolls off at 20 dB/dec. The noise from the VCO is attenuated by the LPF gain within the open-loop bandwidth and increases by 20 dB/dec afterward. It should be noted that all noise sources are uncorrelated.

If the noise from the WhB is dominant, by substituting the noise PSD from the $R$ and SC resistor in (14), and then input-referring it with (12), the PSD (normalized to the temperature input) can be obtained. Because the TDC output is decimated by a sinc filter of length $T_{\mathrm{conv}}$, the rms temperature noise (*i.e.* the temperature sensitivity $\Delta T$) is

$$\Delta T \approx \sqrt{2\frac{S_{\mathrm{R}}}{2T_{\mathrm{conv}}}\left|\frac{\mathrm{NTF_R}}{\mathrm{STF}}\right|^2} = \frac{4}{\alpha V_{\mathrm{DD}}}\sqrt{\frac{k_{\mathrm{B}}\mathrm{TR}}{T_{\mathrm{conv}}}}. \tag{15}$$

Similarly, the RH sensitivity, $\Delta$RH, is

$$\Delta\mathrm{RH} \approx \frac{4}{\beta V_{\mathrm{DD}}}\sqrt{\frac{k_{\mathrm{B}}\mathrm{TR}}{T_{\mathrm{conv}}}}. \tag{16}$$

Upon reaching steady state, the WhB power consumption is

$$P_{\mathrm{WhB}} = \frac{V_{\mathrm{DD}}^2}{2R} \tag{17}$$

where the power consumption in the reference branch is negligible (shown later). Substituting (15) and (17) into the temperature sensor FoM equation, the WhB front-end FoM is

$$\mathrm{FoM_{WHB}} = \frac{P_{\mathrm{WhB}}}{T_{\mathrm{conv}}}\Delta T^2 = \frac{8k_{\mathrm{B}}T}{\alpha^2}. \tag{18}$$

In practice, the LPF, VCO, and TDC also contribute noise that degrades the sensitivity while consuming a non-negligible power. So, the sensitivity, power, and following FoM will be worse than in (15)–(18). Nevertheless, a few observations can be made from the above analysis. Namely,

1) Both the sensitivity and FoM are inversely proportional to the transduction coefficient (*i.e.* TC and RH coefficients, $\alpha$ and $\beta$, respectively). Thus, the transducers should be carefully selected to maximize the performance.
2) Increasing the supply voltage linearly improves the sensitivity. The WhB power consumption is proportional to $V_{\mathrm{DD}}^2$, while the power consumption of most other analog blocks (*e.g.*, the amplifier) with a static bias current is proportional to $V_{\mathrm{DD}}$. This suggests that even though the FoM of the WhB alone does not improve as $V_{\mathrm{DD}}$ increases, the overall energy efficiency does when the power of the other blocks is considered.
3) Making the WhB fully differential doubles the signal and the sensitivity increases by 3 dB at the cost of doubling the WhB power consumption. Although (18) does not improve, the 2× signal swing reduces the NTFs allowing 4× lower power consumption from the LPF and VCO if they are noise-limited. The fully differential architecture also removes the reference branch, which needs a decoupling capacitor. Furthermore, it cancels switch imperfections. Therefore, a fully-differential SC-WhB would be preferable. A pseudodifferential WhB is adopted in this design because matching two postprocessed RH transducers is very difficult.

## V. Circuit Implementation

### A. Transducers

As shown in the previous analysis, a resistor with high $\alpha$ is preferred. Apart from that, other physical parameters that affect the resistor nonideality should be considered. For example, the second-order TC, voltage dependence, and stress sensitivity affect the sensor nonlinearity, which cannot be corrected by a simple first-order trim. The $1/f$ noise leads to excess noise and worse sensitivity compared with (15) and (16). The sheet resistance determines the required area. In this article, a silicided P-type polysilicon resistor is chosen due to its high $\alpha$ (∼2980 ppm/°C), high linearity (*i.e.* low second-order TC and low-voltage coefficient), and low $1/f$ noise corner (<1 Hz). To achieve 1-mK temperature resolution in a 1-ms conversion time, the resistor value is chosen as 330 kΩ according to (15). Note that because $\alpha$ is technology-dependent, better sensitivity could be achieved if a higher $\alpha$ resistor is available.

The RH transducer is implemented with a metal finger capacitor coated with a PI film (PI-2545). The relative dielectric constant, $\varepsilon_{\mathrm{PI}}$, is 3.4 at ∼35 %RH. The transducer geometry, to the first-order, does not affect $\beta$ but affects the area, coating difficulty, and response time. For an $N$ finger interdigitated capacitor with finger length $L$, gap width $W$, and metal thickness $H$, the total capacitance can be modeled as

$$C = \varepsilon_{\mathrm{PI}}\varepsilon_0(N-1)\frac{LH}{W} \tag{19}$$

where $\varepsilon_0$ is the vacuum permittivity. To minimize the area, $H$ should be maximized, while $W$ should be minimized. Thus, the geometry parameters are chosen as follows: $N = 80$, $H = 40\ \mu$m, $L = 220\ \mu$m, and $W = 2.5\ \mu$m. This geometry results in a capacitance of ∼4 pF, which is confirmed through simulation in Ansys HFSS. The capacitor value is a compromise between area and power: a smaller $C_{\mathrm{RH}}$ (consequently, smaller $C_{\mathrm{f}}$ and active loop filter) leads to higher $f_0$ and thus larger dynamic power. In this article, a relatively large $C_{\mathrm{RH}}$ is chosen because power consumption is the primary concern. It can be modified with a smaller $C_{\mathrm{RH}}$ in a more area constrained design due to the scalability of the FLL-based time-domain readout. The top-metal capacitor is designed to have an opening without passivation to allow for post-processing. The transducer bottom plate is shielded by the overlaying metal layers that connect to ground. This protects from over etching and reduces the parasitic capacitance associated with the top plate, which connects to the switches. As for the reference capacitor, an MIM capacitor with ∼10 ppm/°C is used. Both the MIM capacitor and the silicided polysilicon resistor are not exposed to the air, thus showing no humidity dependence.

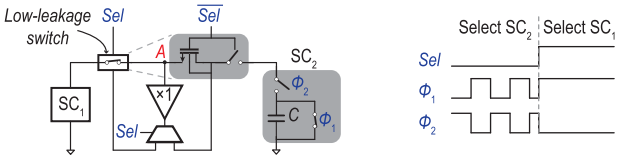


Fig. 7. Schematic and timing of the high-isolation multiplexer scheme.

### B. SC Front-End

The reference branch of the WhB is implemented by 4× series diode-connected PMOS transistors. The static current is ∼50 nA at room temperature. The transistors are configured in a common-centroid layout and have their bulk tied to the source to mitigate mismatch and the body effect. It should be noted that even if there is mismatch between the transistors, as long as the mismatch is constant over temperature (a 200-run Monte Carlos simulation shows $R_1/R_2$ vary $< \pm 0.1\%$ over the temperature range), it only manifests as a gain error, which is removed by a first-order calibration as described in Section VI. The noise of the reference branch can be limiting. On-chip, the reference noise bandwidth is limited to 10 Hz, which is insufficient for near-dc environmental sensing. An off-chip 20-nF capacitor was added to aggressively bandlimit the reference noise to ∼10 mHz to make its noise contribution negligible.

The switches in the multiplexer require extra attention. While the switch should have a low on-resistance to not affect the accuracy of $R$, it should also have good isolation between the two SC cells. To achieve this, the multiplexer switches are implemented with NMOS low-leakage switches (*i.e.* using a unity-gain buffer to drive the intermedia node of two series switches and the body of the switch when the switch is off, as in [39]). The unity-gain buffer does not require high bandwidth to cover $f_0$, because the ripple at $f_0$ is less than 5 mV. The residual leakage is negligible, even if there is residual offset due to the low bandwidth. The two switches in the multiplexer share one buffer in a time-multiplexed fashion to minimize the power consumption. In addition, the SC cell is designed to stay in $\Phi_1$ when it is not selected (Fig. 7),

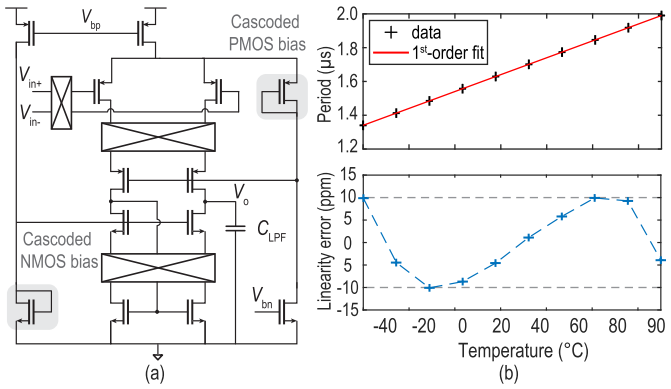


Fig. 8. (a) Schematic of the active low-pass filter and (b) simulated FLL transfer curve and linearity error.

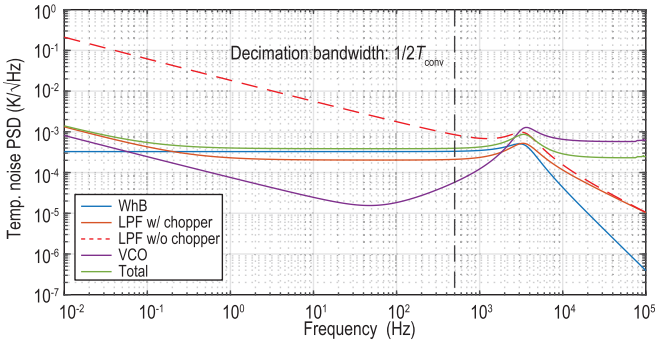


Fig. 9. Simulated FLL noise PSD referred to the temperature input.

such that the un-selected capacitor (either MIM or PI film) is shorted to ground to further reduce the crosstalk. In simulation, the crosstalk is negligible (<5 ppm error when the un-selected capacitor changes by 20%).

### C. Chopper-Stabilized Active Filter

As analyzed in Section IV, the active LPF needs to have high enough dc gain to achieve high system linearity and low gain error, and low $\omega_{\mathrm{LPF}}$ to maintain the FLL stability. Compared with prior work with phase-domain DSM readout, the active LPF has low-voltage swing at both the input and the output, which relaxes the linearity requirement. Thus, instead of using a closed-loop filter, an open-loop $g_m$-$C$ architecture is used.

The required dc gain can be obtained from (11) where, assuming the system undergoes 30% supply variation (a typical value for a battery) and the normalized VCO gain ($K_{\mathrm{VCO}}/f_0$) varies between 3 and 5, the dc gain should be $>$ 79 dB to achieve $\lessdot\pm$10 ppm nonlinearity error. Thus, a telescopic architecture is adopted in the $g_{\mathrm{m}}$ cell [Fig. 8(a)]. Compared with a two-stage or folded-cascode architecture, it has better noise efficiency. The input pair is implemented with PMOS transistors for two reasons: 1) PMOS transistors have a lower $1/f$ noise corner in this process and 2) PMOS transistors have a higher threshold voltage than NMOS such that the input pair is always in subthreshold, which has the optimal noise efficiency, across PVT variation. With a 1.5-V supply voltage, the PMOS input pair is biased in subthreshold saturation, while the NMOS load is biased in above-threshold saturation with a high overdrive voltage, such that the transistor's thermal noise is attenuated. This also results in at least 400-mV output swing, which covers the expected VCO tuning range and frequency drift due to PVT variation. The dc gain is nominally 84 and $>$79 dB across process corners and temperatures. With such high gain, the FLL transfer curve is simulated using an ideal resistor with $\alpha = 3000$ ppm/°C in the transistor-level interface, and the nonlinearity error is $< \pm 10$ ppm from $-40$ to 85 °C. Simulation shows the nonlinearity (mainly from $g_m$ cell and VCO) is attenuated by the FLL loop gain successfully. To maintain stability and fast step response, the closed-loop bandwidth in (12) needs to be lower than 4 kHz (because the non-dominate pole is at $\omega_{\mathrm{WhB}}$). Simulation shows that $C_{\mathrm{LPF}}$ needs to be 3.5 nF to achieve this over PVT variation. This also attenuates the switching ripple to $\sim$20 $\mu$V. It is implemented with a stacked MOS capacitor, custom metal–oxide–metal (MOM) capacitor using stacked metals (metal layers 1–5), and high-density MIM capacitor to maximize the density. In total, a 6-nF capacitor bank is implemented on chip, but only 3.5 nF is connected during the measurement, which occupies 0.29 mm$^2$.

The $g_{\mathrm{m}}$ cell is chopped to remove its $1/f$ noise and offset, which is temperature-dependent and introduces nonlinearity. The up-modulation chopper is placed at the input, and the down-modulation choppers are placed at the cascode nodes, which have $\sim$100$\times$ lower impedance and higher bandwidth than the output nodes. Thus, the down-modulated signal settles faster and creates less settling error. The up-modulated $1/f$ noise and offset are filtered by $C_{\mathrm{LPF}}$. The chopper clock is the FLL output divided by 8. By synchronizing the chopping clock to the SC clock (and therefore the signal), spurious tones due to the intermodulation between the chopping and SC operation are avoided. The divider ratio is chosen to be 8 such that the nominal chopper frequency (94 kHz) is slightly higher than the simulated $g_{\mathrm{m}}$ cell $1/f$ noise corner frequency ($\sim$60 kHz). The clock division also relaxes the $g_{\mathrm{m}}$ cell bandwidth requirement accordingly, which enables an 8$\times$ power savings. As shown in Fig. 9, chopping reduces the $1/f$ noise corner to $<$1 Hz and attenuates the integrated noise by 26 dB. The simulated noise PSD is 0.3 nV/$\sqrt{\mathrm{Hz}}$, corresponding to 0.19 mK/$\sqrt{\mathrm{Hz}}$, 5 dB lower than the WhB noise PSD. Therefore, the total FLL noise PSD (green curve) is dominated by the WhB noise contribution (blue curve). The noise efficiency factor, integrated to the decimation filter bandwidth ($1/2T_{\mathrm{conv}}$), is 2.4 with a 4-$\mu$A bias current – only slightly higher than the theoretical limit for a common-source differential amplifier [40]. It can also be observed from Fig. 9 that the noise PSD rolls off by 40 dB/dec for the WhB and 20 dB/dec for the LPF after the closed-loop bandwidth matching the derived NTFs shown in Fig. 6(b).

### D. VCO and Counter-Based TDC

The VCO is implemented with a nine-stage $g_{\mathrm{m}}$-current-controlled oscillator ($g_{\mathrm{m}}$-CCO) architecture for linearity, as shown in Fig. 10(a) [41]. Because the LPF uses a PMOS tail current source, its output, $V_{\mathrm{VCO}}$, is insensitive to supply variation. By implementing the VCO $g_{\mathrm{m}}$ cell with an NMOS,

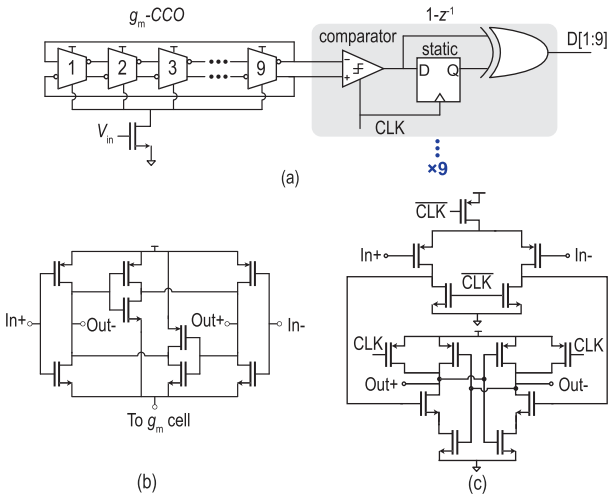


Fig. 10. Schematic of the (a) VCO and TDC, (b) delay cell, and (c) latch.

$V_{GS}$ of the $g_m$ cell is also supply-insensitive. Thus, the current fed into the CCO and consequently $f_0$ have >30 dB better supply rejection than a VCO with a PMOS $g_m$. The delay cell is differential rather than single-ended for better supply rejection and symmetric slewing. A cross-coupled pair is added at each delay cell output to sharpen the transition edge, which improves the VCO $1/f$ noise performance and mitigates the following D flip–flop metastability (in the TDC) [Fig. 10(b)].

Because the VCO noise is shaped by the active LPF, the VCO has a relaxed thermal noise requirement and is designed for low power consumption (1.2 $\mu$W nominally). However, the VCO $1/f$ noise cannot be overlooked. The NMOS $g_m$ cell is sized large ($W/L = 80/60$) to attenuate the $g_m$ cell $1/f$ noise, and the nine stages were chosen to attenuate the delay cell $1/f$ noise. With these techniques, the VCO noise is mostly $1/f$ noise with a $-10$ dB/dec slope (Fig. 9). The VCO $1/f$ noise could be further improved with a larger $g_m$ cell and more stages, at the cost of extra power and area; however, there is no need to do that because the VCO noise is attenuated by the loop gain and contributes the least to the overall FLL noise (Fig. 9).

The VCO delay cell output phase is sampled and sliced by a clocked comparator. The $1-z^{-1}$ operation is realized by feeding the sampled phase with respect to a delayed version into an XOR gate. A dynamic comparator, consisting of a double-tail latch [Fig. 10(c)] in cascade with an SR latch (not shown), is used because the VCO does not have rail-to-rail swing. All nine XOR outputs sum together and generate a 4-bit output, which represents the total number of transition phases during one sample period. To avoid missing a transition phase, the sampling frequency, $f_s$, should be at least twice as $f_0$. Thus, $f_s$ is chosen to be 2 MHz. The system is designed to be thermal noise rather than TDC quantization noise limited. According to [19], the signal-to-quantization noise ratio (SQNR) is calculated to be 116 dB, and the quantization noise to be 0.46 mK (referred to temperature), lower than the FLL input-referred thermal noise limited.

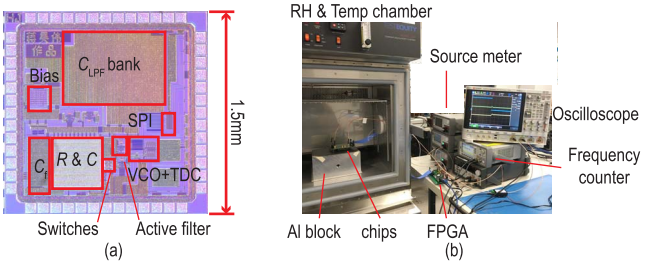


Fig. 11. Photograph of (a) annotated die and (b) measurement setup.

## VI. Measurement

The RH/temp sensor was fabricated in a 180-nm CMOS process [Fig. 11(a)]. The die was directly mounted on an FR4 printed circuit board (PCB) and partially encapsulated with epoxy with an opening above the RH transducer. The sensor occupies 0.72 mm$^2$, among which the transducers and LPF occupy 0.21 and 0.29 mm$^2$, respectively. The circuits for testing purpose (*e.g.*, voltage buffers) and unused capacitor banks are not included in the reported area. The decimation filter, a 13-bit counter, was implemented off-chip in an FPGA. If implemented on-chip, it would consume 0.4 $\mu$W and 0.002 mm$^2$.

### A. PI Coating and Measurement Setup

PI-2545 was drop-cast and spin-coated at 2000 rpm for 60 s. The spin-coating process prevented the PI layer from being too thick, which would slow down the response time. The chips were then cured at 250 °C for 5 h. Note that all the postprocessing procedures could be done more easily on the entire wafer rather than on a single chip in large-volume production.

The measurement setup is shown in Fig. 11(b). An environmental chamber (TEQ-123H) was used for RH/temp control. To filter out the background temperature noise generated by the chamber, the sensors were mounted on a 10-kg aluminum block through a thermal conductive pad. The FPGA and other off-the-shelf testing circuits were placed outside the chamber because they cannot tolerate the harsh environment. Calibrated, high-accuracy commercial sensors were used as references, which include a ±0.05 °C inaccuracy self-adhesive Pt-100 temperature probe mounted on the aluminum block and a 2 %RH inaccuracy capacitive polymer RH sensor embedded in the chamber. Because the reference sensors were using similar transducer technologies compared with this article, that is, thermistor and polymer capacitor, similar thermal and humidity response is ensured, such that the comparison solely focused on the interface circuit itself.

### B. Measurement Results

The circuit consumed 15.6 $\mu$W from a 1.5-V supply at room temperature, where the analog blocks (active filter and the bias circuits) consumed 7.9 $\mu$W, SC-WhB 3.4 $\mu$W, and digital blocks (VCO and TDC) 4.2 $\mu$W. The power breakdown

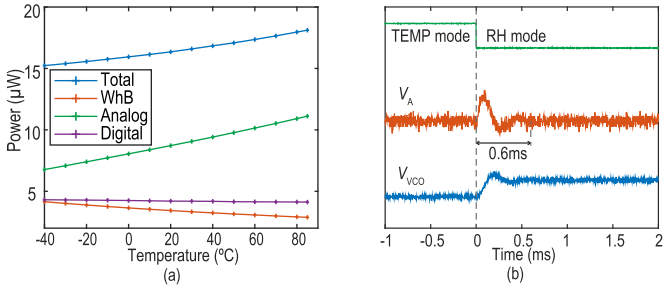


Fig. 12. Measured (a) power versus temperature and (b) transient waveforms during mode switching.

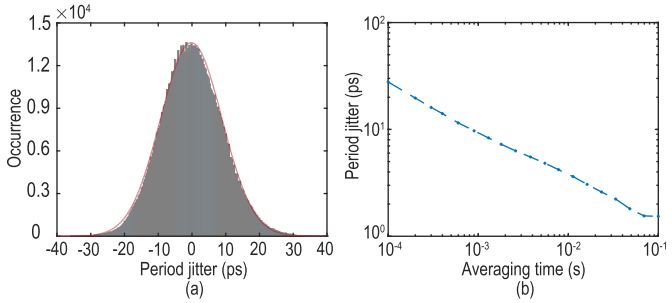


Fig. 13. Measured (a) FLL jitter histogram with 1 ms averaging and (b) jitter versus averaging time.

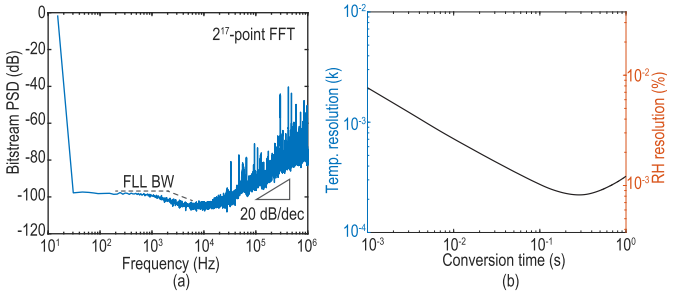


Fig. 14. Measured (a) TDC PSD and (b) temperature and RH resolutions versus $T_{conv}$.

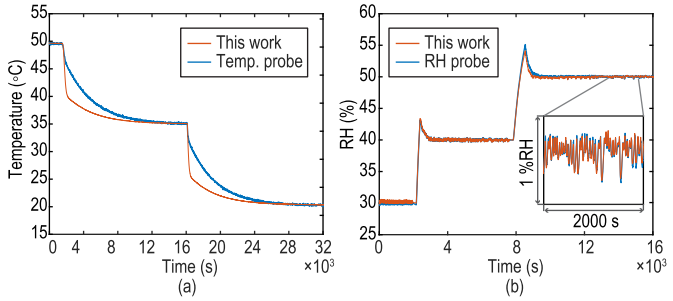


Fig. 15. Measured step response when (a) temperature and (b) RH are changed.

over temperature is shown in Fig. 12(a) where the digital power slightly decreased at higher temperature because the FLL output frequency is CTAT, whereas the analog block power increases with temperature due to the PTAT constant-$g_m$ current reference [42]. The mode switching feature is verified in Fig. 12(b). Because $C_f$ holds the charge such that $V_A$ does not drop during the mode switching, the FLL re-settles in just 0.6 ms. This allows the sensor to start the RH sensing within 1 ms after temperature sensing, which is short enough to remove any cross-sensitivity due to ambient temperature changes.

The FLL period jitter was measured with a frequency counter (Keysight 53230A). Because oversampling is applied to the FLL, the period jitter after averaging is of interest. The histogram shows a standard deviation of 8 ps, corresponding to 5.9 ppm, with 1 ms averaging applied to $10^6$ period samples [Fig. 13(a)]. The period jitter is plotted versus the averaging time in Fig. 13(b). From 0.1 to 10 ms (2 decades), the jitter reduced by 10× because the design is white-noise-limited. The maximum averaging time was limited by the equipment's memory depth.

The TDC was characterized at room temperature (20 °C) and fixed humidity (30 %RH), thus the FLL generated a fixed output frequency, which served as a dc input for the TDC. The TDC output bitstream PSD was assessed using a $2^{17}$-point fast Fourier transform (FFT) and 10× averaging [Fig. 14(a)]. Because the FLL noise dominates at low frequency, the FLL bandwidth could be directly observed from the PSD to be ∼2 kHz, slightly lower than simulation, likely due to process variation. The system resolution was characterized by measuring the output noise at room temperature, and then normalized to both temperature and RH inputs [Fig. 14(b)]. An SNR of 104 dB, or 6-ppm resolution, was achieved with a 1-ms conversion time. This was slightly larger than the FLL jitter with the same averaging time, which verified that the excess noise added by the TDC was much lower than the FLL. By referring to the temperature and RH inputs with $\alpha$ and $\beta$ to the input, 2 mK and 0.0073 %RH resolution were obtained, respectively. For applications demanding low energy consumption (*e.g.*, IoT-oriented), the high resolution can be traded for lower energy by shortening the averaging time. For applications requiring high accuracy, the resolution improves by 10× when $T_{conv}$ increases by 100× because the design is thermal-noise-limited, until environmental drift worsened it after ∼0.3 s. The environmental drift is most likely due to the residual temperature fluctuation at low frequency and unfiltered humidity noise in the test setup. A similar effect was observed in a prior work [9].

The time-domain responses are plotted against commercial sensors in Fig. 15. The temperature mode responded faster than the commercial probe. This is likely due to the slightly different placement of the reference sensor and the test chip where the reference sensor, which had an adhesive surface, had better contact with the aluminum block, thus a stronger filtering effect. Each temperature step took about 14 ks to settle, which ensured the measurement accuracy. It can also be observed that this work showed better noise performance than the commercial probe with 10-mK resolution. While in the RH mode, this work showed nearly the same step response as the commercial sensor, which validated the proposed postprocessing method. This work showed the same fluctuation as the commercial one because the environmental chamber dominated the background RH noise at 0.5 %RH.

The transfer curves in both modes were measured on multiple chips ($n = 10$), as shown in Fig. 16(a) and (c). The temperature transfer curve showed an average $\alpha$ of 2,984 ppm/K and a 6.5% spread on the nominal period. The RH transfer

TABLE I
PERFORMANCE COMPARISON OF ENVIRONMENTAL SENSORS

| | Parameter | Park [7] | Pan [8] | Pan [11] | Choi [12] | Angevare [44] | Mordakhay [43] | Tan [1] | Cirmirakis [2] | Park [18] | Yang [24] | Maruyama [5] | This Work |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| System | Tech. (nm) | 180 | 180 | 180 | 65 | 180 | 65 | 160 | 600 | 180 | 350 | 180 | **180** |
| | Sensor(s) | Temp | Temp | Temp | Temp | Temp | Temp | RH | RH | RH/pres./acc. | *C* | RH & Temp | **RH & Temp** |
| | AFE type | *RC* | *RC* | *R* | *RC* | *RC* | *RC* | *RC* | *C* | *C* | *RC* | *C* | ***RC*** |
| | Active area ($mm^2$) | 0.09 | 0.72 | 0.12 | 0.007 | 0.007 | 0.01 | 0.28 | 2 | 1.28 | 0.35 | 4.5 | **0.72** |
| | Supply (V) | 1.7/1 | 1.6~2 | 1.6~2 | 0.85~1.05 | 1.8 | 1.2 | 1.2 | 5 | 1.1 | 3.3 | 1.55 | **1.5~2** |
| | Conversion time (ms) | 32 | 5 | 10 | 1 | 0.333 | 0.08 | 0.8 | NA | 0.85 | 10.5 | 20 | **1** |
| | Power (μW) | 31 | 160 | 79 | 68 | 1600 | 12.8 | 10.3 | 890 | 2.96 | 759 | 3875 | **15.6** |
| | $FOM_{sen}$ (μJ·$ppm^2$) | 14.7 | 1.17 | 0.39 | 2.08 | 71000 | 45.1 | 1319 | NA | 21.4 | 55.1 | 258 | **0.55** |
| Temp. | Temp. range (°C) | -40~85 | -40~85 | -55~125 | -40~85 | -35~125 | -40~110 | 25 only | 27~35 | 40 only | 20~70 | -20~85 | **-40~85** |
| | 3σ error (K) [trim points] | 0.12 [3] | 0.03[2] [2] | 0.14[2] [2] | 0.7[2] [2] | 0.35[2] [2] | 1.4 [2] | - | - | - | - | 0.6 [NA] | **0.55 [2]** |
| | α (ppm/°C) | 1356[2] | 3000[2] | 4400 | 2200 | 3000[2] | 1465 | - | - | - | - | NA | **2984** |
| | Resolution (mK) | 2.8 | 0.41 | 0.16[4] | 2.5 | 120 | 150 | - | - | - | - | 15 | **2** |
| | $FOM_{Temp}$ (fJ·$K^2$) | 8,000 | 130 | 20 | 430 | 7.6E6 | 2.1E4 | - | - | - | - | - | **62** |
| RH | RH range (%) | - | - | - | - | - | - | 30~95 | 15~85 | 30~90 | - | 0~100 | **10~95** |
| | 3σ error (%) [trim points] | - | - | - | - | - | - | 1.6[5] [2] | NA | 3.3[5] [2] | - | 4 [NA] | **2.2 [2]** |
| | β (ppm/%RH) | - | - | - | - | - | - | 1750 | 730 | 1842 | - | 316[7] | **860** |
| | Resolution (%RH) | - | - | - | - | - | - | 0.05 | NA | 0.04 | 2.63[6] | 0.0057 | **0.0073** |
| | FOM[1](pJ·%$RH^2$) | - | - | - | - | - | - | 20.7 | NA | 6.3 | - | 2518 | **0.83** |

[1] Energy / conversion × (RH resol.)[2] [2] Used high order nonlinearity correction [3] Read from measurement plots [4] Resistors were trimmed
[5] Peak-to-peak error [6] Relative resolution (ppm), calculated from ENOB [7] Calculated from Table III

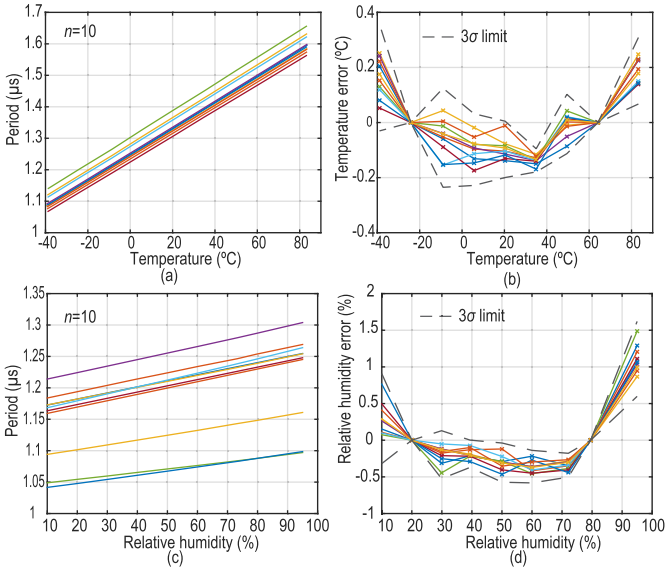


Fig. 16. Measured (a) temperature transfer curve, (b) temperature error, (c) RH transfer curve, and (d) RH error.

curve showed an average $\beta$ of 860 ppm/%RH and a 19% spread, larger than the temperature mode due to the additional postprocessing. The calibration was done by measuring this work against the reference sensors at two temperature points (−20 and 60 °C) and two RH points (20 and 80 %RH). Then, the obtained the first-order polynomial coefficients were applied to other readout points to remove gain error and offset. After a first-order calibration, the remaining errors are shown in Fig. 16(b) and (d): the 3$\sigma$ error is 0.55 °C over the −40 to 85 °C range (industrial standard) and 2.2 %RH over 10–95 %RH (limited by equipment). Compared with prior temperature sensor in Table I, it achieves similar accuracy without using digital-extensive high-order nonlinearity correction owing to the highly linear FLL and SC-based WhB. Varying the supply from 1.5 to 2 V at room temperature, the sensor output changes by 0.018%, corresponding a 0.12 °C/V or 0.43 %RH/V supply sensitivity.

To compare the performance of the 2-in-1 RH/temp sensor with prior temperature and RH sensors, a slightly modified temperature sensor resolution FoM is used to make a fair comparison regardless of the transducer type. Instead of referring the resolution to absolute temperature, resolution referred to the baseline signal (*i.e.* 1/SNR) is used in the FoM definition where

$$\text{FoM}_{\text{sen}} = \frac{\text{Power} \times T_{\text{conv}}}{\text{SNR}} = \text{FoM}_{\text{Temp}}\alpha^2 \tag{20}$$

whose unit is J·$ppm^2$. It should be noted that this can also be obtained by removing the transducer parameter (*i.e.* $\alpha$) from the existing temperature sensor FoM, $\text{FoM}_{\text{Temp}}$. By doing this, this FoM only compares the circuit performance, not process- and sensor-dependent physical parameters. This work demonstrated the state-of-the-art FoM (0.55 $\mu$J·$ppm^2$) compared with the prior RH sensor and compound sensor and comparable (1.5 dB worse) FoM compared with the state-of-the-art temperature-only sensor. It should be noted that this architecture would show better efficiency by designing the WhB to be fully differential, which relaxes the readout circuit noise requirement and eliminates the additional reference branch.

## VII. CONCLUSION

This article presents a fully integrated temperature and humidity sensor consisting of a unified *R&C*-to-*T* converter. Using an FLL with an incomplete-settling, SC-based WhB and a TDC, it avoids high power consumption needed to actively drive the SC compared with prior art and maintains <10 ppm tolerance. Combined with a chopper-stabilized LPF, this system achieves a state-of-the-art RH FoM without degrading the temperature FoM and has low energy (15.6 nJ/meas.) suitable for IoT applications.

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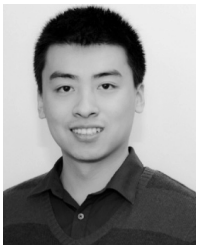

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