A 174.7-dB FoM, 2nd-Order VCO-Based ExG-to-Digital Front-End Using a Multi-Phase Gated-Inverted-Ring Oscillator Quantizer

Corentin Pochet, *Student Member, IEEE*, Jiannan Huang, *Member, IEEE*, Patrick Mercier, *Senior Member, IEEE*, and Drew A. Hall, *Senior Member, IEEE*

***Abstract*—This paper presents a second-order voltage-controlled oscillator (VCO)-based front-end for the direct digitization of biopotential signals. This work addresses the non-linearity of VCO-based ADC architectures with a mismatch resilient, multi-phase quantizer, a gated-inverted-ring oscillator (GIRO), achieving >110-dB SFDR. Leveraging the time-domain encoding of the first integrator, the ADC's power is dynamically scaled with the input amplitude enabling up to 35% power savings in the absence of motion artifacts or interference. An auxiliary input-impedance booster increases the ADC's input impedance to 50 MΩ across the entire bandwidth. Fabricated in a 65-nm CMOS process, this ADC achieves 92.3-dB SNDR in a 1 kHz BW while consuming 5.8 μW for a 174.7 dB Schreier FoM.**

***Index Terms*—VCO-based ADC, direct-digitization, high input impedance, ECG, ExG, biopotential.**

I. Introduction

With the rise of the Internet-of-things (IoT), there has been mounting interest in wearable devices for long-term, continuous health and wellness monitoring [1]–[5]. However, there are many challenges in acquiring high-fidelity, clinical-grade physiological data from a person outside a stationary, controlled environment like a hospital or clinic. For example, a wearable device must tolerate motion artifacts and power line interference (*e.g.*, 50/60 Hz) while having ultra-low power consumption to ensure high-quality measurements over an extended period on a single charge.

Electrocardiography (ECG), electroencephalography (EEG), and electromyography (EMG) are examples of biopotential recording applications. The signals recorded from these are collectively referred to as ExG signals [6], [7]. When recorded using non-invasive electrodes, ExG signals have amplitudes between a few μVs and 10 s of mV over a 1 kHz bandwidth (BW),

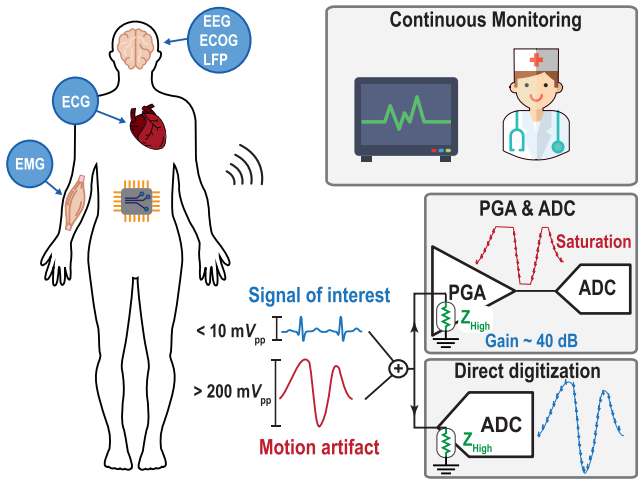


Fig. 1. ExG signal acquisition systems.

thus requiring an input-referred noise $<5\ \mu V_{rms}$. The electrodes also introduce up to 100 mV dc offset. The electrode impedance depends on the electrode material, area, and presence/absence of a conductive gel. Several studies have characterized the impedance of different electrodes and shown that the resistivity in sub-kHz frequencies ranges from ∼1 to 100 kΩ/cm^2 [8], [9]. This results in electrodes with an impedance between 10 kΩ and 5 MΩ, requiring a front-end with high input impedance to not attenuate the signal. More challenging, motion artifacts can induce large in-band signals (common-mode and differential), requiring >200 mV input range [10]. Thus, an ExG analog front-end (AFE) for wearable applications requires a dynamic range (DR) >90 dB to digitize the ExG signal in the presence of electrode offset and motion artifacts without saturation. Importantly, most motion artifact removal algorithms operate on the assumption that the acquired signal is a linear combination of the artifact and ExG signal [11], [12], thus imposing a strict linearity requirement.

A conventional AFE for biopotential acquisition is illustrated in Fig. 1. It is composed of a programmable gain amplifier (PGA) that amplifies and filters the ExG signal before digitization while also providing high input impedance (>10 MΩ). This structure works well for stationary recording, but motion artifacts can cause saturation and/or distortion due to the PGA's

Manuscript received August 9, 2021; revised October 14, 2021; accepted November 21, 2021. Date of publication December 7, 2021; date of current version February 16, 2022. This work was supported in part by Synic and the Korea Electronics Technology Institute (KETI). This paper was recommended by Associate Editor P. Mohseni. *(Corresponding author: Drew A. Hall.)*

The authors are with the Department of Electrical and Computer Engineering, University of California, San Diego, La Jolla, CA 92093 USA (e-mail: cpochet@eng.ucsd.edu; jih324@eng.ucsd.edu; pmercier@ucsd.edu; drewhall@ucsd.edu).

Color versions of one or more figures in this article are available at https://doi.org/10.1109/TBCAS.2021.3133531.

Digital Object Identifier 10.1109/TBCAS.2021.3133531

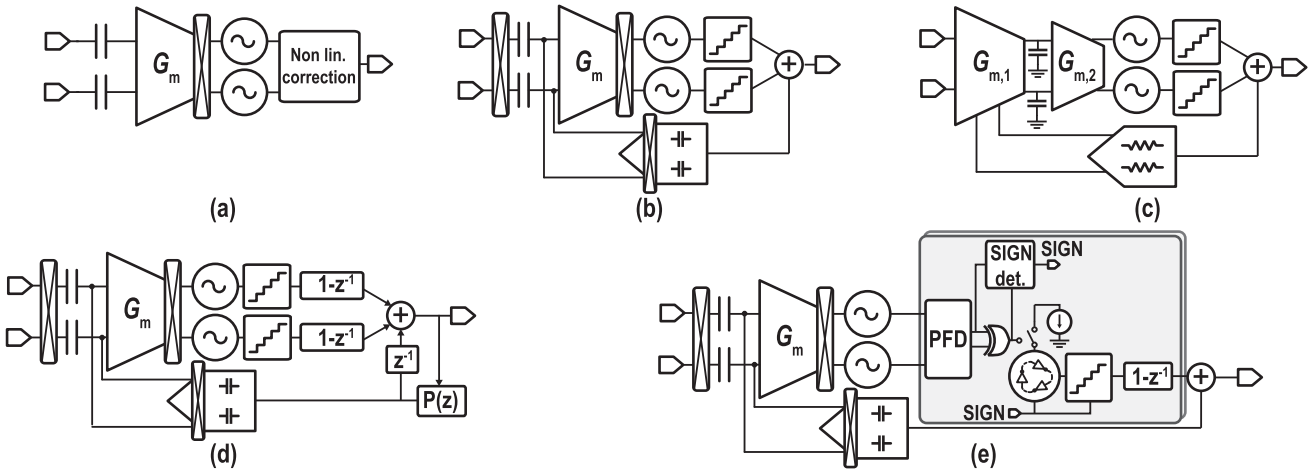


Fig. 2. Direct digitization VCO-based sensor front-end architectures: (a) Open-loop with digital linearity correction, (b) Closed-loop ac-coupled, (c) Hybrid dc-coupled, (d) DPCM-based, and (e) Proposed 2nd-order multi-phase quantizer.

limited DR and linearity. As such, there has been increasing effort toward removing the PGA and directly digitizing the signal [1], [13]–[20], as shown in Fig. 1.

Continuous-time (CT) delta-sigma modulators (DSM) are one candidate to replace the classic PGA and ADC front-end as they have intrinsic anti-aliasing, can achieve high DR, and can be designed to have high input impedance [1], [15], [16], [21]. Several designs have achieved the necessary DR for wearable applications [1], [14], [17]; however, they typically do not have sufficient linearity, complicating downstream signal processing and analysis. Conventionally, CT-DSMs are designed using amplifiers and comparators processing the signal in the voltage domain. While this can achieve excellent performance [21], [22], designing these analog-heavy implementations is complicated with technology scaling, which reduces the supply voltage and intrinsic gain [23]. A key element to achieving high DR and linearity with a DSM relies on multi-bit internal quantizers, which require a mismatch shaping technique to remove mismatch-induced non-linearities in the feedback path, adding delay and power. Due to these drawbacks, there has been growing interest in using time-domain CT-DSMs with phase-domain integration through the use of voltage-controlled oscillators (VCO). By processing the signal in the time/phase-domain, VCO-based ADCs do not suffer as much from the supply voltage reduction and benefit from the shorter transition times associated with advanced process nodes. Furthermore, in some implementations, the circular nature of the ring oscillator can be leveraged to provide intrinsic data weighted averaging (DWA) [9], [13].

This paper reports an ExG front-end that achieves both high DR (>90 dB) and SFDR (>110 dB) in a 1 kHz BW with a 400 mV_{pp} input range. This is accomplished using a single-loop, 2nd-order VCO-based ADC that incorporates a novel multi-phase, multi-quantizer noise-shaped time-to-digital converter (TDC) to achieve high DR and SNDR in a power-efficient fashion. Auxiliary input impedance boosters provide a high input impedance [10]. The time-domain operation also allows for dynamic power scaling through the amplitude-dependent duty cycling of the ADC's second integrator and quantizer, leading to ∼35% power savings in the absence of artifacts. This paper extends the work presented in [25].

The rest of this paper is organized as follows. Section II reviews prior-art in VCO-based ADCs for direct digitization. The system architecture and the proposed quantizer are discussed in Section III. Section IV describes the circuit implementation, and Section V presents measurement results. Finally, conclusions are drawn in Section V.

II. VCO-Based ADC Prior-Art

VCO-based ADCs have become a popular alternative to standard voltage-based continuous-time ADC as they process the information in the time domain, benefiting from process scaling. While much of the research in VCO-based ADCs has been for high-speed applications with bandwidths >10 MHz [26]–[30], VCO-based ADCs also offer significant advantages for sensor applications with kHz bandwidths [31]. This is exemplified by the growing number of sensor-focused, VCO-based ADCs that have been reported in the literature [15], [16], [20], [24], [32]. However, VCO-based ADCs rely on an intrinsically non-linear voltage-to-frequency conversion, limiting their linearity to <50 dB in open-loop without linearity compensation techniques [26].

Several techniques have been reported to address this linearity limitation and are illustrated in Fig. 2. In [15], Jiang *et al.* proposed using an open-loop VCO and linearizing it with digital non-linearity correction [Fig. 2(a)]. While this non-linearity correction algorithm increases the SFDR to ∼80 dB, the input amplitude is limited to 100 mV_{pp}. To further improve the system's linearity and increase the input range, a closed-loop architecture was reported in [16]. As shown in Fig. 2(b), this design achieved 90 dB SFDR, but the input range was still only 100 $mV_{pp,}$ and the 1st-order noise shaping required a high oversampling ratio (OSR) and thus a high chopping frequency leading to a low input impedance (220 kΩ). In [24], a dc-coupled architecture combines a G_m-C integrator with a VCO-based quantizer, as shown in Fig. 2(c). The dc-coupled architecture ensures a high

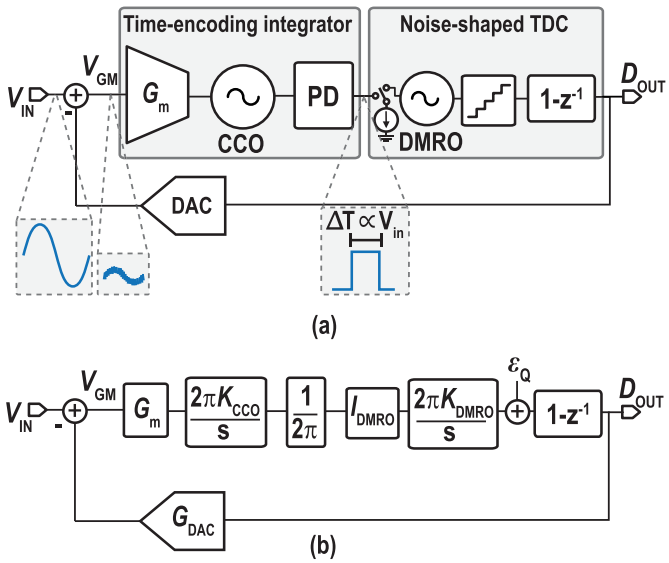


Fig. 3. (a) Simplified single-ended ADC diagram and node waveforms. (b) ADC's block diagram.

input impedance, but it comes at the cost of sensitivity to input common-mode and an analog-heavy first-stage. A differential pulse-code modulation (DPCM)-based predictor is used in [18] to maintain 1st-order quantization noise shaping while allowing for second-order shaping of the input, as shown in Fig. 2(d). However, this requires a large 9-bit capacitive DAC (CDAC) with a large input capacitance, resulting in low input impedance.

III. Architecture

A. Basic Operation

We propose a single-loop, 2nd-order VCO-based ADC that leverages a novel multi-phase, multi-quantizer noise-shaped TDC second stage to achieve high DR and SNDR in a power-efficient fashion [Fig. 2(e)]. The approach is combined with an auxiliary input impedance booster for high input impedance. The proposed architecture is inspired by [33], a high-speed ADC with 2nd-order noise-shaping using only ring oscillator-based integrators. As illustrated in Fig. 3(a), the ADC is composed of a G_{m} stage and a current-controlled oscillator (CCO) followed by a phase detector (PD). The PD output is quantized by a dual-mode ring oscillator (DMRO) TDC and fed back to the input. The first G_{m}-CCO acts as an integrator in the phase domain, accumulating the difference between the input voltage and the DAC. The PD compares the phase between two differential CCOs resulting in a time encoding of the integration value. This time-based encoding has two notable benefits: 1) It enables the use of a low supply voltage after the first stage since the information is in the pulse width, not the amplitude, and 2) The 2nd stage's linearity is guaranteed since a two-level signal drives it. The noise-shaped TDC quantizes the pulse width while providing an additional order of noise-shaping, resulting in 2nd-order noise-shaping for the system. Feedback through a multi-bit DAC results in low input swing at the G_{m}-cell input, which ensures high linearity despite using a non-linear G_{m}-CCO integrator in the 1st stage.

B. Loop Dynamics

The equivalent block diagram of the ADC is shown in Fig. 3(b). The loop has two integrators, and therefore, its stability must be evaluated. Since the loop contains both CT integrators and a discrete-time (DT) differentiator, it must be converted to one domain for analysis using the techniques described in [34]. The equivalent DT model allows the signal transfer function (STF) and noise transfer function (NTF) to be computed as

$$STF\ (z) = \frac{2FT_{\mathrm{s}}^2}{2 + \left(FG_{\mathrm{DAC}}T_{\mathrm{s}}^2 - 2\right)z^{-1} + FG_{\mathrm{DAC}}z^{-2}} \quad (1)$$

$$NTF\ (z) = \frac{2\left(1 - z^{-2}\right)}{2 + \left(FG_{\mathrm{DAC}}T_{\mathrm{s}}^2 - 2\right)z^{-1} + FG_{\mathrm{DAC}}z^{-2}} \quad (2)$$

where $F = 2\pi G_{\mathrm{m}}K_{\mathrm{CCO}}I_{\mathrm{DMRO}}K_{\mathrm{DMRO}}$, G_{m} is the input stage's transconductance, K_{CCO} is the CCO's current-to-frequency gain, I_{DMRO} is the current pulse driving the DMRO, K_{DMRO} is the DMRO's current-to-frequency gain, G_{DAC} is the equivalent DAC gain, and T_{s} is the sampling period. The NTF confirms the 2nd-order noise-shaping behavior of the system. The loop dynamics were further explored and characterized in [35], and the system was shown to be stable over a wide range of coefficients and excess loop delay (ELD), up to an entire clock cycle. This can be explained by the fact that despite having two integrators in the loop, the differentiator effectively "cancels" the effect of an integrator, thus making the system equivalent to a 1st-order $\Delta\Sigma$.

C. Implementation

The practical implementation of this architecture poses several challenges. First, this architecture relies on pseudo-differential encoding at the PD output, which makes it very sensitive to mismatch and limits the linearity (SFDR $<$ 80 dB) in previous designs [33], [35], [36]. Second, prior-art used a switched-ring oscillator (SRO) TDC, which offers good linearity [37], but increases the power consumption, making the system less efficient. This is evident when the 2nd integrator consumes as much (or more) power than the 1st integrator [33], [35], [36], which is far from ideal in a noise-limited design. Finally, the integrator's time-encoded output ensures intrinsic linearity from the second stage, but it generates large tones around the CCO frequency, f_{CCO}, like a pulse-width modulation (PWM) encoded signal. To avoid folding these PWM tones in-band and degrading the SQNR, f_{CCO} must be higher than the sampling frequency, f_{s}, and thus consumes higher power [35].

We tackle these implementation challenges through several innovations. The TDC quantizer is based on a novel gated-inverted-ring oscillator (GIRO) structure that significantly improves power efficiency, mismatch tolerance, and thus the SFDR. This is coupled with a multi-phase, multi-quantizer architecture that relaxes the power required by the first CCO and improves the power efficiency while maintaining high linearity.

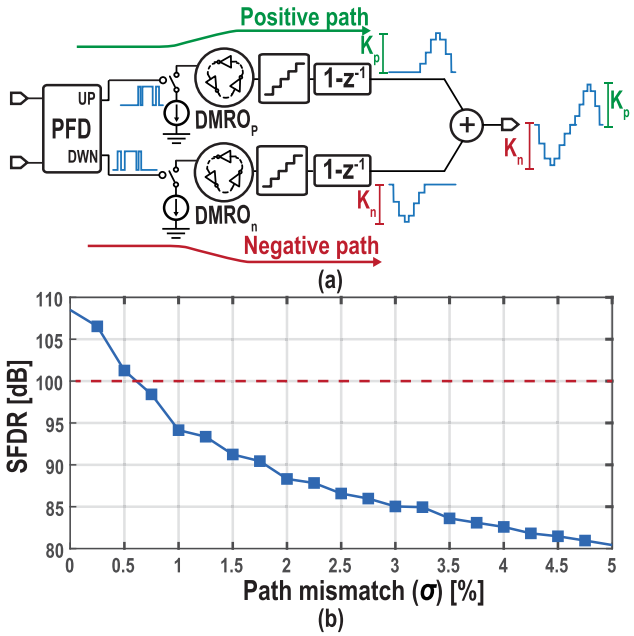


Fig. 4. (a) Block diagram of mismatch induced non-linearity in a dual-path TDC. (b) Simulated SFDR as a function of path mismatch.

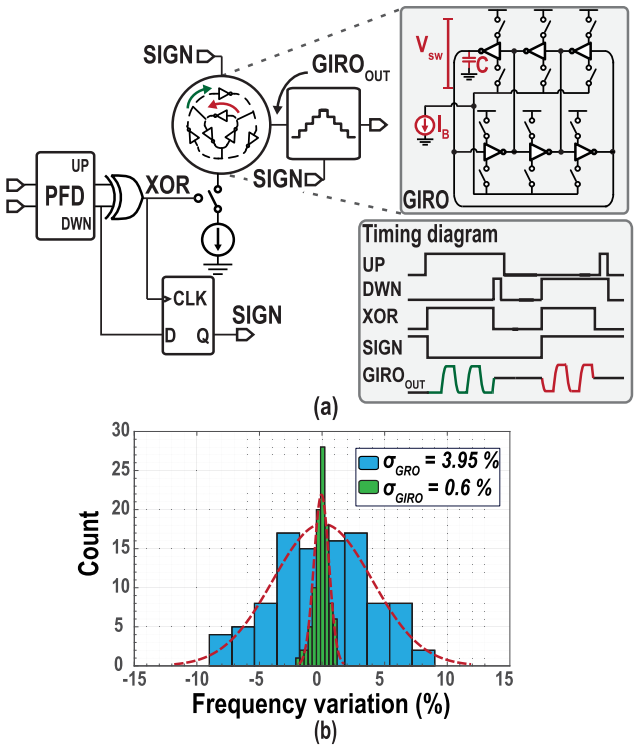


Fig. 5. (a) GIRO and sign detection circuit with timing diagram and (b) Monte Carlo simulation results comparing a GRO and GIRO.

Finally, we use a counter-based quantizer [18] instead of a phase domain sense-amplifier DFF-based quantizer [16], allowing signal-dependent power savings in the absence of motion artifacts.

D. Mismatch Resilient GIRO-Based Quantizer

As illustrated in Fig. 3(b), the TDC is modeled as a CT integrator followed by a digital differentiator, which is equivalent to having a block with $2\pi K_{\mathrm{DMRO}}$ gain [37]. For correct operation, the pulse width must be proportional to the input amplitude. Therefore, the non-saturating range of the PD directly defines the ADC's input range, as an overflow would cause the loop to be unstable. Typically the PD is implemented using a phase-frequency detector (PFD), which has a $2\times$ larger non-saturating input range than an XOR-based PD [38]. The PFD-based TDC operation is shown in Fig. 4, where the positive or negative path is activated depending on the signal polarity. This pseudo-differential operation leads to significant SFDR degradation with path mismatch, despite the high loop gain. Fig. 4(b) shows the simulated linearity where the path mismatch was varied from 0 to 5%. To achieve $>$100 dB SFDR, the mismatch between the two paths must be $<$0.5% and degrades rapidly, reaching 80 dB with 5% mismatch due to even-order harmonic distortion. This SFDR degradation also exists in prior-art dual-path DMRO TDCs, where simulation results show $>$100 dB linearity while measurement results have an SFDR $<$80 dB [33], [35], [36].

There are two common implementations of a DMRO noise-shaped TDC, both based on a current-starved ring oscillator: a gated-ring oscillator (GRO) [39] and an SRO [37]. While a GRO has lower power and better noise performance due to the on/off behavior, the SRO reduces the timing skew and thus improves the linearity. The three major sources of frequency mismatch in a current-starved ring oscillator are: 1) The total node capacitance, C_{tot}, which is influenced by variation in sizing and oxide capacitance; 2) The voltage swing, V_{sw}, due to threshold voltage variation; and 3) Bias current, I_{B}, variation. To improve the path matching of a GRO, we propose the GIRO structure shown in Fig. 5. The GIRO combines an inverted ring oscillator-based TDC [40] and a sign-detection circuit, similar to a digital PLL [41]. The sign detection is implemented with an XOR gate and a DFF. The XOR takes the "absolute value," outputting only the pulse width, and clocks the DFF, which samples the DWN path, thus extracting the "sign" information. This is slightly different from [41], where the other PFD output clocked the sign detection circuit. Clocking with the XOR gate ensures that the SIGN bit updates at the start of the XOR pulse instead of flipping between the start and end, as in the original implementation. With this sign detection circuit, the two TDC paths can be merged into a single path, and the polarity correction is pushed to the digital domain.

The noise-shaping is maintained by using an inverted ring oscillator structure, which merges two ring oscillators such that the TDC oscillates in a clockwise or counter-clockwise direction depending on the SIGN bit. This allows the nodes to share the same capacitance and bias current, significantly improving the matching. The path merging also reduces the leakage by ensuring that the TDC only holds the charge during the short time between pulses instead of between polarity flips, as required in a dual-path GRO.

Fig. 5(b) shows Monte Carlo simulation results ($n = 100$) of the frequency variation of a GRO and GIRO. For the GRO,

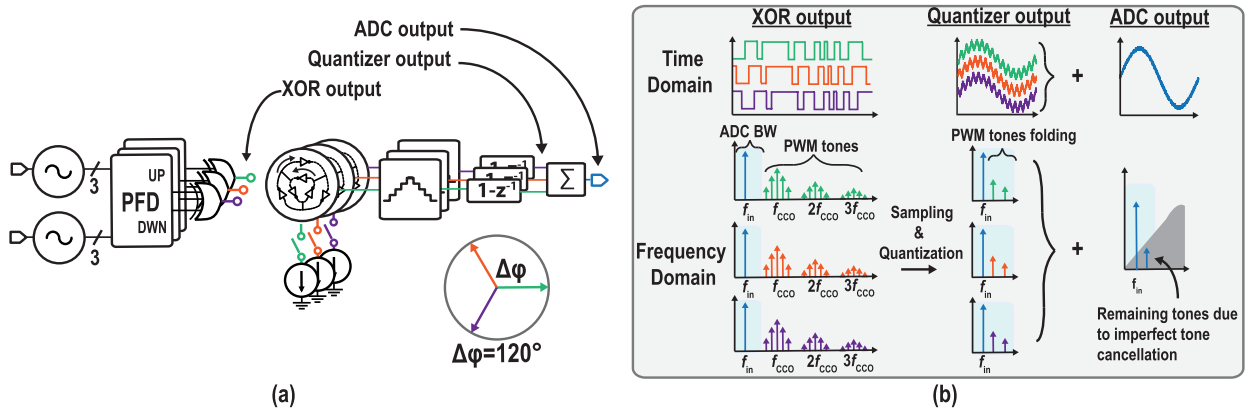


Fig. 6. (a) Multi-quantizer based TDC ($N = 3$); (b) Time and frequency domain operation of the constructive and destructive summing.

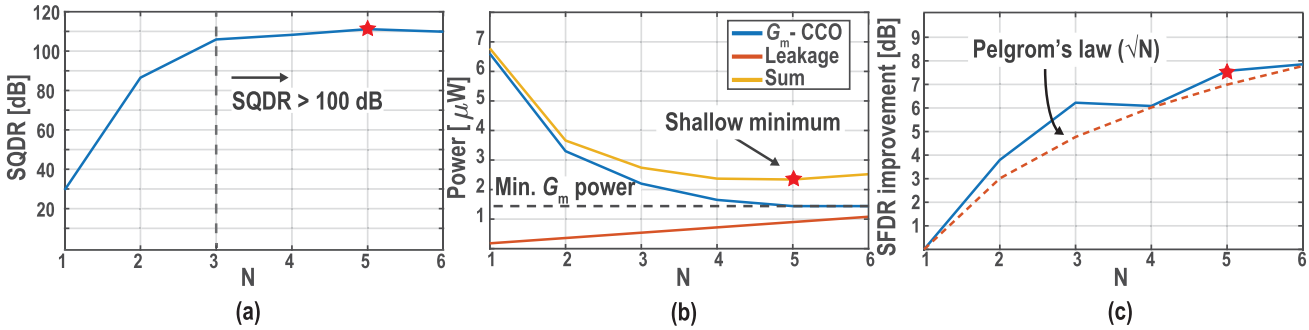


Fig. 7. (a) SQDR vs N, (b) Power vs. N, and (c) SFDR improvement vs. N.

the mismatch is zero-mean with a 4% variance, limiting the SFDR to ∼82 dB, per Fig. 4(b). The GIRO also has zero-mean mismatch, but the variation is reduced to 0.6%. For similar matching, the size of the dual-path DMRO would need to be increased by ∼36× based on Pelgrom's Law, which would require significantly increasing the power consumption of the quantizer. Thus, the GIRO structure improves the matching by 6.5× over a GRO and enables the system to achieve 100 dB much more efficiently than the two-path approach.

E. Multi-Quantizer TDC

The 1st integrator's output after the PFD is represented by a PWM encoded signal at f_{CCO}. This PWM signal contains the result of the integration information at low frequency and high-frequency tones around f_{CCO}. Despite being partially filtered by the second integrator, these high-frequency tones can fold back in-band and degrade the SQNR [35]. To reduce this effect, the CCO can be designed to oscillate at a frequency higher than f_{s} [35]; however, this has the significant drawback of increasing the power consumption. The integrator gain, K_{int}, is

$$K_{\mathrm{int}} = G_{\mathrm{m}}\, K_{\mathrm{CCO}} \propto \frac{G_{\mathrm{m}}}{I_{\mathrm{B}}} f_{\mathrm{CCO}}. \tag{3}$$

This shows that for a target K_{int}, a higher f_{CCO} reduces the G_{m}-cell's efficiency. Since the noise target sets G_{m}, it is critical to minimize f_{CCO} to minimize the integrator's power.

In [33], a multi-phase approach was proposed to break this tradeoff, where f_{CCO} is virtually increased by tapping and combining multiple phases of the ring oscillator in the current domain. While this technique lowers f_{CCO}, it comes at the cost of losing the intrinsic linearity of the TDC-based quantizer. We propose using multiple noise-shaped TDCs in parallel, which maintains the intrinsic linearity of each channel and allows a lower f_{CCO}. This approach is illustrated in Fig. 6(a) using three phases. Similar to [33], multiple out-of-phase components of the ring oscillator are tapped, but instead of being combined in an analog fashion using a current summer, each of the individual channel's SIGN bit is detected, and then the output of the XOR gate is fed to the GIRO-based TDC. The results are then summed digitally. We ensure that each channel only operates between two levels by pushing this summation to the digital domain, thus preserving the inherent linearity.

Fig. 6(b) illustrates how the digital tone cancellation works. Each XOR output pulse contains the integration information and high-frequency tones quantized by a separate TDC. Each TDC output is composed of input tones scaled by 1/N, where N is the number of channels, and folded back tones. The phase and frequency of the input tone are matched across the channels, while the folded tones generated by the PWM encoding are both out-of-phase *and* at the same folded frequency. These conditions enable the signal tones to add constructively during digital summation while the folded tones add destructively. This leads to a high SQNR and is reasonably insensitive to phase and

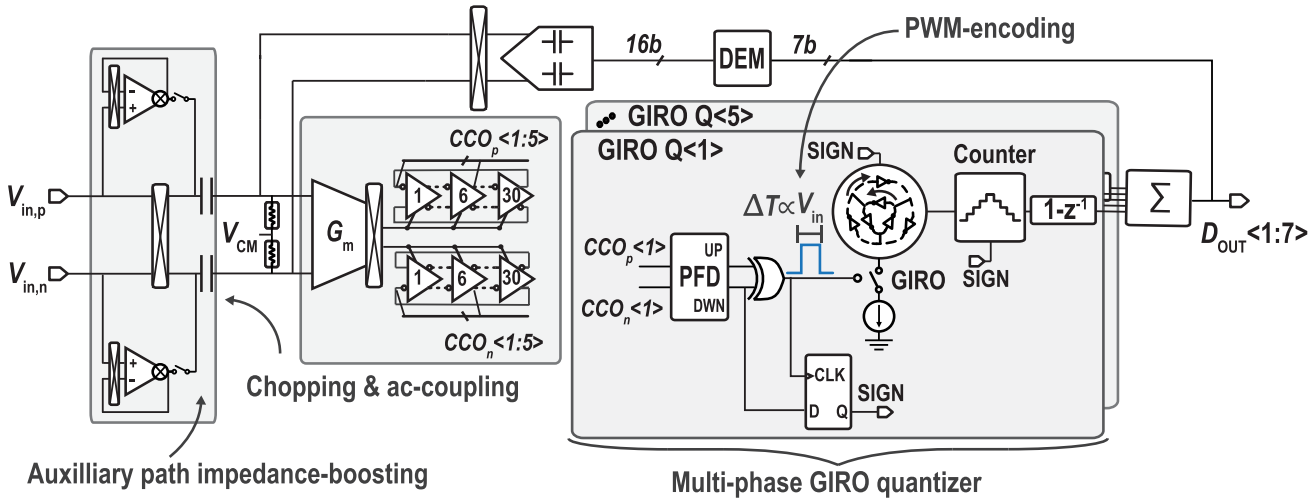


Fig. 8. ADC architecture.

gain mismatch between the channels. Selecting N is a tradeoff between area, power, and target signal-to-quantization noise and distortion ratio (SQDR). As illustrated in Fig. 7(a) and (b), as the number of phases increases, the SQDR increases while the power required by the $G_{\rm m}$-CCO decreases. However, the leakage power of the digital cells increases, which leads to a shallow power optimum. Balancing these tradeoffs, $N = 5$ was selected for this design.

Another advantage of the multi-quantizer approach is that it improves the linearity due to averaging by reducing the distortion and the quantization noise, as observed in [42]. Here the multiple TDCs act as staggered quantizers improving the SQNR and linearity. This was simulated and is shown in Fig. 7(c), where the matching increases with N and follows the well-known Pelgrom's Law [43], [44], which trades-off area (the number of quantizers) for improved matching. For $N = 5$, this improves the SFDR by 7 dB. This multi-quantizer averaging also reduces the effect of inter-channel gain and phase mismatch. Simulations showed no SQNR degradation occurs for gain and phase mismatch $<$15%, which is easily achieved with appropriate sizing and layout.

IV. Circuit Implementation

A. System Architecture

The ADC architecture is shown in Fig. 8. A 200 kHz sampling frequency was selected for an OSR of 100 and a 1 kHz BW. The loop coefficients ($G_{\rm m} = 18$ µS, $K_{\rm CCO} = 74$ GHz/A, $K_{\rm DMRO} = 10$ THz/V, and $I_{\rm DMRO} = 200$ nA) were selected through extensive behavioral simulations using *Simulink* and *Spectre*, trading off the SQNR and the loop stability. A 7-bit DAC was selected for an SQNR $>$110 dB and to guarantee a small swing at the $G_{\rm m}$-cell input. These parameters tolerate up to 2% delay from the digital logic and DEM without additional compensation.

The first integrator is chopped at $f_{\rm s}/2$ (100 kHz) to reduce 1/f noise. This chopping frequency was picked to avoid quantization noise folding. The input capacitance is 900 fF, implemented with a metal-insulator-metal (MIM) capacitor. This capacitance forms a high-pass filter (corner frequency $<$ 10 Hz) with the pseudo-resistors used to bias the $G_{\rm m}$-cell. The 7-bit CDAC designed with custom 1.85 fF metal-oxide-metal (MOM) capacitors guarantees that the input swing is $<$15 $\rm mV_{pp}$. The MOM capacitors were sized to achieve $<$0.2% matching according to [45]. The total CDAC capacitance is 300 fF, such that the input capacitive attenuation is 0.7. A switched-capacitor resistor is formed by chopping before the input capacitance, significantly reducing the input impedance ($\sim$5 MΩ). This impedance is too low to interface with small electrodes, which have impedances of several MΩ. An auxiliary amplifier precharges the input capacitance after the chopping clock, thus reducing the charge that needs to be supplied from the electrode and increasing the input impedance. The input impedance booster was implemented similarly to [10] using buffer duty-cycling for power savings and capacitive charge sharing for fast charging. The maximum achievable input impedance is limited by two factors: 1) The input impedance due to chopping the auxiliary buffer, which is needed to eliminate its offset and 1/f noise [10]; and 2) The duty-cycle needs to be $<$5% of $T_{\rm s}$ to maintain low power and avoid SNDR degradation, which leaves 250 ns to precharge the input capacitor. These factors limit the maximum input impedance with auxiliary input-impedance boosting to a few 10s of MΩ in a CT-DSM-based direct-digitization architecture [1].

B. G_m-CCO Integrator

The 1st integrator is composed of a chopped $G_{\rm m}$ and two 30-stage ring oscillators. The chopping reduces the 1/f noise such that the system is thermal noise limited. The $G_{\rm m}$ is implemented as a differential pair for direct current control of the CCO and to avoid the power overhead required for common-mode feedback and the non-linearity of a two-stage current-reuse topology [18]. It is source degenerated by a 12 kΩ tunable resistor ($\pm$10%) to

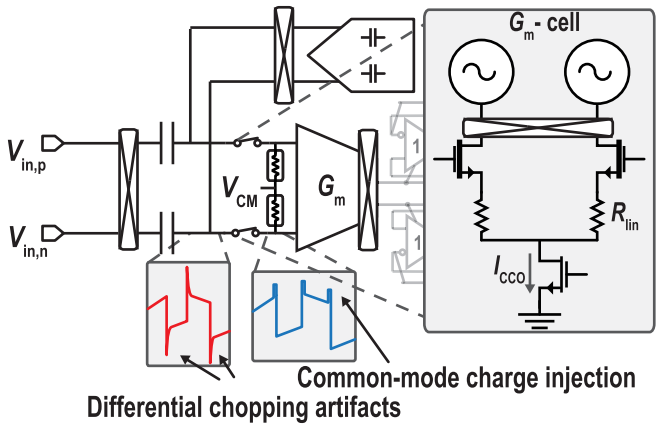


Fig. 9. Schematic of the chopped G_{m}.

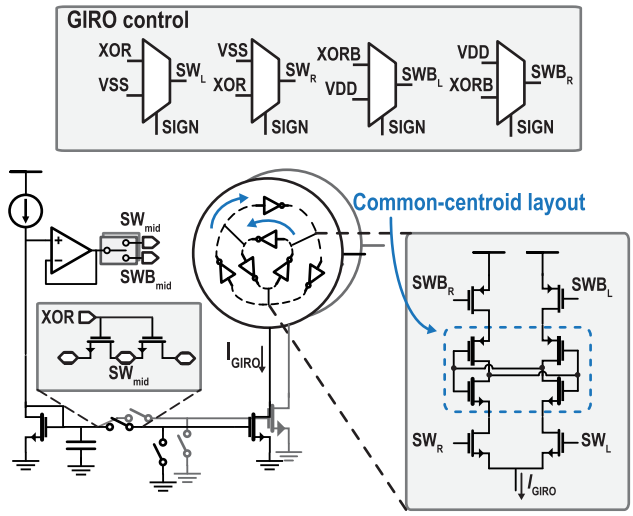


Fig. 10. Schematic of the GIRO.

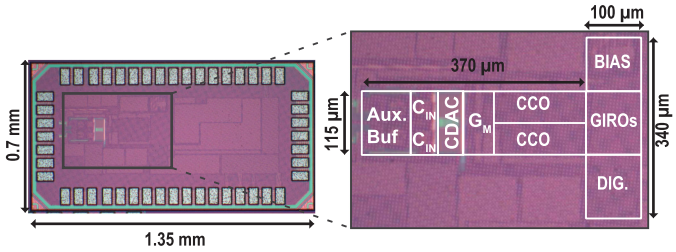


Fig. 11. Die photo.

linearize the G_{m} that tunes the loop parameters while maintaining a constant f_{CCO}. The input transistors are thick-gate oxide NMOS devices to reduce gate leakage and avoid common-mode drift from the pseudo-resistors. As shown in Fig. 9, dead-band switches in front of the G_{m} are opened for 300 ns during chopping and convert the differential switching artifacts to a common-mode signal. The dead-band switch pulse-width was chosen to absorb the digital propagation delay while minimally affecting the input-referred noise.

Each ring oscillator stage is a cross-coupled PMOS due to its superior noise performance [36]. The loop parameters determined the sizing, and 30 stages were chosen for flexibility as it could be easily reconfigured to work with $N = 6$ based on post-layout simulations. Every 6th node of the CCO is tapped, such that the five outputs are separated by 72°. As described earlier, this relaxes the requirement on f_{CCO} such that it can be reduced to 120 kHz.

C. GIRO Quantizer

Each TDC channel has a PFD, a sign detector, and a GIRO. The PFD is implemented using the well-known NAND structure. The UP and DOWN outputs are fed to the XOR gate and the DFF. The XOR is designed so that the propagation delay is long enough to allow the DFF to settle and avoid settling errors. While this could cause incorrect polarity extraction, this can only happen if the UP and DOWN pulses are extremely close to each other, which is a negligible error as it means the signal is extremely close to a polarity flip. An additional cross-coupled delay chain is added between the XOR and the GIRO input to generate differential signals and ensure a 2 ns delay between the polarity flipping and the first GIRO edge. This delay allows settling of the counters across process variation and corners. The delay chain output controls the GIRO behavior through digital muxes, as shown in Fig. 10.

Each stage of the GIRO is implemented using single-ended, thick-oxide inverters to reduce leakage. They are laid out in a common-centroid fashion to improve the matching between the two paths. The inverter switches are minimum-sized transistors to reduce charge injection and leakage. The bias current generation is shared among all channels, and each independent current source is gate switched. A large MIM capacitor enables quick charge sharing for rapid turn on/off and reduces skew. Due to the shared bias and the low current reference (200 nA), the large switches' leakage can modulate the current source's bias voltage, leading to non-linearity. A low-leakage switch structure was used to ensure that this effect is limited and does not degrade the linearity [46], as illustrated in Fig. 10. The buffer only consumes 100 nA, and is shared by the 5 channels.

D. Digital Blocks

Each GIRO output is fed to a counter, triggered by the rising or falling edge depending on whether the polarity bit is positive or negative. Since the counter's output is updated asynchronously with the sampling clock, this leads to potential sampling errors. Multiple bits could flip during a sampling instant for a binary counter, leading to a significant output error. Instead, the counter is implemented with a gray counter that guarantees only a 1-bit flip, limiting the sampling error. The output of each counter is passed through a gray-to-binary encoder and combined to obtain the final ADC output.

Given the multi-bit inner quantizer and feedback, a form of mismatch shaping is needed. While DWA is a popular choice in high precision ADCs due to its low SQNR degradation, segmented DEM is used in this work since the number of wires

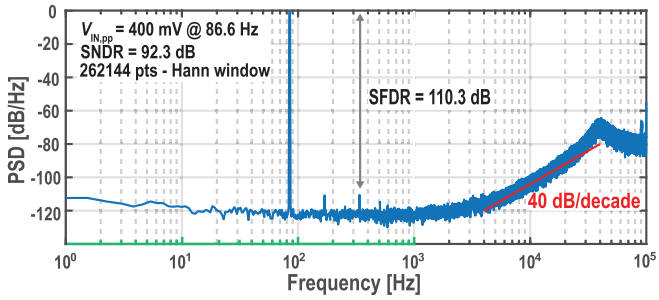


Fig. 12. Measured ADC output spectrum.

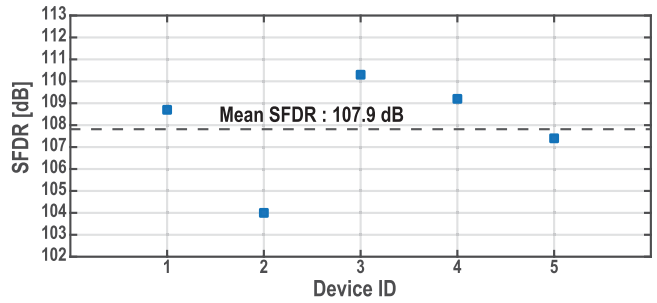


Fig. 13. Measured ADC SFDR for 5 devices.

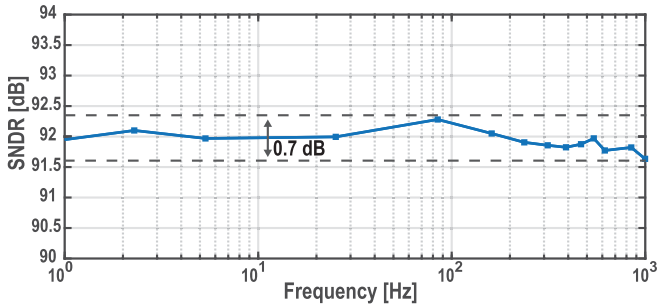


Fig. 14. Measured ADC SNDR over its bandwidth.

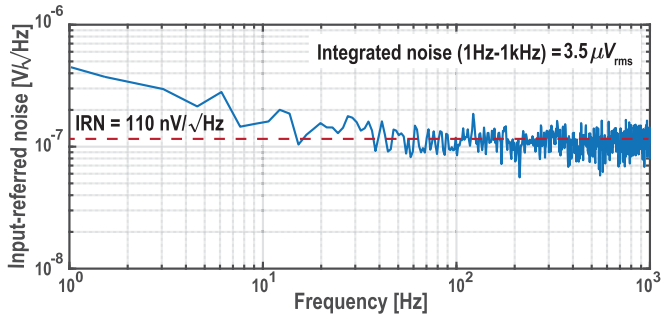


Fig. 15. Measured ADC input-referred noise spectrum.

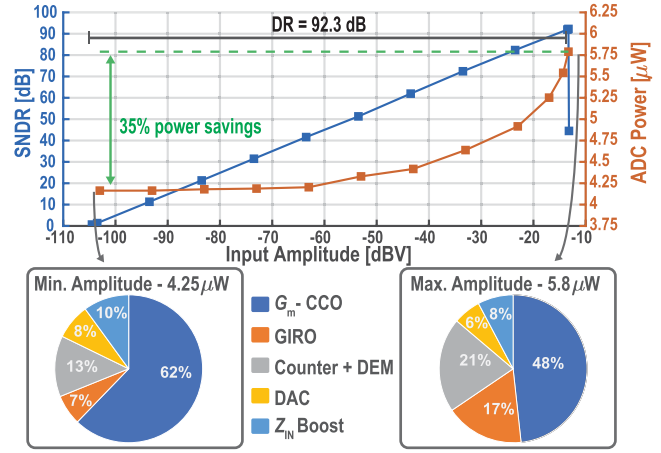


Fig. 16. Measured SNDR and power vs. input amplitude.

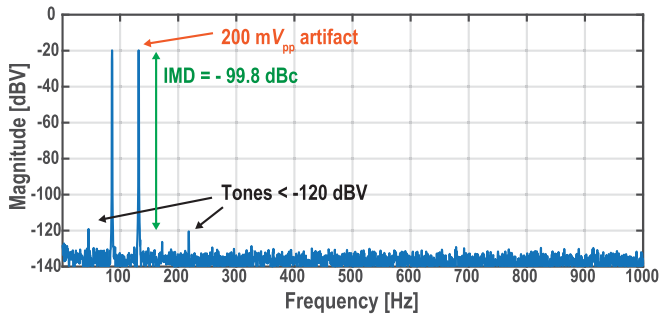


Fig. 17. Measured intermodulation distortion (IMD).

required for DWA ($2^7 = 128$) would have severely complicated the CDAC layout. On the other hand, segmented-tree DEM only requires ($2^4 = 16$) wires, leading to a more straightforward layout and routing, and does not generate any tones at the cost of a higher noise floor. Simulink simulations confirmed that an SQNR $>$100 dB could be achieved with up to 1% DAC mismatch (5$\times$ our design target). All digital logic was written in Verilog and synthesized using a standard digital flow.

V. Measurement Results

The VCO-based ADC was fabricated in a 65 nm TSMC LP process and occupied an active area of 0.075 mm^2. An annotated die micrograph is shown in Fig. 11. The 1st integrator, impedance-booster, and CDAC are powered from a 1.2 V supply while the multi-phase TDC quantizer and the digital blocks containing the summer and DEM logic operate at 0.8 V.

A. Electrical Characterization

The ADC's SNDR, SFDR, and DR were characterized with an ultra-low distortion signal generator (APx555) that generated a full-scale, 400 mV_{pp} sinusoid. The measured output spectrum is shown in Fig. 12. The ADC achieved an SNDR of 92.3 dB in 1 kHz BW and a 110.3 dB SFDR, limited by the 3rd harmonic. The 40 dB/decade noise-shaping expected from the 2nd-order NTF is evident. To assess the mismatch resilience, the SFDR of 5 devices was measured (Fig. 13). The average SFDR is 107.9 dB and consistently above 104 dB. The SNDR as a function of frequency from 1 Hz to 1 kHz is shown in Fig. 14. The SNDR varies by less than 0.7 dB across the entire frequency range.

The ADC input-referred noise was measured with shorted inputs. The PSD is shown in Fig. 15. The integrated noise from

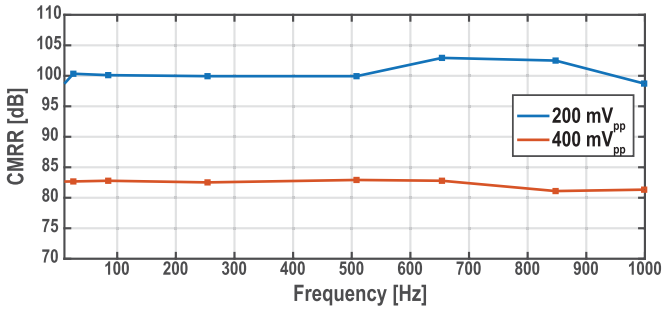


Fig. 18. Measured common-mode rejection ratio (CMRR) with a 200 mV_{pp} (orange) and a 400 mV_{pp} (blue) common-mode input.

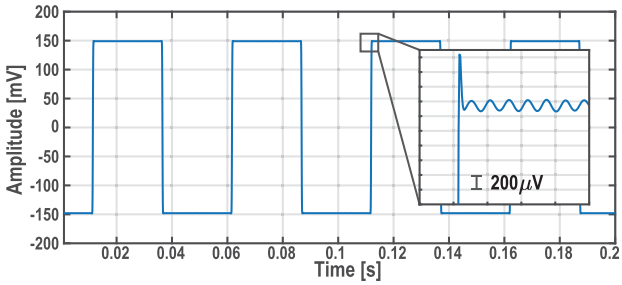


Fig. 19. Square wave and sinusoid combined.

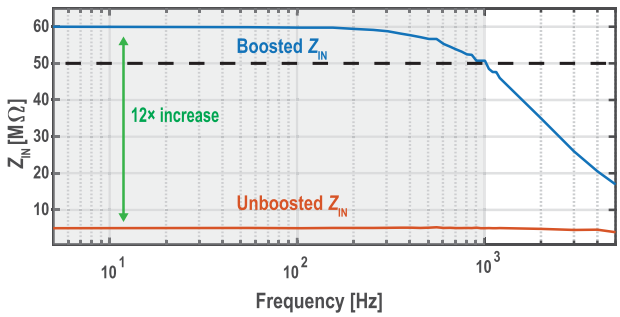


Fig. 20. Measured input impedance with and without boosting.

1 Hz to 1 kHz is 3.5 μV_{rms}, and the spot noise is 110 nV/$\sqrt{}$Hz. The 1/*f* noise in the spectrum is mainly due to the inverters in the 1st CCO, which are not chopped. However, this is less than 15% of the integrated noise.

Fig. 16 shows the measured 92.3 dB DR and the power as a function of the amplitude. The pie charts show that the system power reduced from 5.8 to 4.25 μW (35%) when the input amplitude was below 10 mV. As expected, the power of the GIRO and digital blocks reduce significantly, and the power consumption is dominated by the input G_m-cell. This results from the input-dependent quantizer duty-cycling, enabling low power in the absence of motion artifacts.

The ADC was excited with two tones at 200 mV_{pp} to evaluate the impact of large motion artifacts on the linearity. Fig. 17 shows the measured intermodulation distortion (IMD) was 99.8 dBc with the intermodulation products ∼1 μV, which is below the 3.5 μV_{rms} integrated noise of the AFE. This demonstrates that even in the presence of significant motion artifacts/interference, the distortion would be below the noise floor and thus not introduce any unwanted signals.

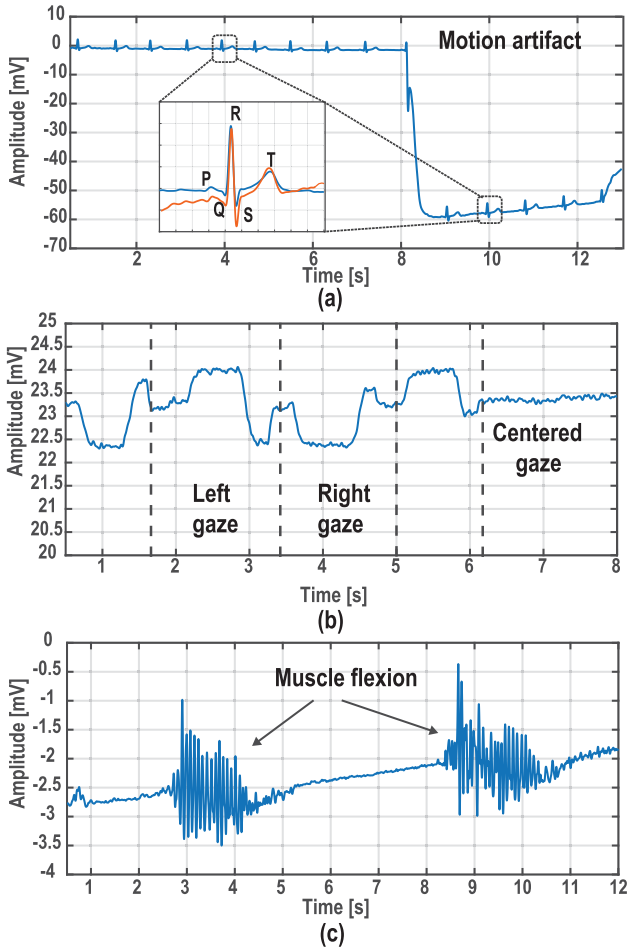


Fig. 21. ExG measurements: (a) ECG, (b) EOG, and (c) EMG.

The common-mode rejection ratio (CMRR) was measured across the bandwidth with a full-scale ADC input (200 mV_{pp} single-ended) and was above 95 dB over the entire frequency range. Since a larger common-mode artifact is expected in a wearable device (up to 400 mV_{pp}), the ADC's CMRR was measured with this larger input to be 82 dB. Common-mode artifacts larger than 400 mVpp cause the ADC's loop stability to degrade, leading to a loss in performance. It should be noted that the results are better than reported in the original paper [25] due to an improvement in the testing setup. The insensitivity to large and rapid artifacts was tested by superimposing a 150 μV_{pp} sinusoid signal on a 300 mV_{pp} square wave. As illustrated in Fig. 19, the ADC quickly recovers from the artifact, allowing the small sinusoidal to be clearly observed.

To measure the input impedance, Z_{in}, high precision 1 MΩ resistors were placed in series with the ADC inputs and the voltage across them amplified by an instrumentation amplifier. Fig. 20 shows Z_{in} measured across the bandwidth with and without activating the auxiliary path booster. Z_{in} is boosted by 12× when the auxiliary path is enabled and is >50 MΩ across the entire bandwidth.

TABLE I
PERFORMANCE SUMMARY AND COMPARISON TO THE STATE-OF-THE-ART

Parameter	[15]	[19]	[16]	[24]	[22]	[21]	This work
Integration domain	Time	Time	Time	Hybrid	Voltage	Voltage	**Time**
Topology	Open-loop	1st-ord.	1st-ord.	2nd-ord.	3rd-ord.	CCIA + 3rd-ord.	**2nd-ord.**
Technology [nm]	40	65	40	65	180	65	**65**
Area [mm^2]	0.135	0.08	0.025	0.078	0.5	0.113	**0.075**
Supply (A/D) [V]	1.2/0.45	0.8	0.8/0.6	1	1	1.2	**1.2/0.8**
Power [µW]	7	1.68	4.5	6.5	6.5	7.3	**4.25-5.8**
Coupling	ac	ac w/chopping	ac w/chopping	dc	ac w/chopping	ac w/chopping	**ac w/chopping**
Input-range [mV$_{pp}$]	100	460	100	300	360	200	**400**
Sampling frequency [kHz]	3	64	2500	1280	12.8	400	**200**
BW [kHz]	0.2	0.5	10	10	0.3	5	**1**
CMRR [dB]	66	97	83	76	84	78	**100.2 dB**
Input-referred noise [nV/√Hz]	367	118	36	95	265	90	**110**
SNDR [dB]	75.2	94.2	78.5	80.4	84.3	78	**92.3**
DR [dB]	77.4	95.1	79	80.4	84.3	81	**92.3**
SFDR [dB]	79	128	91	92.2	104.7	81	**110.3**
Z_{in} at DC / BW [MΩ]	∞ / 8	8 / 8	0.22 / 0.22	∞ / 13.3	39 / 39	1500 / 19.6	**60 / 50**
FoM$_{SNDR}$[dB]	149.6	178.9	172	172.3	160.9	166.4	**174.7**

B. Biological Measurements

This ADC was validated by measuring various ExG signals with 3M red dot electrodes on a healthy volunteer. Fig. 21(a) shows the waveform from a three-lead chest ECG recording. Around 8 seconds into the recording, motion artifacts were purposely generated to showcase the ability of the system to correctly digitize the ECG waveform in the presence of large motion artifacts like one would encounter with a wearable in a non-stationary environment. The system does not saturate, and the ECG waveform can be observed and extracted despite the large motion artifact. The system was also used to measure EOG [Fig. 21(b)] and EMG [Fig. 21(c)] showing that the system can measure standard ExG waveforms.

C. Comparison to the State-of-the-Art

Table I compares this work with recently published direct digitization ADCs operating in the time and the voltage domains. This work achieves excellent linearity due to the improved matching of the proposed GIRO-based quantizer. The time-domain signal processing also enables significant power savings in the "nominal" operating state (*i.e.*, in the absence of artifacts). This work achieves a competitive Schreier figure-of-merit (FoM) of 174.7 dB while maintaining an input impedance >50 MΩ over the entire bandwidth of interest.

VI. CONCLUSION

This paper presents a direct-digitization VCO-based ADC for biopotential recording that achieves over 90 dB SNDR and 100 dB SFDR enabling it to digitize small ExG signals in the presence of large motion artifacts and interference. This is accomplished by enabling second-order noise-shaping using an integrating and time-encoding VCO-based 1st stage followed by a multi-phase, multi-quantizer noise-shaped TDC. The system's linearity is further improved using a GIRO that significantly reduces the mismatch sensitivity. Leveraging the time-based processing of the ADC, the system's power is naturally duty-cycled with the input amplitude leading to 35% power savings in the absence of artifacts. To achieve the high input impedance required to interface with small electrodes, an input-impedance boosting circuit is placed around the input-chopper boosting the input impedance by 12× and guaranteeing >50 MΩ input impedance over the entire bandwidth while achieving very high linearity, low noise, and high power-efficiency.

REFERENCES

[1] X. Yang *et al.*, "A 108 dB DR hybrid-CTDT direct-digitalization ΔΣ-ΣM front-end with 720 mVpp input range and >300 mV offset removal for wearable bio-signal recording," in *Proc. Symp. VLSI Circuits*, 2019, pp. C296–C297, doi: 10.23919/VLSIC.2019.8778185.

[2] S. Mondal, C.-L. Hsu, R. Jafari, and D. Hall, "A dynamically reconfigurable ECG analog front-end with a 2.5 × data-dependent power reduction," in *Proc. IEEE Custom Integr. Circuits Conf.*, 2017, pp. 1–4, doi: 10.1109/CICC.2017.7993705.

[3] S. Mondal and D. A. Hall, "A 13.9-nA ECG amplifier achieving 0.86/0.99 NEF/PEF using AC-coupled OTA-stacking," *IEEE J. Solid-State Circuits*, vol. 55, no. 2, pp. 414–425, Feb. 2020, doi: 10.1109/JSSC.2019.2957193.

[4] Y. Zheng *et al.*, "Unobtrusive sensing and wearable devices for health informatics," *IEEE Trans. Biomed. Eng.*, vol. 61, no. 5, pp. 1538–1554, May 2014, doi: 10.1109/TBME.2014.2309951.

[5] J. Andreu-Perez, D. R. Leff, H. M. D. Ip, and G. Yang, "From wearable sensors to smart implants—toward pervasive and personalized healthcare," *IEEE Trans. Biomed. Eng.*, vol. 62, no. 12, pp. 2750–2762, Dec. 2015, doi: 10.1109/TBME.2015.2422751.

[6] J. Warchall, P. Theilmann, Y. Ouyang, H. Garudadri, and P. P. Mercier, "Robust biopotential acquisition via a distributed multi-channel FM-ADC," *IEEE Trans. Biomed. Circuits Syst.*, vol. 13, no. 6, pp. 1229–1242, Dec. 2019, doi: 10.1109/TBCAS.2019.2941846.

[7] S. Lee, L. Yan, T. Roh, S. Hong, and H. Yoo, "A 75 μ w real-time scalable body area network controller and a 25 μW ExG sensor IC for compact sleep monitoring applications," *IEEE J. Solid-State Circuits*, vol. 47, no. 1, pp. 323–334, Jan. 2012, doi: 10.1109/JSSC.2011.2170636.

[8] A. Searle and L. Kirkup, "A direct comparison of wet, dry and insulating bioelectric recording electrodes," *Physiol. Meas.*, vol. 21, no. 2, pp. 271–283, May 2000, doi: 10.1088/0967-3334/21/2/307.

[9] G. Li, S. Wang, and Y. Y. Duan, "Towards gel-free electrodes: A systematic study of electrode-skin impedance," *Sensors Actuators B: Chem.*, vol. 241, pp. 1244–1255, Mar. 2017, doi: 10.1016/j.snb.2016.10.005.

[10] H. Chandrakumar and D. Markovic, "An 80-mVpp linear-input range, 1.6-GΩ input impedance, low-power chopper amplifier for closed-loop neural recording that is tolerant to 650-mVpp common-mode interference," in *Proc. IEEE Int. Solid-State Circuits Conf.*, 2017, pp. 1–18, doi: 10.1109/JSSC.2017.2753824.

[11] D. Seok, S. Lee, M. Kim, J. Cho, and C. Kim, "Motion artifact removal techniques for wearable EEG and PPG sensor systems," *Front. Electron.*, vol. 2, 2021, Art. no. 4, doi: 10.3389/felec.2021.685513.

[12] X. Jiang, G.-B. Bian, and Z. Tian, "Removal of artifacts from EEG signals: A review," *Sensors*, vol. 19, no. 5, Feb. 2019, Art. no. 987, doi: 10.3390/s19050987.

[13] H. Kassiri *et al.*, "Rail-to-rail-input dual-radio 64-channel closed-loop neurostimulator," *IEEE J. Solid-State Circuits*, vol. 52, no. 11, pp. 2793–2810, Nov. 2017, doi: 10.1109/JSSC.2017.2749426.

[14] C. Kim, S. Joshi, H. Courellis, J. Wang, C. Miller, and G. Cauwenberghs, "Sub- μ Vrms-noise sub- μ W/Channel ADC-direct neural recording with 200-mV/ms transient recovery through predictive digital autoranging," *IEEE J. Solid-State Circuits*, vol. 53, no. 11, pp. 3101–3110, Nov. 2018, doi: 10.1109/JSSC.2018.2870555.

[15] W. Jiang, V. Hokhikyan, H. Chandrakumar, V. Karkare, and D. Markovic, "A ±50-mV linear-input-range VCO-based neural-recording front-end with digital nonlinearity correction," *IEEE J. Solid-State Circuits*, vol. 52, no. 1, pp. 173–184, Jan. 2017, doi: 10.1109/JSSC.2016.2624989.

[16] S. Li *et al.*, "A 0.025-mm2 0.8-V 78.5dB-SNDR VCO-based sensor readout circuit in a hybrid PLL-ΔΣM structure," in *Proc. IEEE Custom Integr. Circuits Conf.*, 2019, pp. 1–3, doi: 10.1109/CICC.2019.8780175.

[17] M. R. Pazhouhandeh, M. Chang, T. A. Valiante, and R. Genov, "Track-and-Zoom neural Analog-to-Digital converter with blind stimulation artifact rejection," *IEEE J. Solid-State Circuits*, vol. 55, no. 7, pp. 1984–1997, Jul. 2020, doi: 10.1109/JSSC.2020.2991526.

[18] J. Huang and P. P. Mercier, "A 112-dB SFDR 89-dB SNDR VCO-based sensor front-end enabled by background-calibrated differential pulse code modulation," *IEEE J. Solid-State Circuits*, vol. 56, no. 4, pp. 1046–1057, Apr. 2021, doi: 10.1109/JSSC.2020.3037833.

[19] J. Huang and P. P. Mercier, "28.1 A distortion-free VCO-based Sensor-to-Digital front-end achieving 178.9dB FoM and 128dB SFDR with a calibration-free differential pulse-code modulation technique," in *Proc. IEEE Int. Solid- State Circuits Conf.*, 2021, pp. 386–388, doi: 10.1109/ISSCC42613.2021.9365950.

[20] H. Jeon, J. Bang, Y. Jung, I. Choi, and M. Je, "A high DR, DC-Coupled, time-based neural-recording IC with degeneration R-DAC for bidirectional neural interface," *IEEE J. Solid-State Circuits*, vol. 54, no. 10, pp. 2658–2670, Oct. 2019, doi: 10.1109/JSSC.2019.2930903.

[21] H. Chandrakumar and D. Marković, "A 15.2-ENOB 5-kHz BW 4.5- μ W chopped CT ΔΣ -ADC for artifact-tolerant neural recording front ends," *IEEE J. Solid-State Circuits*, vol. 53, no. 12, pp. 3470–3483, Dec. 2018, doi: 10.1109/JSSC.2018.2876468.

[22] J.-S. Bang, H. Jeon, M. Je, and G.-H. Cho, "A 6.5μW 92.3dB-DR biopotential-recording front-end with 360mVpp linear input range," in *Proc. Symp. VLSI Circuits Dig. Tech. Papers*, 2018, Art. no. 2.

[23] P. R. Kinget, "Scaling analog circuits into deep nanoscale CMOS: Obstacles and ways to overcome them," in *Proc. IEEE Custom Integr. Circuits Conf.*, 2015, pp. 1–8, doi: 10.1109/CICC.2015.7338394.

[24] C. Lee *et al.*, "A 6.5-μW 10-kHz BW 80.4-dB SNDR G_m-C-based CT ΔΣ modulator with a feedback-assisted G_m linearization for artifact-tolerant neural recording," *IEEE J. Solid-State Circuits*, vol. 55, no. 11, pp. 2889–2901, Nov. 2020, doi: 10.1109/JSSC.2020.3018478.

[25] C. Pochet, J. Huang, P. P. Mercier, and D. A. Hall, "28.4 A 400mVpp 92.3 dB-SNDR 1kHz-BW 2nd-Order VCO-based exg-to-Digital front-end using a multiphase gated-inverted ring-oscillator quantizer," in *Proc. IEEE Int. Solid- State Circuits Conf.*, 2021, pp. 392–394, doi: 10.1109/ISSCC42613.2021.9365985.

[26] G. Taylor and I. Galton, "A reconfigurable mostly-digital delta-sigma ADC with a worst-case FOM of 160 dB," *IEEE J. Solid-State Circuits*, vol. 48, no. 4, pp. 983–995, Apr. 2013, doi: 10.1109/JSSC.2013.2239113.

[27] Y. Zhong *et al.*, "A second-order purely VCO-based CT ΔΣ ADC using a modified DPLL structure in 40-nm CMOS," *IEEE J. Solid-State Circuits*, vol. 55, no. 2, pp. 356–368, Feb. 2020, doi: 10.1109/JSSC.2019.2948008.

[28] V. Dhanasekaran *et al.*, "A continuous time multi-bit ΔΣ ADC using time domain quantizer and feedback element," *IEEE J. Solid-State Circuits*, vol. 46, no. 3, pp. 639–650, Mar. 2011, doi: 10.1109/JSSC.2010.2099893.

[29] K. Reddy, S. Dey, S. Rao, B. Young, P. Prabha, and P. K. Hanumolu, "A 54mW 1.2GS/s 71.5dB SNDR 50MHz BW VCO-based CT ΔΣ ADC using dual phase/frequency feedback in 65nm CMOS," in *Proc. Symp. VLSI Circuits*, 2015, pp. C256–C257, doi: 10.1109/VLSIC.2015.7231278.

[30] K. Reddy *et al.*, "A 16-mW 78-dB SNDR 10-MHz BW ct$\delta\sigma$ ADC using residue-cancelling VCO-based quantizer," *IEEE J. Solid-State Circuits*, vol. 47, no. 12, pp. 2916–2927, Dec. 2012, doi: 10.1109/JSSC.2012.2218062.

[31] E. Gutierrez, P. Rombouts, and L. Hernandez, "Why and how VCO-based ADCs can improve instrumentation applications," in *Proc. 25th IEEE Int. Conf. Electron., Circuits Syst.*, 2018, pp. 101–104, doi: 10.1109/ICECS.2018.8618004.

[32] C. Tu, Y. Wang, and T. Lin, "A 0.06mm2± 50mV range −82dB THD chopper VCO-based sensor readout circuit in 40nm CMOS," in *Proc. Symp. VLSI Circuits*, 2017, pp. C84–C85, doi: 10.23919/VLSIC.2017.8008558.

[33] Y. Zhong *et al.*, "A second-order purely VCO-based CT ΔΣ ADC using a modified DPLL structure in 40-nm CMOS," *IEEE J. Solid-State Circuits*, vol. 55, no. 2, pp. 356–368, Feb. 2020, doi: 10.1109/JSSC.2019.2948008.

[34] "Understanding delta-sigma data converters | IEEE eBooks | IEEE xplore." Accessed: Jul. 31, 2021. [Online]. Available: https://ieeexplore.ieee.org/book/5264508

[35] A. Jayaraj, M. Danesh, S. T. Chandrasekaran, and A. Sanyal, "Highly digital second-order $\Delta\Sigma$ VCO ADC," *IEEE Trans. Circuits Syst. I*, vol. 66, no. 7, pp. 2415–2425, Jul. 2019, doi: 10.1109/TCSI.2019.2898415.

[36] A. Jayaraj, M. Danesh, S. T. Chandrasekaran, and A. Sanyal, "76-dB DR, 48 fJ/Step second-order VCO-Based Current-to-Digital converter," *IEEE Trans. Circuits Syst. I: Regular Papers*, vol. 67, no. 4, pp. 1149–1157, Apr. 2020, doi: 10.1109/TCSI.2019.2941956.

[37] A. Elshazly, S. Rao, B. Young, and P. K. Hanumolu, "A noise-shaping Time-to-Digital converter using switched-ring oscillators—Analysis, design, and measurement techniques," *IEEE J. Solid-State Circuits*, vol. 49, no. 5, pp. 1184–1197, May 2014, doi: 10.1109/JSSC.2014.2305651.

[38] B. Drost, M. Talegaonkar, and P. K. Hanumolu, "Analog filter design using ring oscillator integrators," *IEEE J. Solid-State Circuits*, vol. 47, no. 12, pp. 3120–3129, Dec. 2012, doi: 10.1109/JSSC.2012.2225738.

[39] M. Z. Straayer and M. H. Perrott, "A multi-path gated ring oscillator TDC with first-order noise shaping," *IEEE J. Solid-State Circuits*, vol. 44, no. 4, pp. 1089–1098, Apr. 2009, doi: 10.1109/JSSC.2009.2014709.

[40] X. Yi, Z. Liang, C. C. Boon, G. Feng, F. Meng, and K. Yang, "An inverted ring oscillator noise-shaping Time-to-Digital converter with in-band noise reduction and coherent noise cancellation," *IEEE Trans. Circuits Syst. I: Regular Papers*, vol. 67, no. 2, pp. 686–698, Feb. 2020, doi: 10.1109/TCSI.2019.2949732.

[41] C.-W. Yao *et al.*, "A 14-nm 0.14-psrms Fractional-N digital PLL with a 0.2-ps resolution ADC-Assisted coarse/fine-conversion chopping TDC and TDC nonlinearity calibration," *IEEE J. Solid-State Circuits*, vol. 52, no. 12, pp. 3446–3457, Dec. 2017, doi: 10.1109/JSSC.2017.2742518.

[42] S. T. Chandrasekaran and A. Sanyal, "Stochastic ΔΣ VCO-ADC utilizing 4× staggered averaging," in *Proc. IEEE Int. Symp. Circuits Syst.*, 2020, pp. 1–5, doi: 10.1109/ISCAS45731.2020.9180835.

[43] M. J. M. Pelgrom, A. C. J. Duinmaijer, and A. P. G. Welbers, "Matching properties of MOS transistors," *IEEE J. Solid-State Circuits*, vol. 24, no. 5, pp. 1433–1439, Oct. 1989, doi: 10.1109/JSSC.1989.572629.

[44] A. Sheikholeslami, "Process variation and pelgrom's law [Circuit intuitions]," *IEEE Solid-State Circuits Mag.*, vol. 7, no. 1, pp. 8–9, Winter 2015, doi: 10.1109/MSSC.2014.2369331.

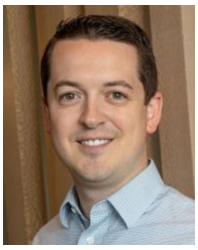
[45] H. Omran, H. Alahmadi, and K. N. Salama, "Matching properties of femtofarad and sub-femtofarad MOM capacitors," *IEEE Trans. Circuits Syst. I: Regular Papers*, vol. 63, no. 6, pp. 763–772, Jun. 2016, doi: 10.1109/TCSI.2016.2537824.

[46] A. C. Sun, E. Alvarez-Fontecilla, A. G. Venkatesh, E. Aronoff-Spencer, and D. A. Hall, "High-Density redox amplified coulostatic discharge-based biosensor array," *IEEE J. Solid-State Circuits*, vol. 53, no. 7, pp. 2054–2064, Jul. 2018, doi: 10.1109/JSSC.2018.2820705.

Corentin Pochet (Student Member, IEEE) received the B.S. and M.E. degrees in electrical engineering from the joint program between the Université Libre de Bruxelles and the Vrije Universiteit Brussel, Brussels, Belgium, in 2014 and 2016, respectively. He is currently working toward the Ph.D. degree in electrical and computer engineering with the University of California at San Diego, La Jolla, CA,USA. His research interests include designing low-power analog front-end circuits and time-based analog-to-digital converters for wearable and biomedical applications. Mr. Pochet was the recipient of the Belgian American Education Foundation (B.A.E.F) Henri Benedictus Fellowship in 2016.

Jiannan Huang (Member, IEEE) received the B.S. degree in electrical engineering from the University of Michigan, Ann Arbor, MI, USA, with outstanding achievement, and Shanghai Jiao Tong University, Shanghai, China, in 2016, and the M.S. and Ph.D. degrees in electrical and computer engineering from the University of California, San Diego, La Jolla, CA, USA, in 2018 and 2021, respectively.

He has held internship positions with Analog Devices, Wilmington, MA, USA, MaXentric Technologies, La Jolla, and Movellus Circuits, Ann Arbor, MI, where he worked on high-performance, low-power mixed-signal circuits. In 2021, he joined Qualcomm Inc., San Diego, as an Analog or mixed-signal Design Engineer. His research interests include analog or mixed-signal integrated circuits with a particular focus on developing high-resolution VCO-based ADCs using digital calibrations.



Patrick P. Mercier (Senior Member, IEEE) received the B.Sc. degree in electrical and computer engineering from the University of Alberta, Edmonton, AB, Canada, in 2006, and the S.M. and Ph.D. degrees in electrical engineering and computer science from the Massachusetts Institute of Technology (MIT), Cambridge, MA, USA, in 2008 and 2012, respectively.

He is currently an Associate Professor in electrical and computer engineering with the University of California, San Diego, CA, USA, where he is also the Co-Director of the Center for Wearable Sensors and the Site Director of the Power Management Integration Center. His research interests include the design of energy-efficient microsystems, focusing on the design of RF circuits, power converters, and sensor interfaces for miniaturized systems and biomedical applications.

Prof. Mercier was the recipient of the Natural Sciences and Engineering Council of Canada (NSERC) Julie Payette Fellowship in 2006, NSERC Postgraduate Scholarships in 2007 and 2009, Intel Ph.D. Fellowship in 2009, 2009 IEEE International Solid-State Circuits Conference (ISSCC) Jack Kilby Award for Outstanding Student Paper at ISSCC 2010, Graduate Teaching Award in Electrical and Computer Engineering with UCSD in 2013, Hellman Fellowship Award in 2014, Beckman Young Investigator Award in 2015, DARPA Young Faculty Award in 2015, UC San Diego Academic Senate Distinguished Teaching Award in 2016, Biocom Catalyst Award in 2017, NSF CAREER Award in 2018, National Academy of Engineering Frontiers of Engineering Lecture in 2019, and San Diego County Engineering Council Outstanding Engineer Award in 2020. From 2015 to 2017, he was an Associate Editor for IEEE TRANSACTIONS ON VERY LARGE SCALE INTEGRATION (TVLSI). Since 2013, he has been an Associated Editor for IEEE TRANSACTIONS ON BIOMEDICAL CIRCUITS AND SYSTEMS (TBioCAS), and is currently a Member of the ISSCC International Technical Program Committee, the CICC Technical Program Committee, the VLSI Symposium Technical Program Committee, and an Associate Editor for IEEE SOLID-STATE CIRCUITS LETTERS. Prof. Mercier was the Co-Editor of the *Ultra-Low-Power Short-Range Radios* (Springer, 2015), *Power Management Integrated Circuits* (CRC Press, 2016), and *High-Density Electrocortical Neural Interfaces* (Academic Press, 2019).

Drew A. Hall (Senior Member, IEEE) received the B.S. degree in computer engineering (with Hons.) from the University of Nevada, Las Vegas, NV, USA, in 2005, and the M.S. and Ph.D. degrees in electrical engineering from Stanford University, Stanford, CA, USA, in 2008 and 2012, respectively.

From 2011 to 2013, he was a Research Scientist with the Integrated Biosensors Laboratory, Intel Corporation, Santa Clara, CA. Since 2013, he has been with the Department of Electrical and Computer Engineering, University of California, San Diego, CA, where he is currently an Associate Professor. His research interests include bioelectronics, biosensors, analog circuit design, medical electronics, and sensor interfaces.

Dr. Hall won First Place in the Inaugural International IEEE Change the World Competition and First Place in the BME-IDEA invention competition, both in 2009. He was the recipient of the Analog Devices Outstanding Designer Award in 2011, Undergraduate Teaching Award in 2014, Hellman Fellowship Award in 2014, NSF CAREER Award in 2015, and NIH Trailblazer Award in 2019. He is also a Tau Beta Pi Fellow. He has been an Associate Editor for IEEE TRANSACTIONS ON BIOMEDICAL INTEGRATED CIRCUITS since 2015, a Member of the CICC Technical Program Committee since 2017, a Member of the ISSCC Technical Program Committee since 2020, and an Associate Editor for IEEE SOLID-STATE CIRCUITS LETTERS since 2021.