A 16×20 Electrochemical CMOS Biosensor Array with In-Pixel Averaging Using Polar Modulation

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***Abstract*—Biosensors based on electrochemical impedance spectroscopy (EIS), an ultra-sensitive, label-free sensing technique, are a promising technology for precise and rapid disease diagnosis at the point-of-care (POC). However, EIS usually requires mixers and lock-in detection to measure both the magnitude and phase of the complex impedance. To address this issue, we report a 16×20 electrochemical biosensor array with on-chip sensors that implements a polar-mode measurement method that allows the readout circuitry to be mostly digital and small enough to fit within a 140×140 µm² pixel. The architecture enables in-pixel digitization and accumulation, which increases the SNR by 10 dB for each 10× increase in readout time. Implemented in a 0.18 µm process, the 3×4 mm² chip achieves state-of-the-art performance with an rms phase error of 0.04% at 50 kHz and was used to measure hybridization of Zika virus oligonucleotides.**

Keywords— point-of-care (POC); electrochemical impedance spectroscopy (EIS); biosensor array; phase-to-digital converter

I. Introduction

Point-of-care (POC) testing is essential to halt the spread of deadly infectious diseases (e.g., Ebola, Zika, etc.) and is needed for rapid and accurate screening both in and outside of clinical settings. Label-free bioassays are desirable for POC testing as they have fewer reagents and assay steps resulting in lower cost and ease of use. Electrochemical impedance spectroscopy (EIS) is an especially promising label-free sensing technique due to both its sensitivity and the scalability of electrochemical sensors that can be fabricated using standard semiconductor processes. Electrochemical sensors, particularly EIS-based, have been applied to many applications including antibody-antigen binding events and DNA hybridization [1]–[5].

These EIS sensors operate by measuring the impedance change at the interface between an electrode and an electrolytic solution that changes due to a binding event on the surface. Conventional EIS architectures contain electrode arrays with column level or off-chip quadrature mixers and lock-in detection to perform the measurement of both the real and imaginary parts of the impedance [1]–[3]. However, EIS assays are typically constructed such that only a single component of the sensor's impedance is modulated by binding events, i.e. the change of the diffusion layer capacitor, C_O, as DNA hybridizes (Fig. 1a). The capacitance shift due to DNA hybridization causes a significant and proportional change to the phase with only a minor variation in the amplitude. Thus, only part of the complex impedance, in this case the phase, is required for binding detection allowing the readout circuitry to be simplified.

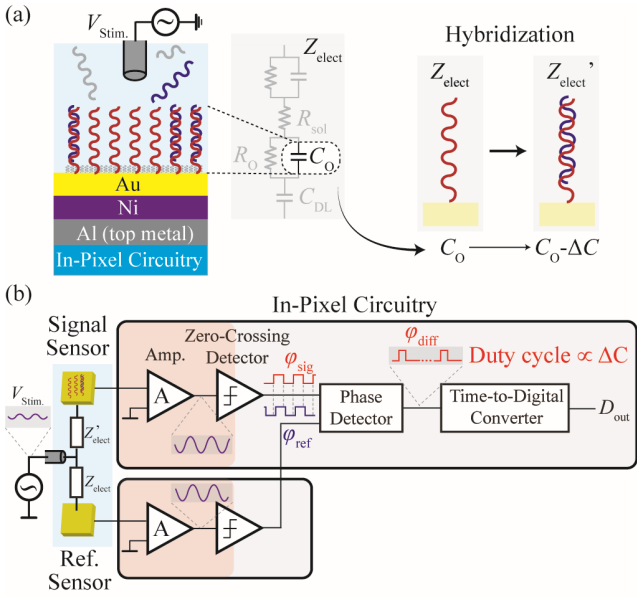

Fig. 1. (a) Concept of polar mode biosensor where hybridization changes the sensor capacitance, and (b) architecture showing in-pixel measurement by detecting the phase change between signal and reference electrodes.

Leveraging this property, we report a high-density 16×20 impedance biosensor array with on-chip sensors and in-pixel circuitry that uses a polar mode impedance measurement scheme to improve both the scalability and sensitivity. The in-pixel circuitry (Fig. 1b) operates as follows: An external Ag/AgCl electrode applies a 10 mV sinusoidal excitation at a frequency, f_{stim}, between 5 kHz and 1 MHz to the electrolytic solution. Each sensor has a 100×100 µm² gold electrode where the signal sensors are functionalized with single-stranded DNA and the reference sensors are unfunctionalized. The corresponding induced current is measured with a transimpedance amplifier and then converted to a rail-to-rail signal by a zero-crossing detector. The remaining signal path consists solely of digital blocks with a phase detector determining the relative phase shift caused by the change of electrode impedance. This phase shift is quantized and averaged using a time-to-digital converter with first-order noise-shaping.

The rest of the paper is organized as follows. Section II describes the architecture of the in-pixel circuitry and Section III shows the implementation. Section IV presents measurement results, and a conclusion is given in Section V.

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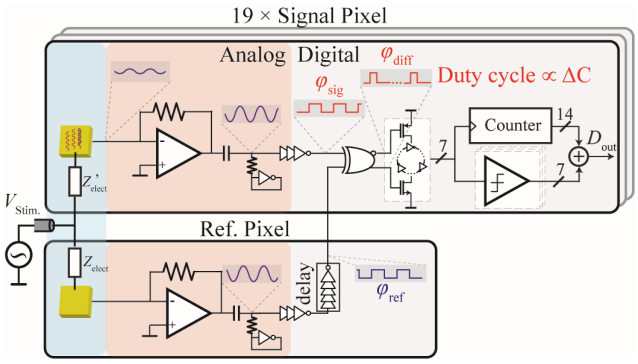

Fig. 2. Architecture of the proposed system with in-pixel digitization.

II. Polar Modulaton Architecture

A. Polar Modulation

Fig. 2 depicts the architecture of the chip. First, the induced currents are measured by a resistive feedback transimpedance amplifier (R-TIA). The output of the R-TIA is bandpass filtered using the impedance of the sensor and the R-TIA bandwidth to limit the noise. To preserve only the zero crossings, an AC-coupling capacitor in conjunction with a self-biased inverter sized the same as the first inverter in the chain are connected to R-TIA output. The inverter chain maintains the zero crossings while transforming the signal into a rail-to-rail square wave, φ_{sig} and φ_{ref} from the signal and reference electrode, respectively. The phase of the signal pixel φ_{sig} is then compared with the phase φ_{ref} from an identical pixel attached to a reference sensor (one for each column in the array that functions as the experimental control) via a phase detector, i.e. an XOR logic gate, to produce a pulse φ_{diff} with a duty cycle linearly proportional to the phase difference. The reference pixels enable a pseudo-differential measurement to cancel common-mode variations (to the first order) such as temperature drift, process variation, and non-specific binding. An additional delay is included in the reference path to remove the dead-zone caused by mismatch and noise such that a zero-phase difference still produces a well-defined minimum XOR pulse. A time-to-digital converter (TDC) that consists of a first-order noise-shaped gated ring oscillator (GRO) converts the pulses to a digital output D_{out}. Since the sinusoidal stimulus waveform is continuous, the TDC accumulates consecutive XOR pulses.

B. In-Pixel Averaging Time-to-Digital Converter

The TDC performs the pulse width to digital conversion of φ_{diff} by only turning on the GRO when φ_{diff} is high, as shown in Fig. 3(a). The phase changes of one stage in the GRO in each stimulation period ($T_{stim} = 1/f_{stim}$) is:

$$\varphi_{GRO} = 2\pi f_{GRO} \times T_{stim} \times (Duty\ Cycle\ of\ \varphi_{diff})\ \text{rad}, \quad (1)$$

where f_{GRO} is the free running frequency of the GRO. Therefore, the duty cycle of φ_{diff} can be obtained by quantizing and normalizing φ_{GRO} to f_{GRO}, and the quantized phase of the GRO provides inherent first-order noise-shaping since φ_{GRO} is an integrated version of φ_{diff} when the GRO is not reset [6].

Each XOR pulse contains the desired phase difference, t_{sig}, due to the sensor impedance change, but is corrupted by noise, $t_{n1,2}$, from the sensor, R-TIA, and other circuitry that is

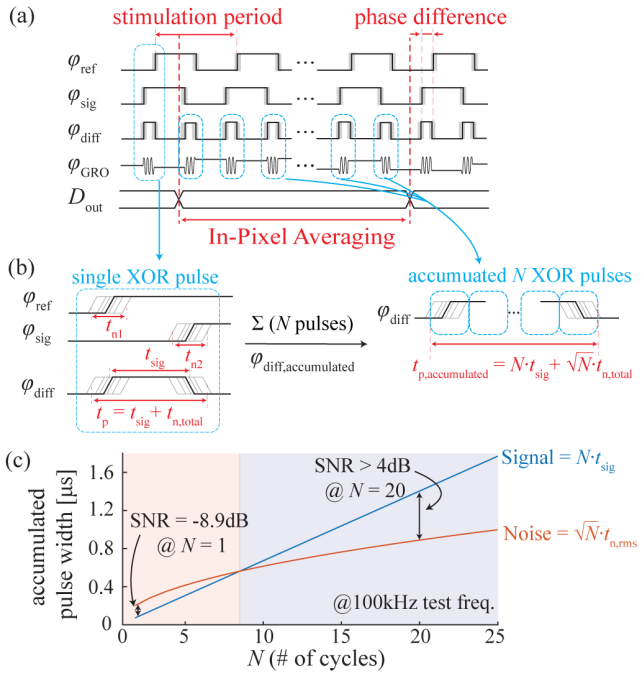

Fig. 3. (a) Waveforms showing concept of phase difference averaging by accumulating several XOR pulses. (b) A single XOR pulse with jitter before and after accumulation, and (c) simulation results showing the SNR increasing 3dB with every 2× integration time.

subsequently converted into jitter as shown in Fig. 3(b). To improve the SNR of the phase measurements, multiple XOR pulses are accumulated in the GRO. Since the phase noise is white within the frequency range of interest, the accumulation of N XOR pulses scales the signal amplitude by N while the noise is only scaled by $\sqrt{N}$, thereby improving the SNR by 3 dB when the integration time is doubled. This SNR improvement enabled the noise requirements of the TIA and TDC to be relaxed since it is no longer necessary to lower the phase noise of a single pulse down to sub-ns for <0.1% TDC error. As simulated in Fig. 3 (c) with values from [1] and a jitter of 200 ns_{rms}, the SNR increases from -8.9 dB to 4 dB by increasing the integration time of the TDC from 10 μs (a single XOR pulse) to 200 μs (20 XOR pulses) at a stimulus frequency of 100 kHz.

III. Implementation

The EIS biosensor chip contains 16×20 pixels with the first row serving as reference pixels and the remaining 19 rows as signal pixels. Each reference pixel generates a reference signal for the signal pixels in the same column. The area of a pixel is 140×140 μm^2 with an electrode area of 100×100 μm^2 using the top metal layer without any passivation. All the circuitry, including R-TIA, inverter chain, and in-pixel averaging TDC are placed beneath this electrode. The R-TIA was designed with a gain of 100 kΩ and implemented using a two-stage, folded cascode amplifier, as shown in Fig. 4. The amplifier was designed with a flicker noise corner frequency of less than 1 kHz by sizing the input devices and using source degeneration on the load devices. The second stage of the amplifier provides the necessary low output impedance to drive the feedback resistor. In simulation, the amplifier in open-loop achieves 100 dB DC gain and 36 MHz unity-gain bandwidth while consuming 142 μW.

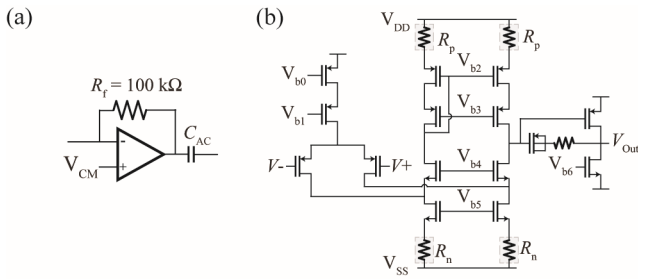

Fig. 4. Schematic of the (a) R-TIA with an AC-coupling capacitor and (b) folded cascode amplifier with source degeneration to reduce flicker noise.

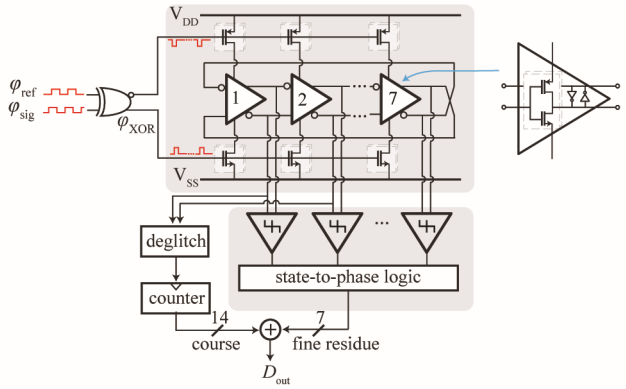

Fig. 5. Schematic of the in-pixel averaging phase-to-digital converter using a 7-stage psuodo-differential gated-ring oscillator.

The application and the polar modulation scheme are tolerant of mismatch (e.g., the offset of the amplifier, the delay of inverter chain, etc.) because any mismatch is converted into a constant phase shift at the output of the R-TIA and a constant duty cycle offset at the output of the XOR. However, the XOR does not provide differentiation between phase leading or lagging between the reference and signal pixels, so an explicit delay chain of 250 ns delay was added to guarantee a minimum pulse width at the XOR output even with noise and mismatch from the in-pixel circuitry (i.e., the signal pixel always sets the rising edge of the pulse whereas the reference pixel determines the falling edge). The inverter chain in the reference pixels were sized larger to minimize mismatch between the reference and the signal pixels. This reduced offset also allows the delay in the reference pixel to be shorter thereby reducing its area.

The TDC was implemented as a 7-stage pseudo-differential GRO designed to balance the noise (white and flicker) and power trade-off, as shown in Fig. 5. When the XOR output is high, this GRO converts the duty cycle of the XOR pulse to phase with a gain of 609 krad/%. Multiple XOR pulses are accumulated in the phase domain, and the phase is stored as voltage on the capacitance at the output node of each stage when the GRO is turned off. The GRO was sized such that the leakage current introduces negligible error in the off state. For coarse phase-to-digital conversion, a counter is used to quantize the phase change φ_{GRO} of every 2π rad of the oscillation. Measuring the state of the ring oscillator using clocked sense amplifiers adds $\pi/7$ fine quantization levels. The clock for the sense amplifier was synchronized with the readout frequency of f_{stim}/N rather than f_{stim} to minimize kickback noise to the GRO. The counter was designed with a 14-bit depth to be able to handle a

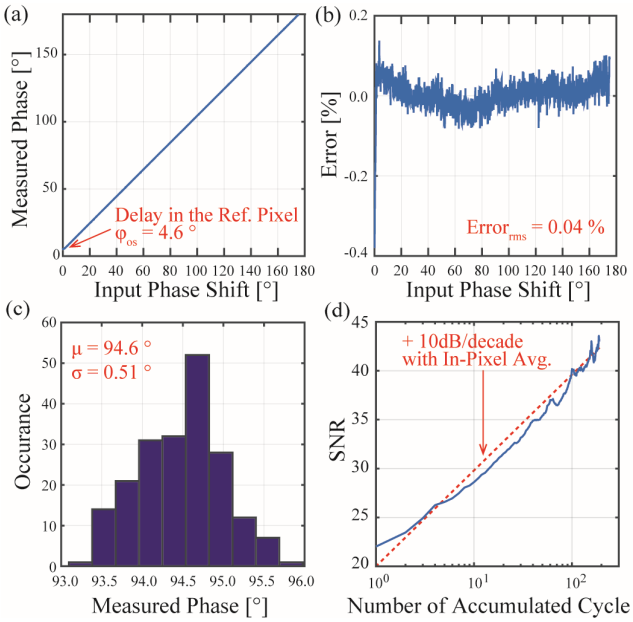

Fig. 6. Characterization of the in-pixel circuitry with a mock cell: (a) transfer function and (b) linearity, (c) noise of single cycle, and (d) SNR improvement with the in-pixel averaging by accumulating multiple cycles.

maximum integration time of 10 ms without overflowing. The combined coarse and fine data from the counter and the comparator conversions respectively provide a 21-bit digital output for each of the pixels. The output of each pixel is readout using a serial peripheral interface (SPI) bus, and the output of 16 pixels in each row are concatenated to a 1-bit width and 336-bit length digital output format. Therefore, the clock frequency for the SPI is 336× the readout rate.

IV. Measurement Results

A. Electrical Measurements

The performance of the in-pixel circuitry was characterized using a mock electrochemical cell, as shown in Fig. 1(a), made from a network of passive components for both the signal and reference channels. This mock cell has an equivalent impedance of a gold-plated 100×100 μm^2 electrode (the same as the on-chip electrodes) in a 4×SSC (saline-sodium citrate) buffer. The linearity was measured by applying two sinusoids with a phase shift between the reference and signal pixel using an arbitrary function generator. The results showed an offset of 4.6° (250 ns) matching the designed delay chain in the reference pixel (Fig. 6a), and an RMS linearity error of 0.04% over a phase full scale range of 175.4° (Fig. 6b) at a test frequency of 50 kHz. The noise was characterized by providing a constant 90° phase shift between the reference and a signal pixel. Fig. 6(c) shows a histogram of a single counter output with an RMS noise of 0.51°, and measured data demonstrating that the in-pixel averaging technique provides an SNR improvement of +10dB per 10× integration time (Fig. 6d).

B. Biological Measurements

Before making biological measurements, each sensor was plated with gold for electrochemical compatibility using a standard ENIG process (Stapleton Technologies, Inc.) [1], [2]. To verify the operation of the sensor array, each bare gold

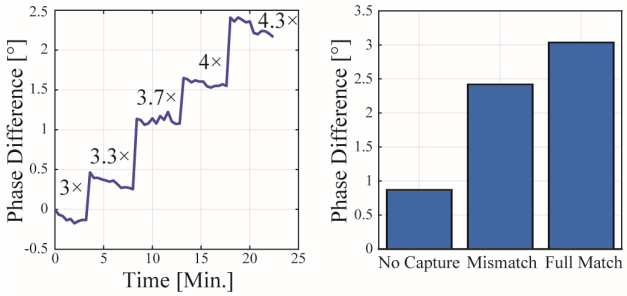

Fig. 7. (a) Phase change due to increasing buffer strength of a single sensor and (b) average phase change due to hybridization, where Zika ssDNA binds to the surface.

electrode in the array was used to measure the phase change at varying buffer strengths that shift the solution resistance and double-layer capacitances of the electrode's impedance model. As demonstrated in Fig. 7(a), where 1 µL of 20× SSC buffer was repeatedly added to an initial sample of 45 µL 3× SSC and measured by the chip, the change in impedance due to the increase in the buffer strength from 3× to 4.3× causes a direct and detectable change in phase.

Next, a single sensor array was functionalized with two types of 30 nucleotide single-stranded DNA (ssDNA) capture probes [7]. The first is the complimentary capture strand (5'GCTTGGCCAGGTCACTCATTGAAAATCCTC), which is intended to fully capture a target DNA probe used to detect the Zika virus. The second is the 15-base pair mismatch capture strand (5'GCTTGGCCAGGTCACGTGCCTGGGGGCAAGA), where only half of the oligonucleotide is complimentary to the target causing only partial binding. During the hybridization step, 50 µL of 1 µM target oligonucleotide was added and impedance measurements were made to detect the binding of the target to the probes. As shown in Fig. 7(b), the on-chip sensors can measure this hybridization in real-time and distinguish between complimentary and mismatched strands.

The chip was fabricated in a TSMC 0.18 µm CMOS process with a 1.8 V supply voltage. Fig. 8 shows an annotated die photo and Table 1 summarizes the performance of this work with prior art. This work achieves the highest pixel density with completely in-pixel analog frontend and quantizer circuity. The polar modulation and in-pixel averaging technique provide 3× less phase error compared to the state-of-the-art allowing ultra-sensitive bioassays.

V. Conclusion

In this paper, we demonstrate a field deployable 16×20 electrochemical CMOS biosensor array for highly scalable label-free nucleic acid testing. The on-chip sensors use a streamlined and highly scalable polar modulation method to monitor bioassay events. The in-pixel circuitry (140×140 µm^2) measures the necessary phase changes of the on-chip sensors using a transimpedance amplifier, zero-crossing detector, and a first-order noise-shaping time-to-digital converter without the need for quadrature signal analysis. This mostly-digital design has the advantage of +10dB noise reduction for each 10× additional data points by using in-pixel averaging and achieves a 0.04% RMS linearity error. Using an alternative impedance

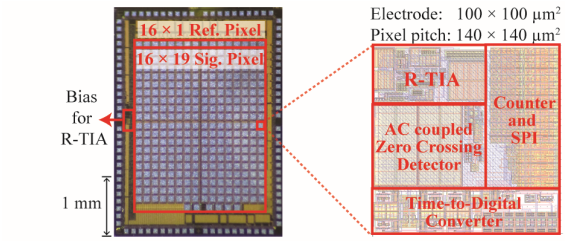

Fig. 8. Chip microphoto and floorplan of a signal pixel.

TABLE I. Comparison with State-of-the-Art CMOS EIS

	JSSC 2009	ISSCC 2010	TBCAS 2012	TBCAS 2017	**This Work**
Tech. [µm]	0.5	0.35	0.13	0.35	**0.18**
Supply [V]	3	3.3	1.2	3.3	**1.8**
On-Chip Electrodes?	No	Yes	Yes	No	**Yes**
Num. Sensors	-	100	64	-	**320**
Num. Readout Channels	1	100	16	1	**320**
Area/Ch. [µm^2]	60,000	10,000*	60,000	70,000	**19,600**
Power [mW]	0.006	84.5	0.35	0.32	**63**
Power/Ch. [µW]	6	845	5.57	320	**197**
ADC	On Chip	Off Chip	In Pixel	In Pixel	**In Pixel**
Freq. Range [Hz]	0.1 - 10^4	10^2 -5×10^7	0.1 - 10^4	10^{-4} - 10^5	**5×10^3 - 10^6**
Quadrature Signal Source Required	Yes	Yes	Yes	No	**No**
Magnitude Error	0.32% @ 10 Hz	-	-	0.28% @ 10 kHz	**N/A**
Phase Error	2.7% @ 1 kHz 38 S/s	-	-	0.12% @ 10 Hz, 10 S/s	**0.04% @ 50 kHz, 24 S/s**

*Require additional off-chip demodulation and quantization circuit.

measurement technique, label-free detection of DNA hybridization was measured with the designed array demonstrating promise for precise and highly scalable biosensing in POC applications.

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