10.2 A 139μW 104.8dB-DR 24kHz-BW CTΔΣM with Chopped AC-Coupled OTA-Stacking and FIR DACs

Somok Mondal[1,2], Omid Ghadami[1], Drew A. Hall[1]

[1]University of California, San Diego, La Jolla, CA
[2]now with Apple, San Diego, CA

Continuous-time delta-sigma modulators (CTΔΣMs) have inherent anti-aliasing, resistive inputs, and relaxed settling requirements making them popular for audio applications. Due to the relatively low bandwidth, the noise-efficiency of the first OTA has a substantial influence on the power and FoM. OTA-stacking is a recently reported technique that improves the noise-current tradeoff in continuous-time amplifiers [1], [2]. This is the central idea behind the proposed CTΔΣM where an AC-coupled stacked OTA improves the noise-efficiency of the first integrator. The ADC with a 3-stack OTA achieves 100.9dB SNDR and 104.8dB DR in a 24kHz bandwidth while consuming 139μW for a state-of-the-art Schreier FoM_{DR} of 187.2dB.

Addressing the noise-efficiency in ΔΣMs has been the focus of several prior works, summarized in Fig. 10.2.1. In [3], FIR DACs enable chopping at lower frequencies, which removes the OTA's 1/*f* noise, but does not reduce the thermal noise. With negative-*R* assistance in [4], the OTA noise is reduced, but incurs additional resistor noise. In [5], a gain stage attenuates the resistor noise, but needs a wide bandwidth to not impact the noise transfer function (NTF). The discrete-time ΔΣM in [6] stacks closed-loop, switched-capacitor amplifiers that reduce the noise like this work, but the implementation limits the OTAs to a single stage (with low gain) and requires a high supply voltage (5.4V). With OTA-stacking, *N* inverters are stacked vertically reusing the same bias current, I_{DC}, as shown in Fig. 10.2.1. In differential-mode, all *N* inverters are decoupled as their source nodes are virtual shorts, while the inputs and outputs are AC shorted, respectively. Hence, all small-signal parameters are in parallel where *N*-fold G_m-boosting results in a 1/*N* reduction of the input-referred noise. Despite the lower noise, stacking comes at the expense of a higher V_{DD} and thus offers only marginal improvements to an amplifier's power efficiency factor (PEF). A single-tailed amplifier's PEF scales as 1+1/*N*, where stacking diminishes the contribution of the tail devices [1]. A tailless version reduces the headroom but sees no PEF improvement with further stacking. The minimum PEF may be realized with a low V_{DD} alone, without stacking. However, an oversampled ADC benefits from both an increase in V_{DD} and stacking since the FoM improves as $10\log(V_{DD})+10\log(N)$. Fundamentally this arises because the PEF captures the tradeoff between the input-referred noise and power, while the Schreier FoM captures the SNDR and power tradeoff.

Having established the merit, implementing OTA-stacking in a CTΔΣM poses several challenges: 1) The AC-coupling blocks DC where an integrator needs high DC-gain. This is readily addressed by upmodulating the signal with chopping. 2) The transient settling response due to the large DAC steps at the modulator's summing node is degraded by the large coupling capacitors. Thus, a multi-level DAC is required to reduce the swing for high linearity. 3) Finally, and most importantly, the OTA has a band-pass response that causes unwanted notches in its frequency response with chopping. This impacts the loop-filter, can potentially degrade the NTF, and, in the worst case, compromises the loop-filter stability. An FIR DAC with multi-level feedback containing spectral nulls solves both of the latter issues. Figure 10.2.2 illustrates the third challenge in more detail. Baseband inputs are upmodulated and processed with constant gain; however, high frequency signals around f_{chop} are downmodulated to DC and filtered. The resulting frequency response exhibits notches at multiples of f_{chop}. While this is not an issue for sensor front-ends that amplify signals at frequencies much lower than f_{chop}, it is problematic in a ΔΣM that must faithfully process high-frequency quantization noise. The most straightforward solution is to set $f_{chop}=f_s$, but this is very power inefficient. FIR DACs offer an additional degree of freedom that can be exploited as they have spectral nulls at multiples of f_s/N_{FIR}, where N_{FIR} is the number of filter taps. As shown in Fig. 10.2.2, with N_{FIR}=8, there are nulls at multiples of f_s/8. This was utilized in [3] to mitigate chopping aliasing issues by selecting $f_{chop}=f_s/2N_{FIR}$. In this work, $f_{chop}=f_s/N_{FIR}$ is used to coincide the notches in the frequency response of the proposed OTA with the nulls of the FIR feedback. Thus, the OTA does not need to process signal content at multiples of f_{chop} making the use of an AC-coupled OTA in a CTΔΣM viable.

The ADC is implemented as a 3rd-order, 1b CTΔΣM (f_s=7.2MHz, OSR=150, SQNR=112dB, R_{in}=13kΩ) using a CIFF-B topology with optimized zeros and 9-tap FIR DACs, as shown in Fig. 10.2.2. For the main FIR DAC, the first tap is zero to allow for a full clock cycle of comparator delay, while the remaining 8 taps are equally weighted. The main path is thus effectively an 8th-tap filter. The auxiliary DAC without the zero tap compensates for the excess loop delay (ELD) of the main DAC. This choice was made because the comparator non-idealities (*e.g.*, signal-dependent delay) degrade the SQNR mostly in the main feedback path and not the auxiliary path. No extra fast path DAC or summing network is needed.

The first integrator, shown in Fig. 10.2.3, is realized by a 4-stage amplifier with feedforward compensation. Two versions of the OTA, a 1- and 3-stack, were designed for comparison. For the tailless 3-stack version, the central inverter is self-biased at V_{DD}/2 and the intermediate devices to reference voltages generated by a replica network. Despite the lack of a tail source to degenerate the common-mode (CM) gain, high common-mode rejection (CMR) is achieved due to the self-feedback in the intermediate differential pairs [1] and the loops biasing the top- and bottom-most differential pairs, along with chopping and filtering. With f_{chop}=900kHz and an OTA -3dB high-pass corner of ~30kHz, CM signals are significantly attenuated (*e.g.*, >50dB at 60Hz). The notch width in the frequency response around multiples of f_{chop} is <60kHz for the stacked-OTA, significantly less than the -3dB width of the FIR feedback nulls (>250kHz). Selection of N_{FIR}=8 considers tradeoffs related to f_{chop}, signal swings, and, importantly, the null width (since higher N_{FIR} lowers f_{chop}, but reduces the null width). With proper $G_{m,main}$:$G_{m,FF}$ ratios of the feedforward stage and an explicit compensation capacitor, C_C, the poles and zeros are placed to avoid multiple gain crossover frequencies across all corners ensuring a phase margin of >70° and a DC-gain >90dB based on simulations. The 1-stack ADC is analogous to the 3-stack version, albeit the input stage is a dual-tail inverter-based OTA with no AC-coupling, 3× more current, and the same input-referred noise. While $R_{in,DAC}$ contributes ~95% of the total noise, the input-G_m draws high power and contributes ~2.5% of the total noise. All other integrators are 3-stage OTAs with nested Miller compensation.

The two ADCs intended for the same resolution were implemented in 65nm CMOS occupying 0.25 and 0.39mm² for the 1- and 3-stack, respectively. Figure 10.2.4 shows the measured SNDR and DR for the 1- and 3-stack ADCs achieving 101.0/104.8dB and 100.9/104.8dB, respectively. The ADC spectra has out-of-band tones at f_s/8.5 and its multiples (likely from the asymmetric 8th- and 9th-tap feedback DACs), in contrast to the out-of-band tones at $f_s/2N_{FIR}$ (from the symmetric feedback) in [3]. These do not limit the in-band performance with the noise floor set by the input resistors. The measured linearity is excellent with >113dB SFDR, the CMRR/PSRR at 60Hz are >95/86dB, respectively, and the alias rejection around f_s is >80dB, as shown in Fig. 10.2.5, along with the power breakdown for both versions. Figure 10.2.6 compares this work to prior art and Fig. 10.2.7 shows an annotated die photo. While the 1-stack version consuming 232μW has a competitive $FoM_{SNDR/DR}$ of 181.1/184.9dB, this is improved by 2.3dB to 183.3/187.2dB with 3-fold stacking and a lower power consumption of 139μW resulting in state-of-the-art performance.

Acknowledgement:
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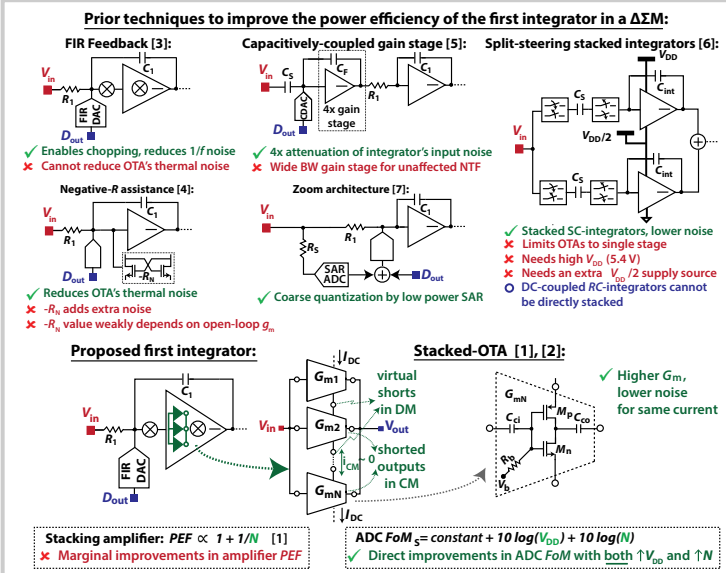

Figure 10.2.1: Summary of prior works and the proposed CTΔΣM with OTA-stacking.

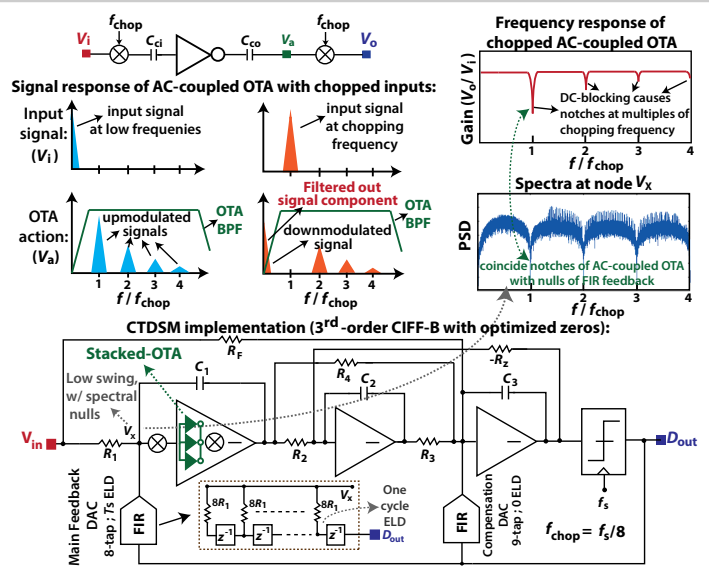

Figure 10.2.2: CTΔΣM with OTA-stacking: Illustration of the key challenge, the proposed solution using FIR feedback, and the CIFF-B implementation.

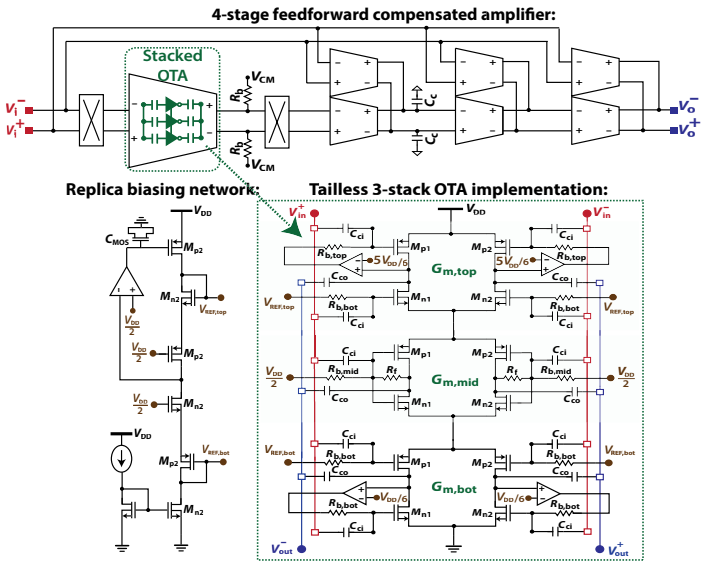

Figure 10.2.3: Implementation of the first integrator with a 4-stage amplifier and the stacked input stage.

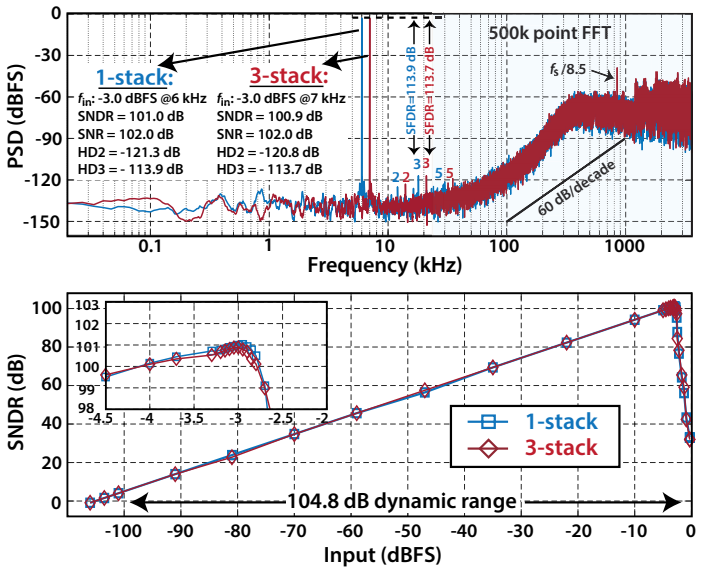

Figure 10.2.4: Measured ADC spectra and dynamic range.

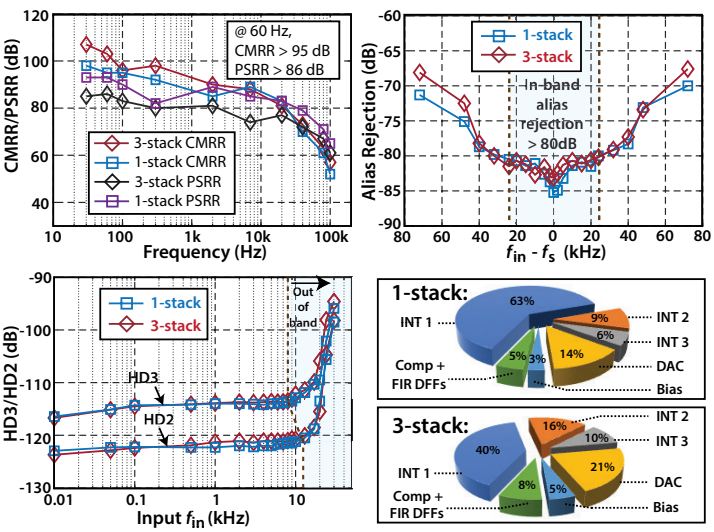

Figure 10.2.5: Measured CMRR/PSRR, anti-aliasing property, linearity, and power breakdown.

	[8] Eland VLSI'20	[4] Jang ISSCC'20	[9] Billa JSSC'20	[7] Gonen VLSI'19	[5] Chandra. ISSCC'18	This Work 1-stack	This Work 3-stack
Topology	DT 2b Zoom	CT 1.5b Neg.-R FIR DAC	CT 1b MASH FIR DAC	CT 1b Zoom	CT 6b w/ gain stage	CT 1b FIR DAC OTA-stacking	
Input	switch-cap	resistive	resistive	resistive	cap-coup.	resistive	
Tech. (nm)	160	65	180	160	40	**65**	**65**
Area (mm^2)	0.27	0.28	0.64	0.27	0.053	**0.25**	**0.39**
Supply (V)	1.8	1.2	1.8	1.8	1.2	**1.2**	**1.2**
BW (kHz)	20	24	24	20	5	**24**	**24**
f_s (MHz)	3.5	8	6.144	5.12	0.2	**7.2**	**7.2**
SNR (dB)	107.5	101	101.7	108.1	94.3	**102.0**	**102.0**
SNDR (dB)	106.5	99.4	100.9	106.4	93.5	**101.0**	**100.9**
DR (dB)	109.8	103.5	104	108.5	96.5	**104.8**	**104.8**
SFDR (dB)	-	110.2	108	-	102.5	**113.9**	**113.7**
Power (μW)	440	134	550	618	4.5	**232**	**139**
FoM_{SNDR}	183.1	181.9	179.6	181.5	184	**181.1**	**183.3**
FoM_{DR}	186.4	186	182.7	183.6	187	**184.9**	**187.2**

FoM_{DR} = DR+10log(BW/Power) FoM_{SNDR} = SNDR+10log(BW/Power)

Figure 10.2.6: Performance summary of the 1- and 3-stack ADCs and comparison to the state-of-the-art.