A 139µW 104.8dB-DR 24kHz-BW CTΔΣM with Chopped AC-coupled OTA-Stacking and FIR DACs

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Speaker Bio

Somok Mondal

B.Tech & **M.Tech**
2013

Indian Institute of Technology, Kharagpur
Electronics & Electrical Communication Engineering

Ph.D.
2020

University of California, San Diego
Electrical and Computer Engineering

ASIC Design Engineer
present

Apple Inc., San Diego

Research Interests

Analog/RF integrated circuits for power-efficient bio-medical and IoT sensor nodes, data-converters

CTΔΣM for high resolution Audio ADCs

Personalized Audio & Entertainment Devices

- Portable far field voice capture devices
- Voice controlled Internet of Thing (IoT) sensors

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Requirements:

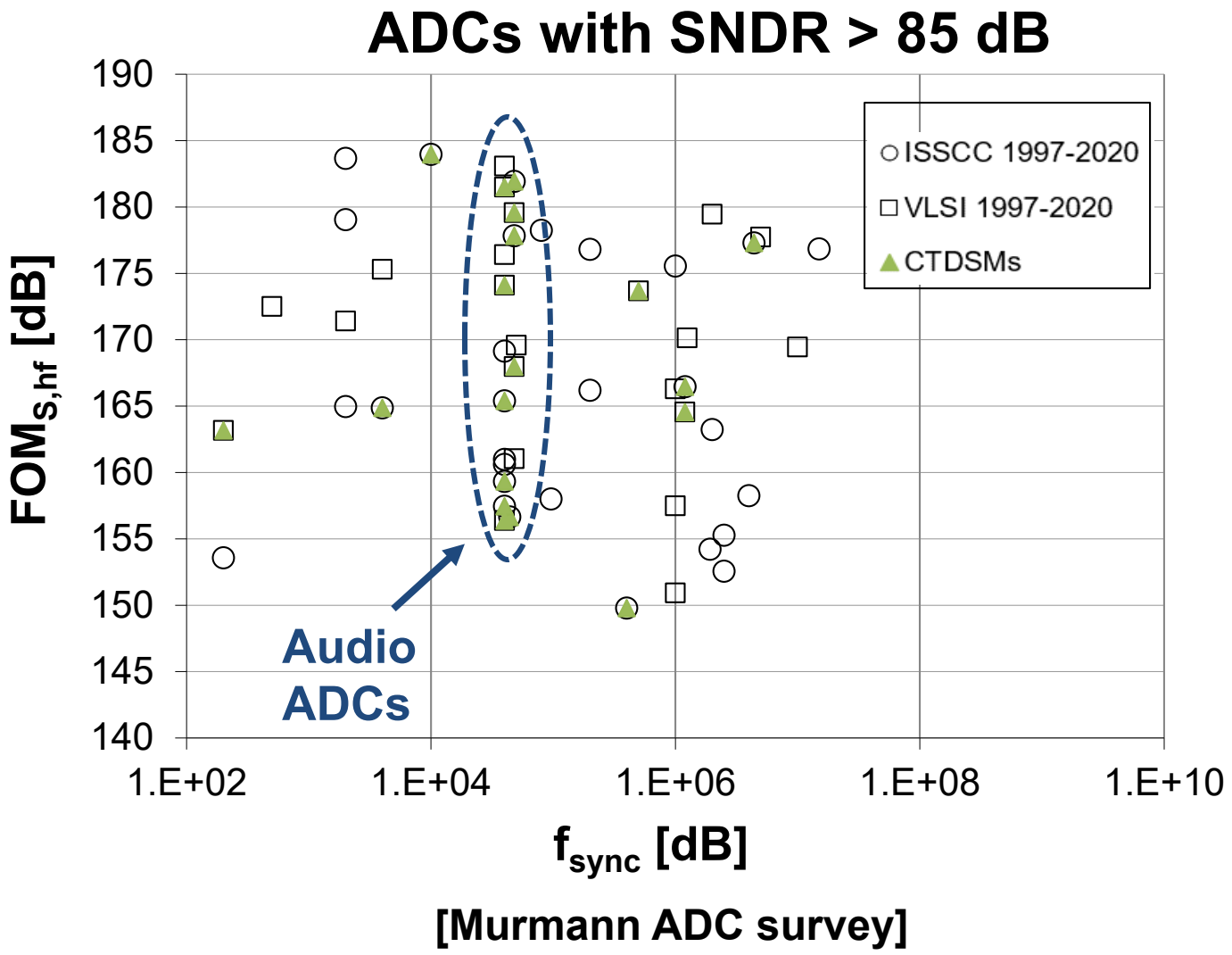
- >100 dB dynamic range
- 16-bit resolution
- 24 kHz bandwidth
- Portable applications

NEED: Low power operation

CTΔΣM for high resolution Audio ADCs

- Resistive inputs
- Inherent anti-aliasing
- Relaxed settling

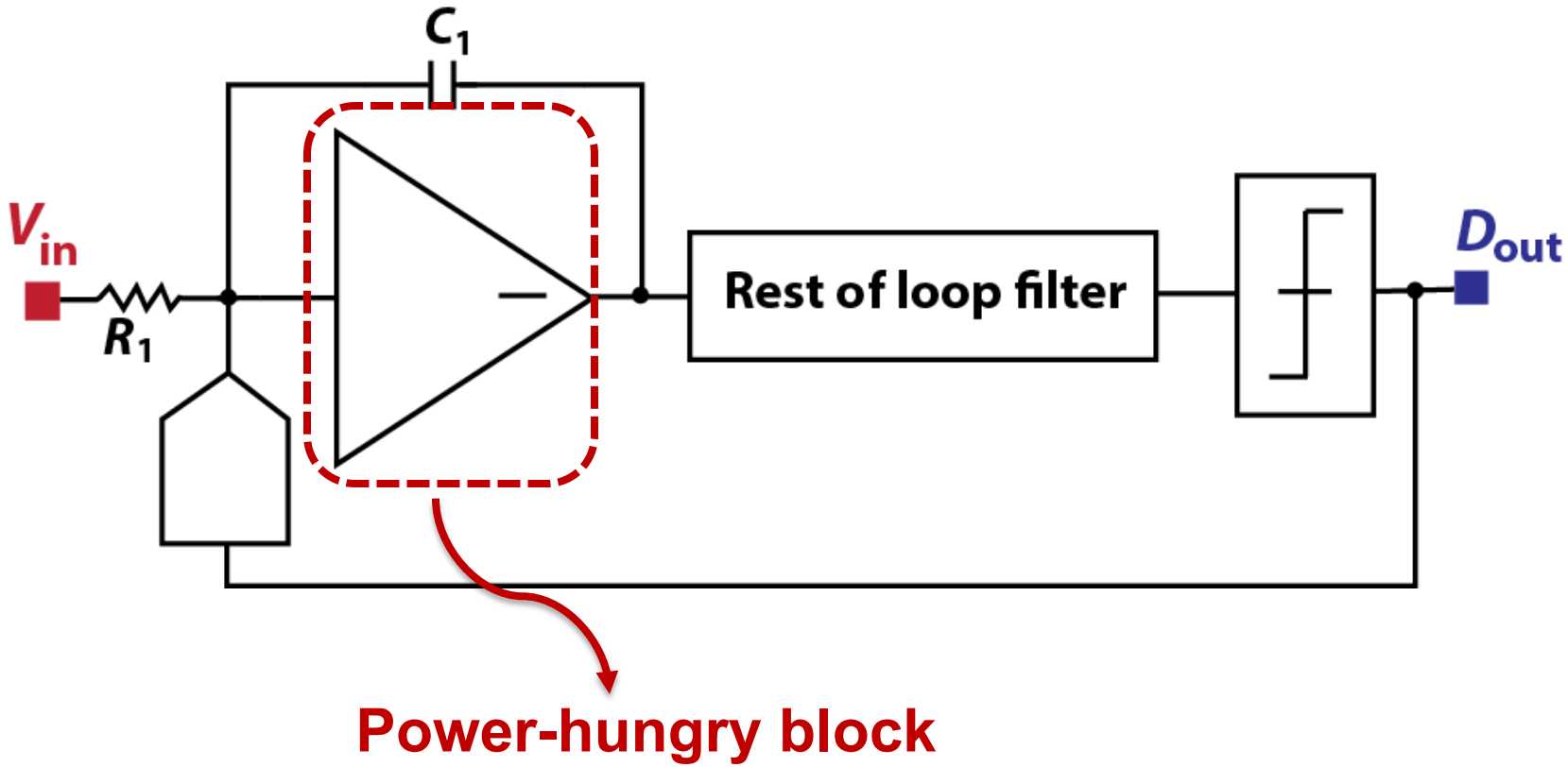
CTΔΣMs are good for power-efficient audio-BW ADCs



Outline

- Motivation and Prior Work
- OTA-Stacking Concept
- Proposed ADC with OTA-Stacking and FIR DACs
- Circuit Implementation
- Measurement Results
- Conclusion

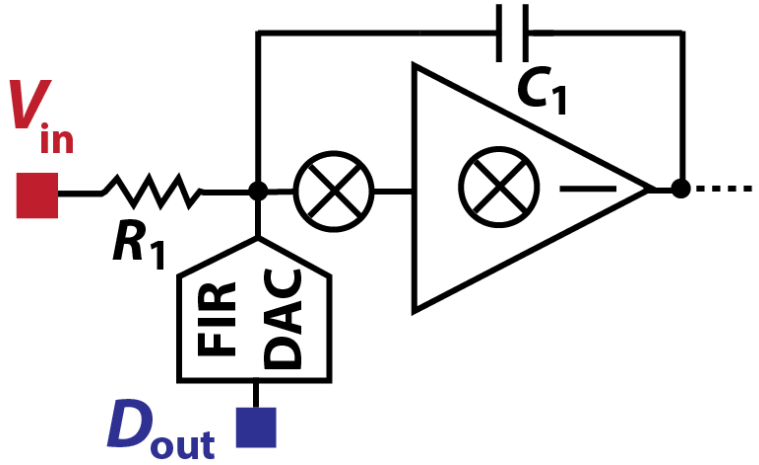
Audio CTΔΣM: Key Limitation



Noise efficiency of the input OTA has a significant influence over the ADC power and FoM

Prior Techniques in ΔΣMs

FIR Feedback [Billa ISSCC'16]:



- ✓ Enables chopping, reduces 1/*f* noise
- ✗ Cannot reduce OTA's thermal noise

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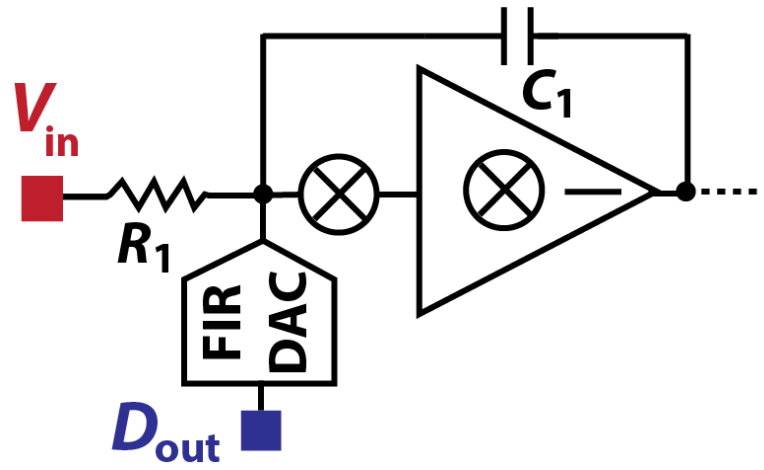

- ✓ Enables chopping, reduces 1/f noise
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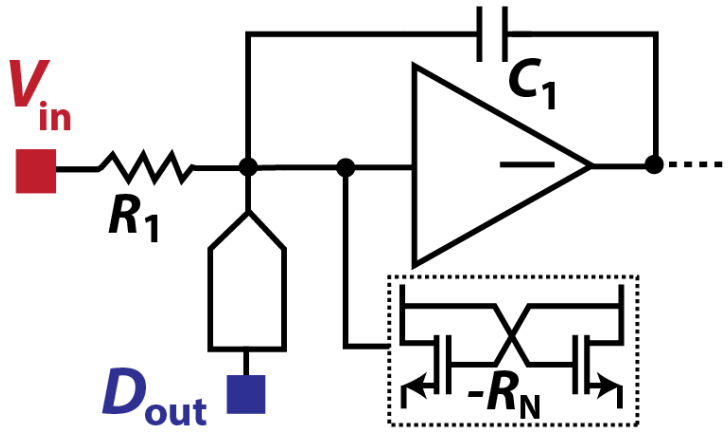
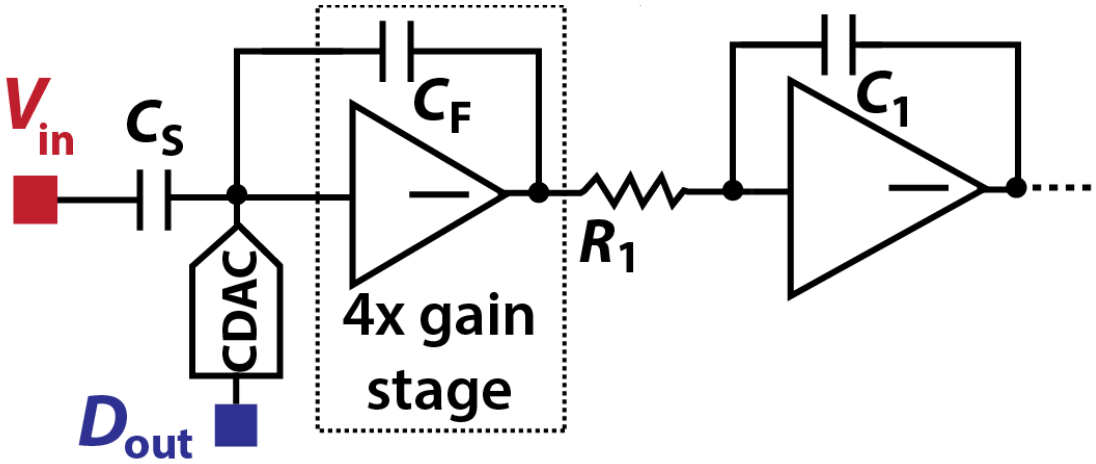
Negative-R assistance [Jang ISSCC'20]:



- ✓ Lowers OTA's thermal noise
- ✗ $-R_N$ adds noise
- ✗ $-R_N$ weakly depends on open-loop g_m

Prior Techniques in ΔΣMs

Cap. gain stage [Chandra. ISSCC'18]:



- ✓ 4x attenuation of integrator's input noise
- ✗ Wide BW gain stage for unaffected NTF

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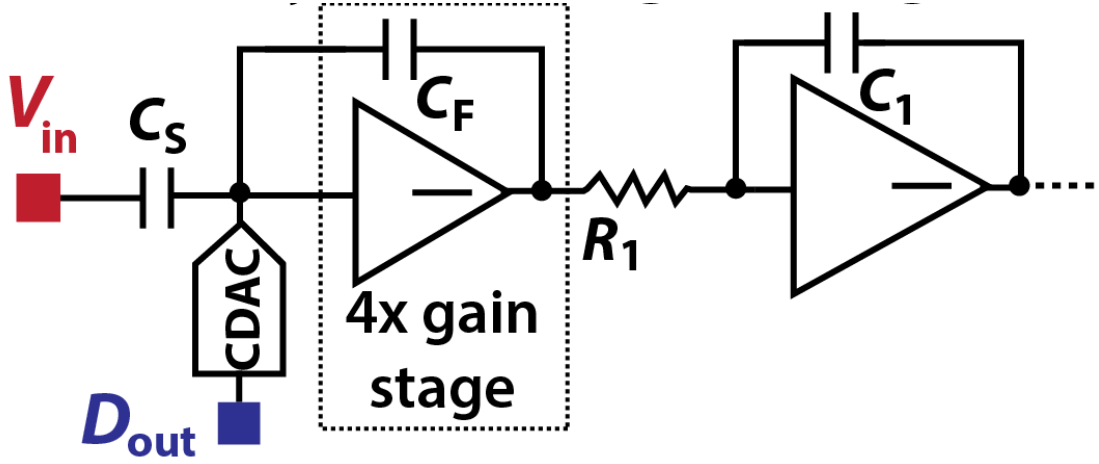

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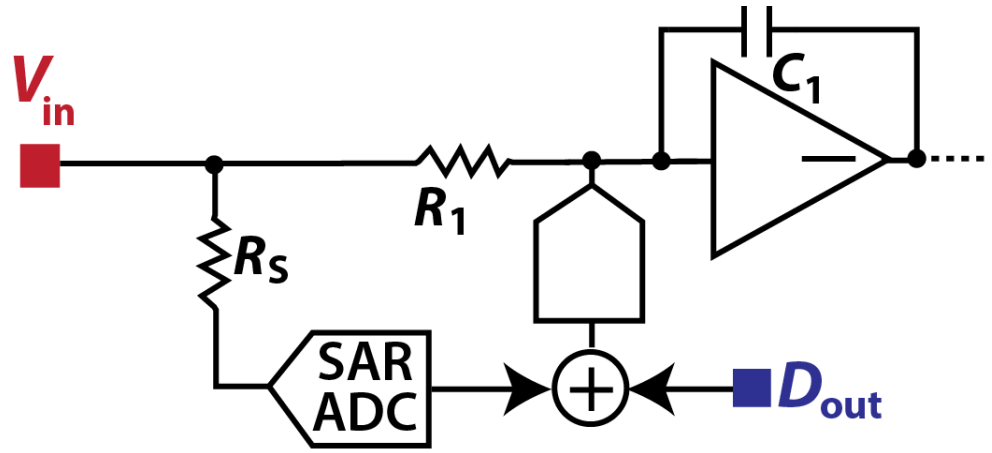
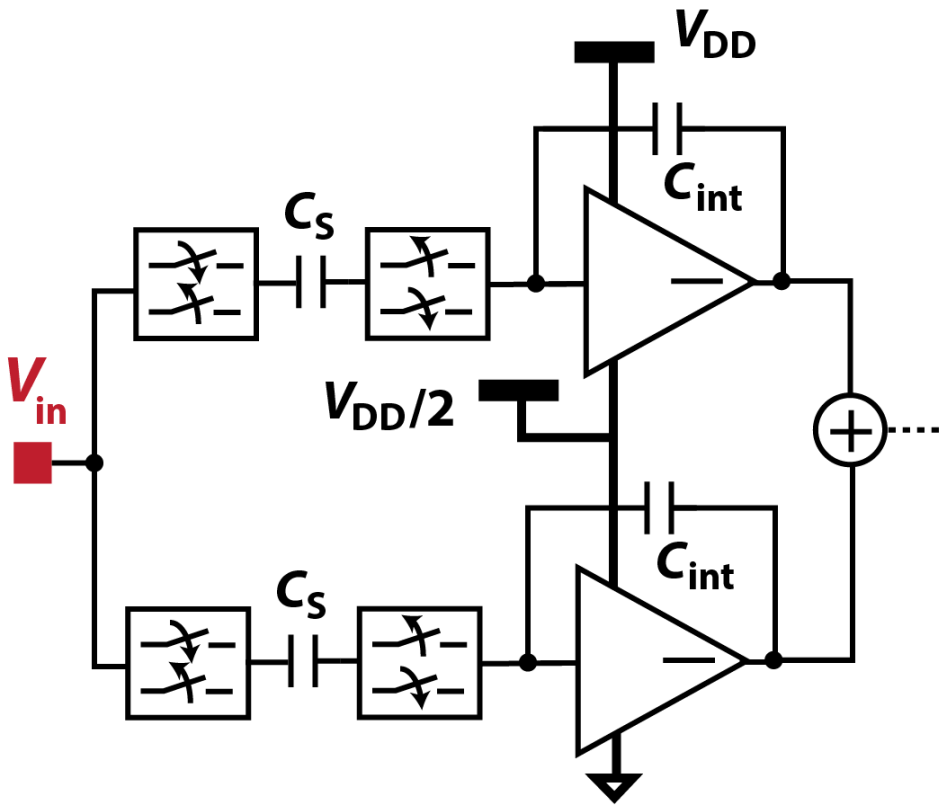
Zoom architecture [Gönen VLSI'19]:



- ✓ Coarse quantization by low power SAR

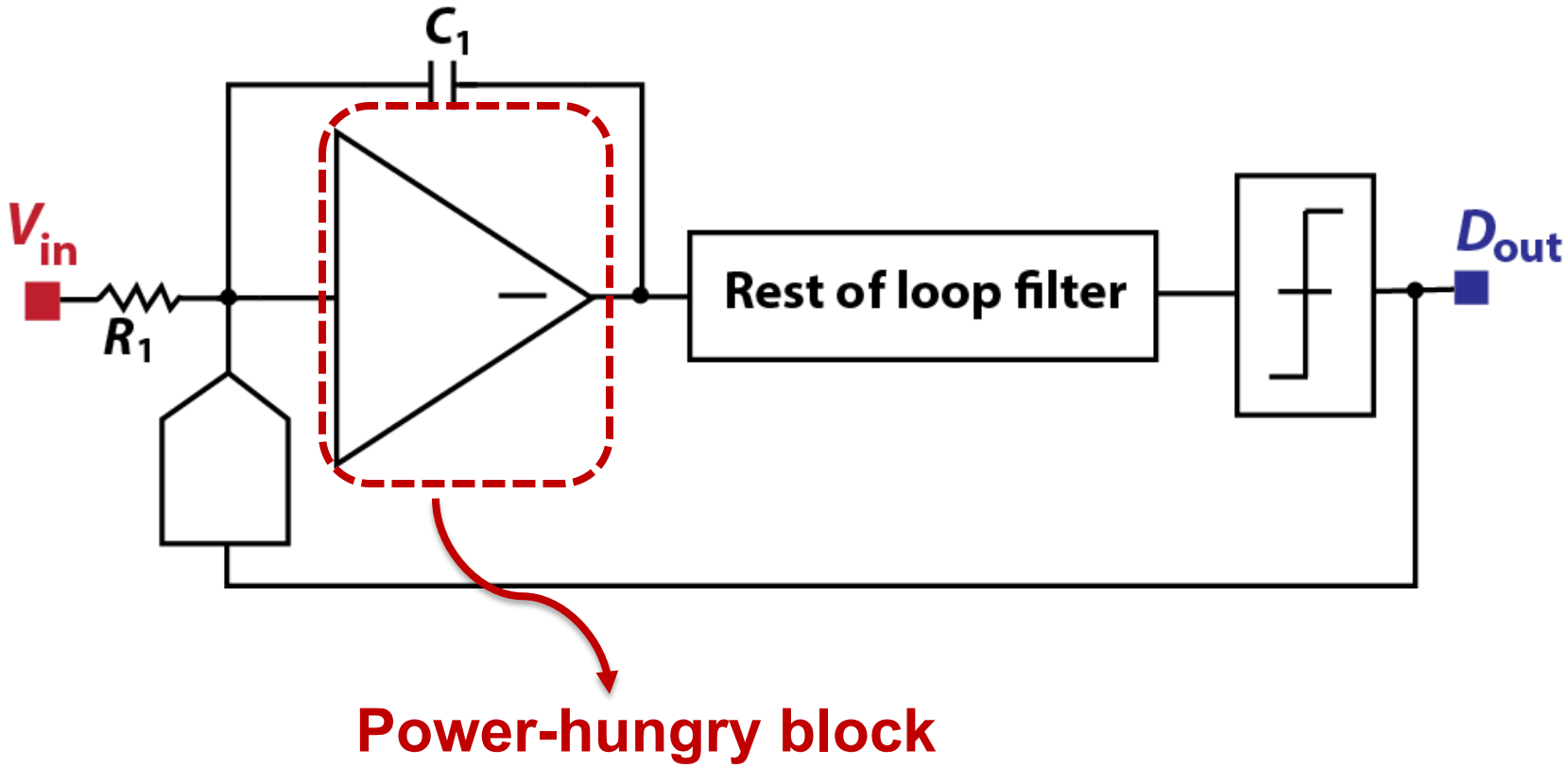
Prior Techniques in ΔΣMs

Split-steering stacked integrators [Steiner ISSCC'16]:



- ✓ Stacked SC-integrators, lower noise for same current
- ✗ Limits OTA implementations to single stage
- ✗ Needs high V_{DD} (5.4 V)
- ✗ Needs an extra $V_{DD}/2$ supply source
- ○ DC-coupled *RC*-integrators cannot be directly stacked

Proposed CTΔΣM with OTA-Stacking



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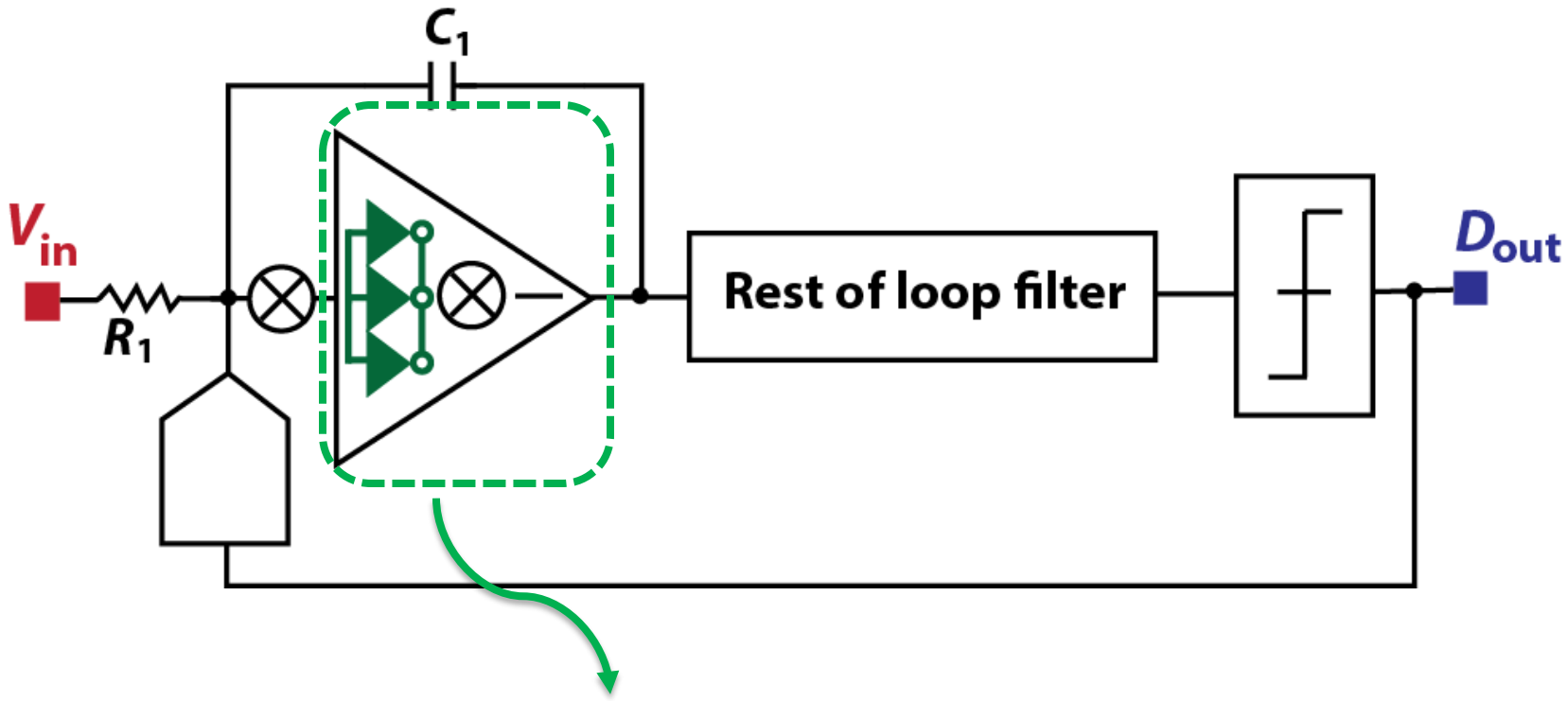


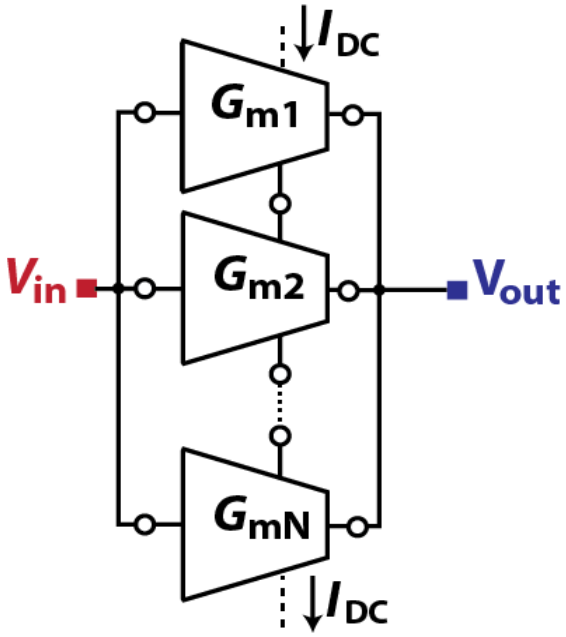
AC- Coupled Stacked-OTA

[Mondal ISCAS'17], [Mondal JSSC'20]

Noise efficiency of the input OTA improved by stacking

OTA-Stacking Concept

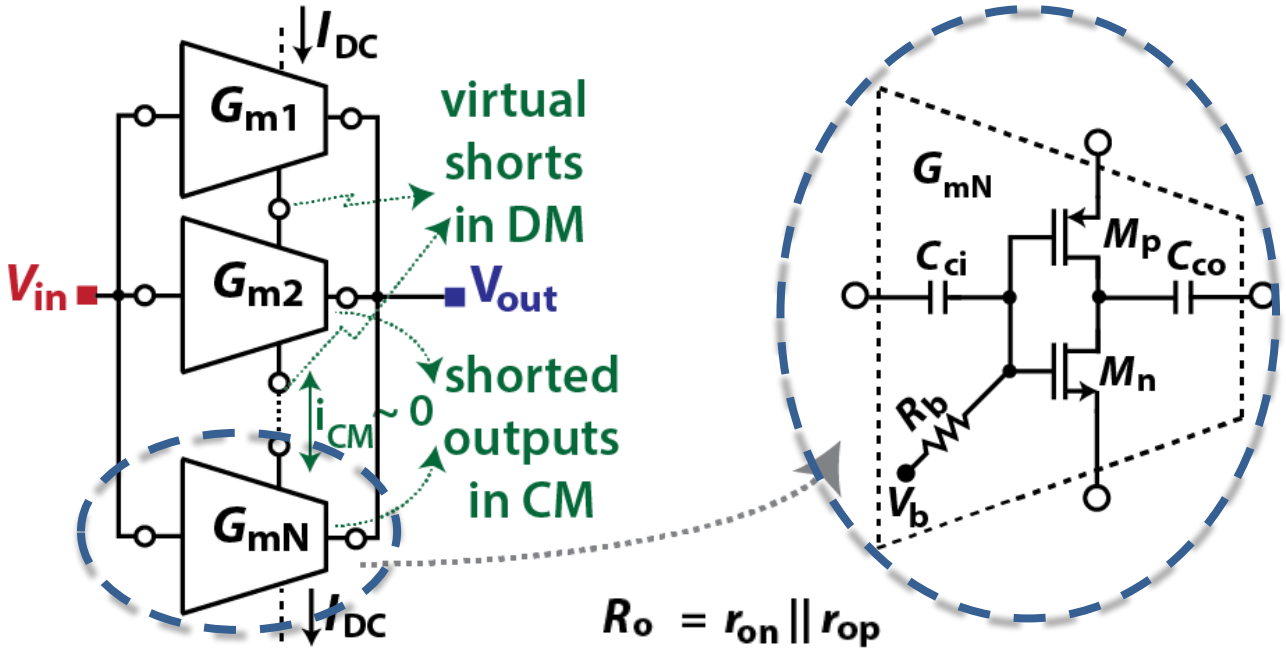
Single-ended Stacked OTA



OTA-Stacking Concept

Single-ended Stacked OTA

AC-coupled inverter-based transconductor

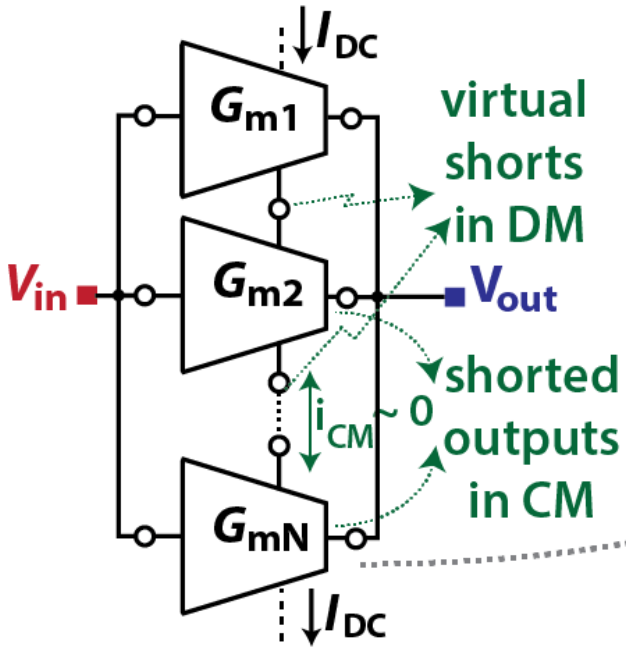


$$R_o = r_{on} \| r_{op}$$

$$G_{mo} = g_{mn} + g_{mp}$$

OTA-Stacking Concept

Single-ended Stacked OTA



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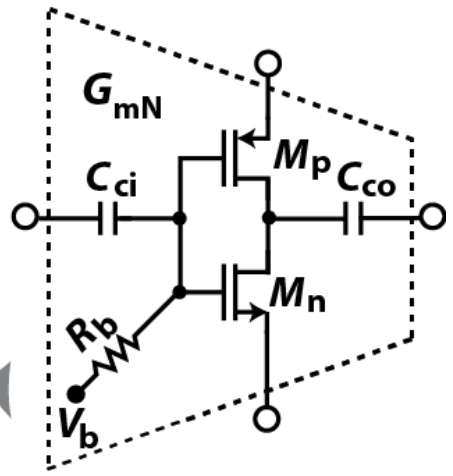
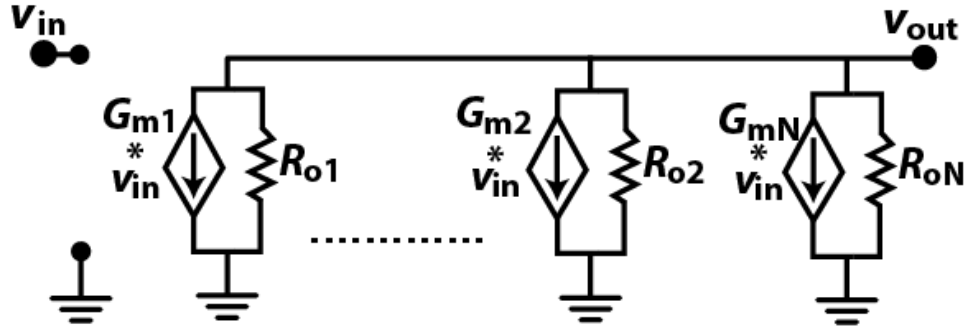


$G_{mo} = g_{mn} + g_{mp}$

Equivalent small-signal model



G_m boosting:

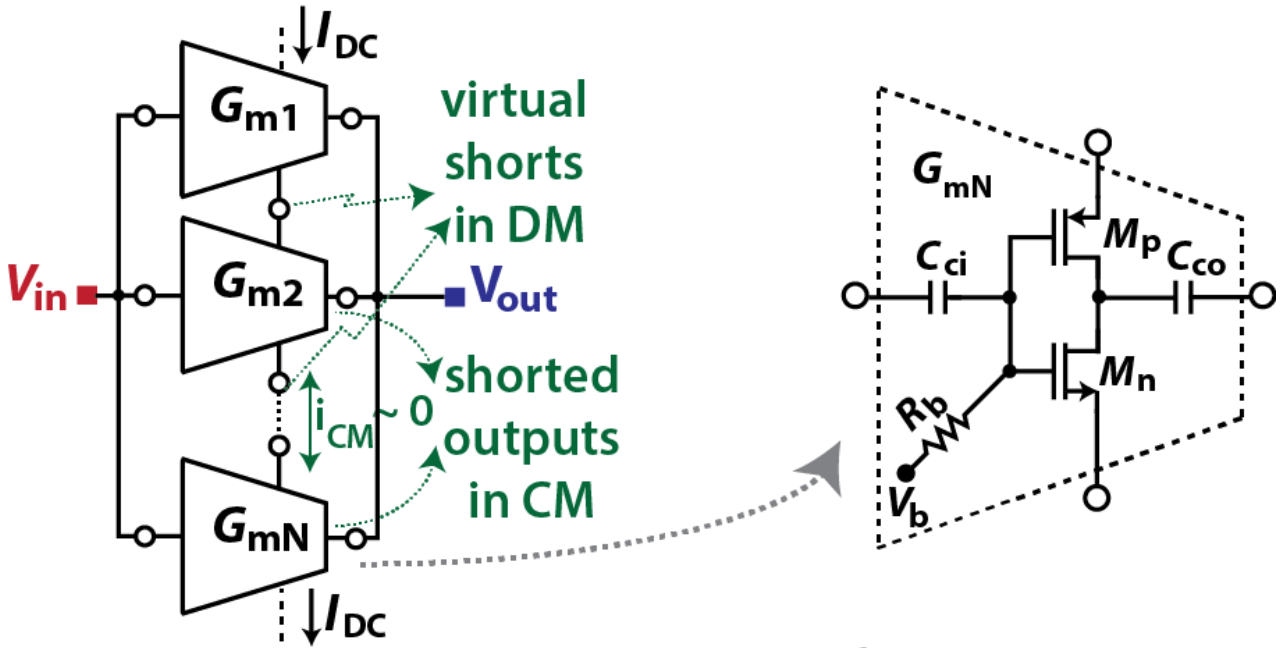
$$G_{m,stacked} = \boldsymbol{N} G_{mo}$$

$$R_{out,stacked} = R_o / \boldsymbol{N}$$

$$A_{v,stacked} = G_m R_{out} = G_{mo} R_o$$

OTA-Stacking Concept

Single-ended Stacked OTA



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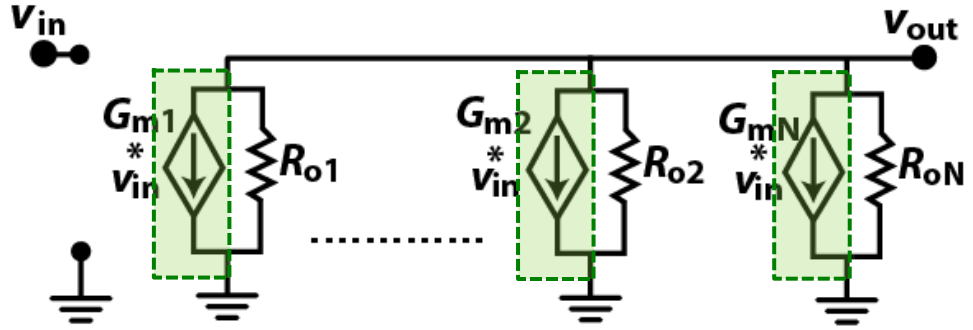


G_m boosting:

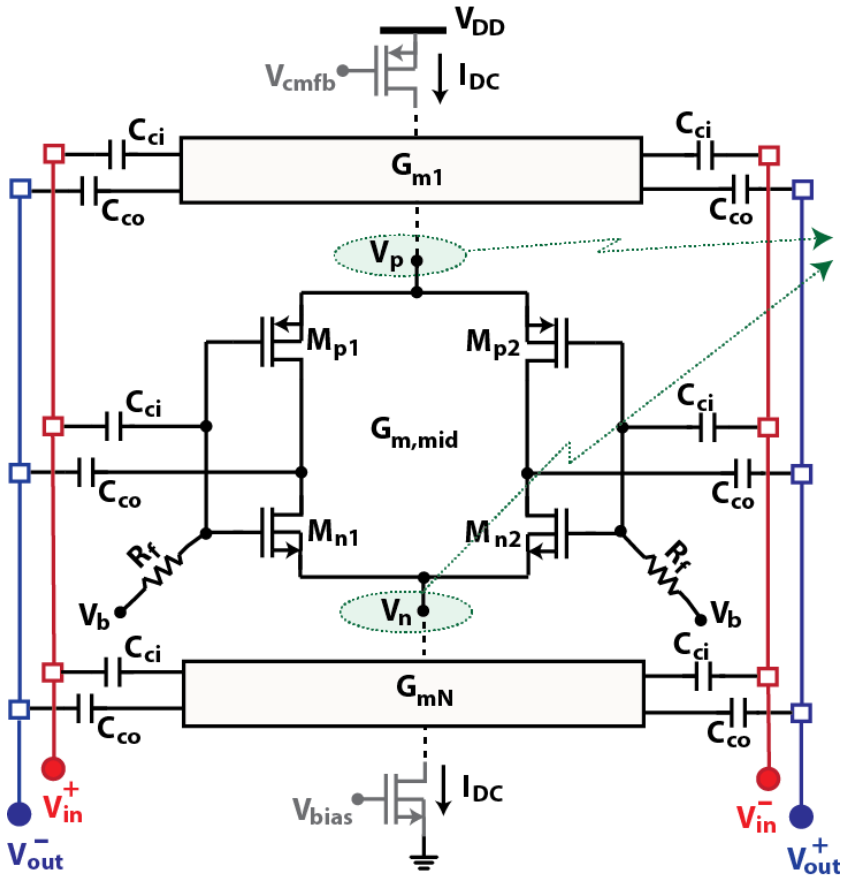
$$G_{m,stacked} = NG_{mo}$$

$$R_{out,stacked} = R_o/N$$

$$A_{v,stacked} = G_m R_{out} = G_{mo} R_o$$

Higher G_m for the same current!

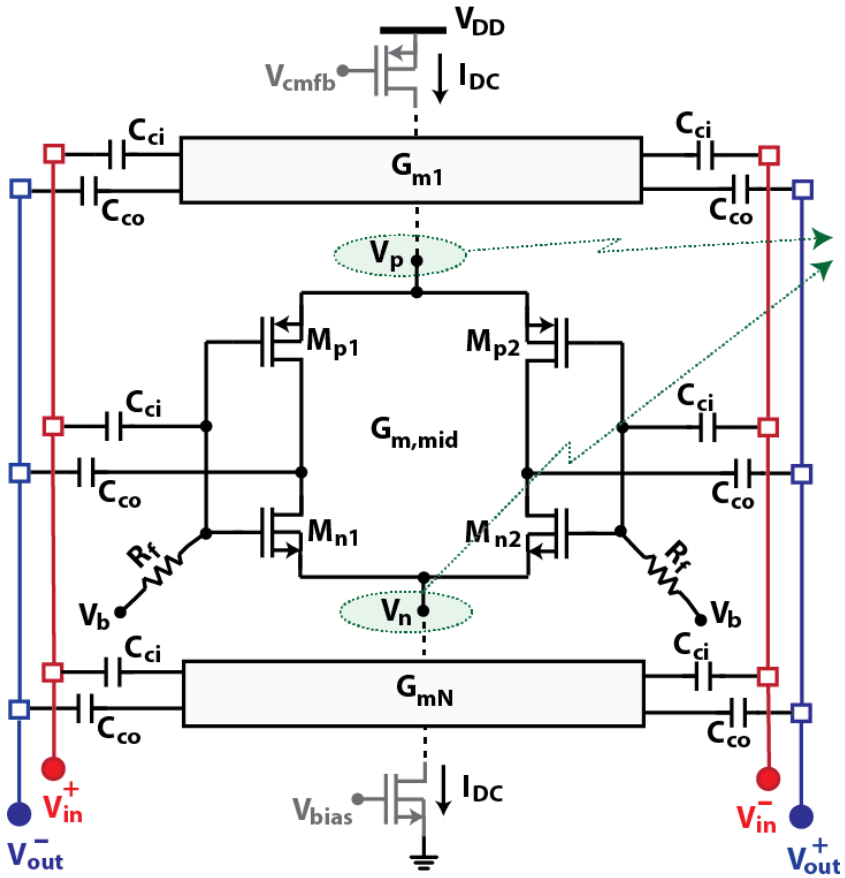
Stacked-OTA in Differential-mode



virtual shorts in differential-mode

Inherent decoupling in differential-mode

Stacked-OTA in Differential-mode



virtual shorts in differential-mode

G_m boosting: $G_{\mathrm{m}} = \boldsymbol{N} G_{\mathrm{mo}}$

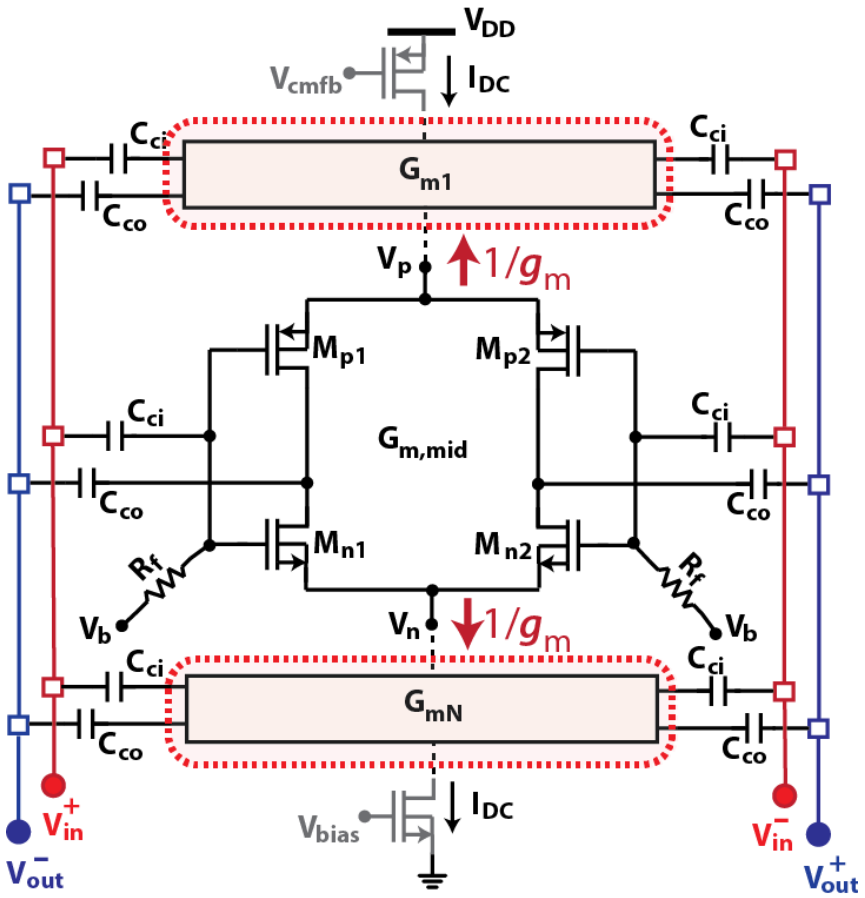
Input-referred thermal noise:

$$\overline{v_{\mathrm{ni,thermal}}^2} = \frac{4k_{\mathrm{B}}T\gamma}{\boldsymbol{N} G_{\mathrm{mo}}}$$

Inherent decoupling in differential-mode

Lower noise for the same current!

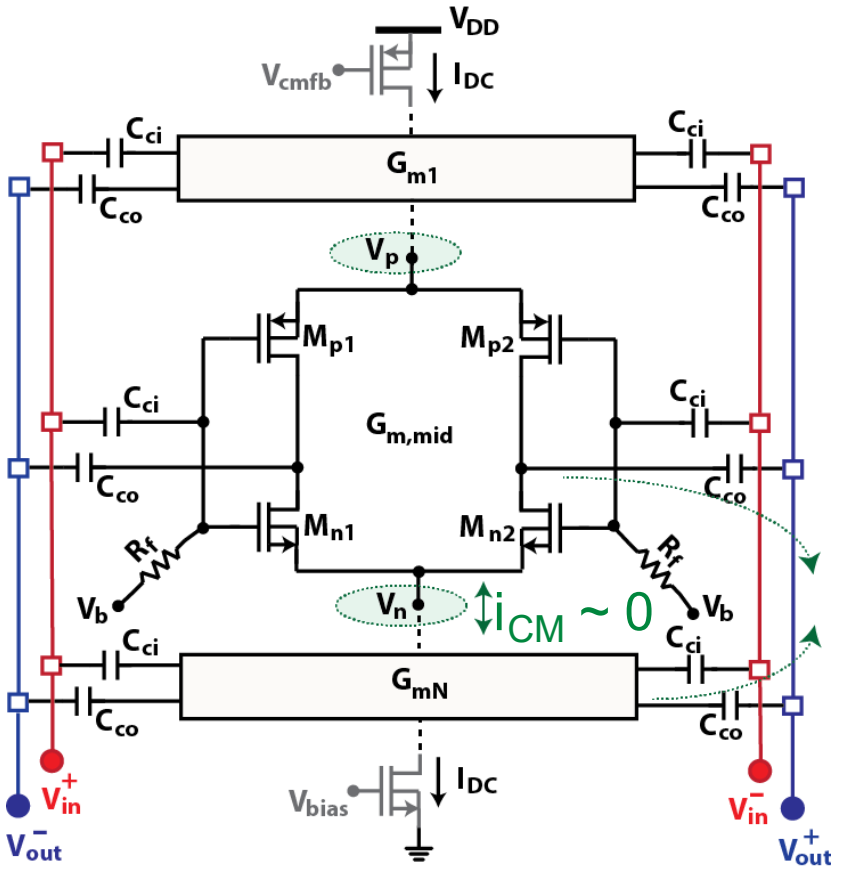
Stacked-OTA in Common-mode



Low impedance looking into the source nodes of other stacked stages

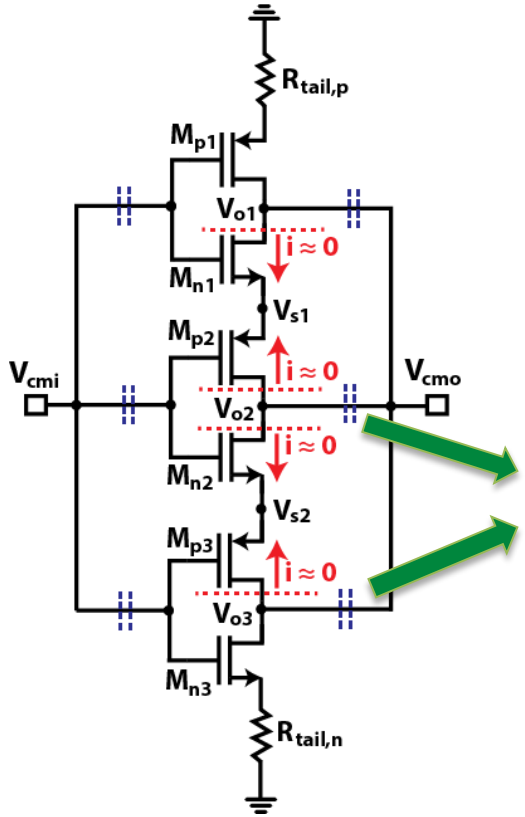
No common-mode rejection?

Stacked-OTA in Common-mode



shorted outputs in CM

CM half-circuit for a 3-stack OTA:

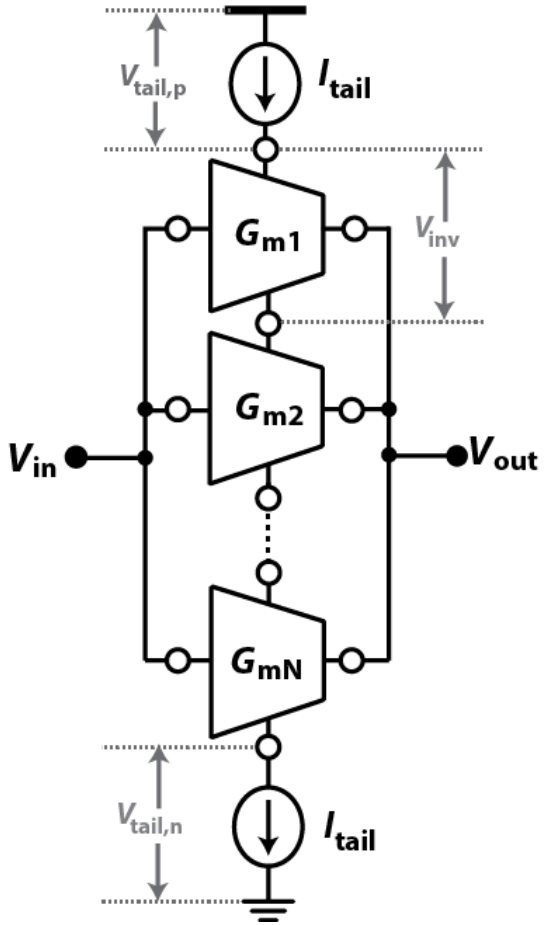


Shorted outputs: CM current into intermediate stacked stages is suppressed by **"self-feedback"**

[Mondal JSSC'20]

Output AC-coupling ensures good-common-mode rejection

Stacking Benefits: Amplifier PEF



$$V_{\mathrm{DD},min} = \boldsymbol{N} V_{\mathrm{INV}} + V_{\mathrm{tail}}$$

$$\boldsymbol{Noise} \downarrow \boldsymbol{N}$$

$$\boldsymbol{Power}_{\mathbf{min}} \uparrow \boldsymbol{N}$$

$$PEF_{min} \propto V_{\mathrm{INV}} + V_{\mathrm{tail}}/N$$

$PEF = NEF^2 V_{\mathrm{DD}}$

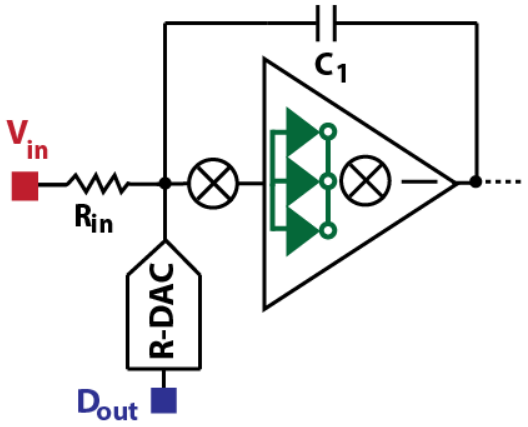
PEF: Amplifier noise *vs* power trade-off.

PEF Improvements $\propto 1 + 1/N$

- Tailed amplifier **[Mondal JSSC'20]:** PEF improves marginally
- Tailless amplifier **[Shen VLSI'19]:** PEF sees no improvement with stacking

Should we lower V_{DD} or keep stacking?

Stacking Benefits: ADC FoM



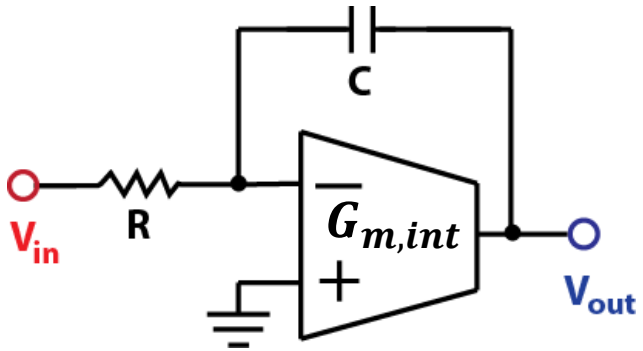
$$Noise = 8KTR_{\text{in,DAC}} + \frac{4KT\gamma}{g_{\text{m}}}$$

$$\cong 8KTR$$

$G_{\text{m}} = \alpha/R$ — G_{m} chosen → OTA noise is proportionately lower than the resistive noise by a consistent factor $2\gamma/\alpha$

"Assuming input G_{m} is the only power consuming block"

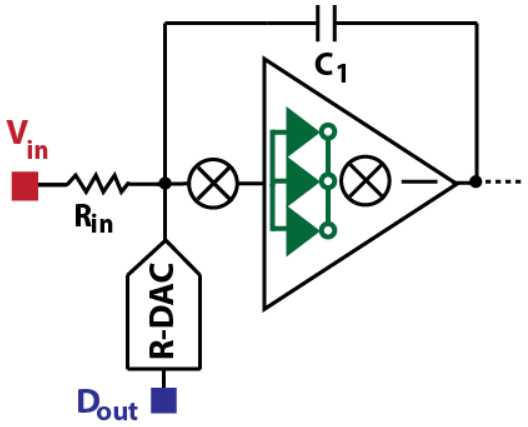
Maximizing R ($G_{\text{m,int}}R$ >> 1) → maximizes the closed-loop linearity



$$\frac{V_{\text{out}}}{V_{\text{in}}}(s) = -\left(\frac{G_{\text{m,int}}R}{1 + G_{\text{m,int}}R}\right)\frac{1}{sCR}$$

(G_{m}: input stage transconductance;
$G_{\text{m,int}}$: RC-integrator overall OTA's transconductance)

Stacking Benefits: ADC FoM



"Assuming input G_m is the only power consuming block"

$$Noise \cong 8KTR \qquad G_m = \alpha/R$$

$$FOM_S = 10\log\left(SNDR \ \frac{\text{BW}}{Power}\right) \cong 10\log\left(\frac{1}{4KT}\frac{V_{DD}}{4\alpha}\ \frac{G_m}{I_{DC}}\right)$$

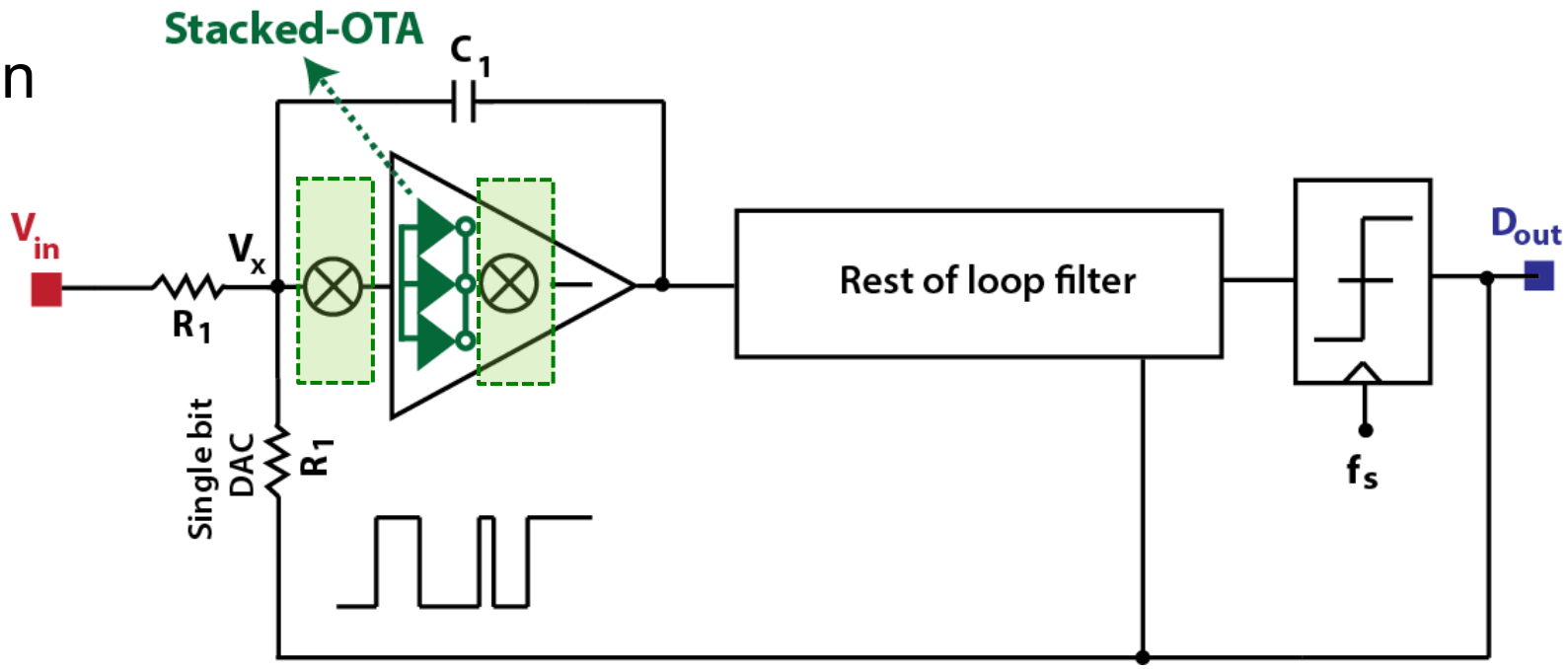
$$\cong -10\,log(4KT) + constant\ term + 10\log(V_{DD}) + 10\log(N)$$

- $-10\,log(4KT)$: -198 dB
- $constant\ term$: Dependent on device and design parameters
- $10\log(V_{DD}) + 10\log(N)$: Benefit of stacking

Direct Improvements in ADC FoM with both $\uparrow V_{DD}$ and $\uparrow N$

CTΔΣM with Stacking: Challenges

- ✘ AC-coupling blocks DC; integrator needs high DC gain
- ➔ Use chopping



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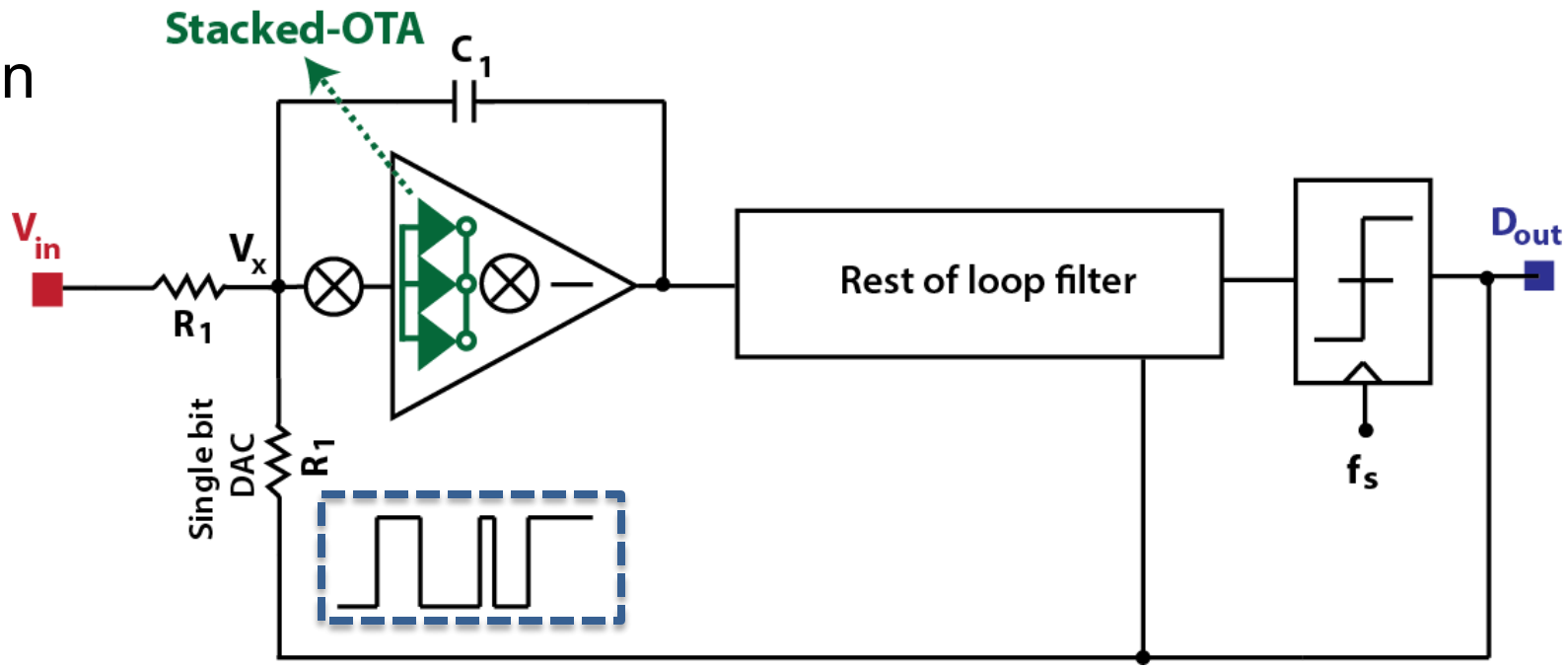
- ✘ Step response is poor with large coupling capacitors



CTΔΣM with Stacking: Challenges

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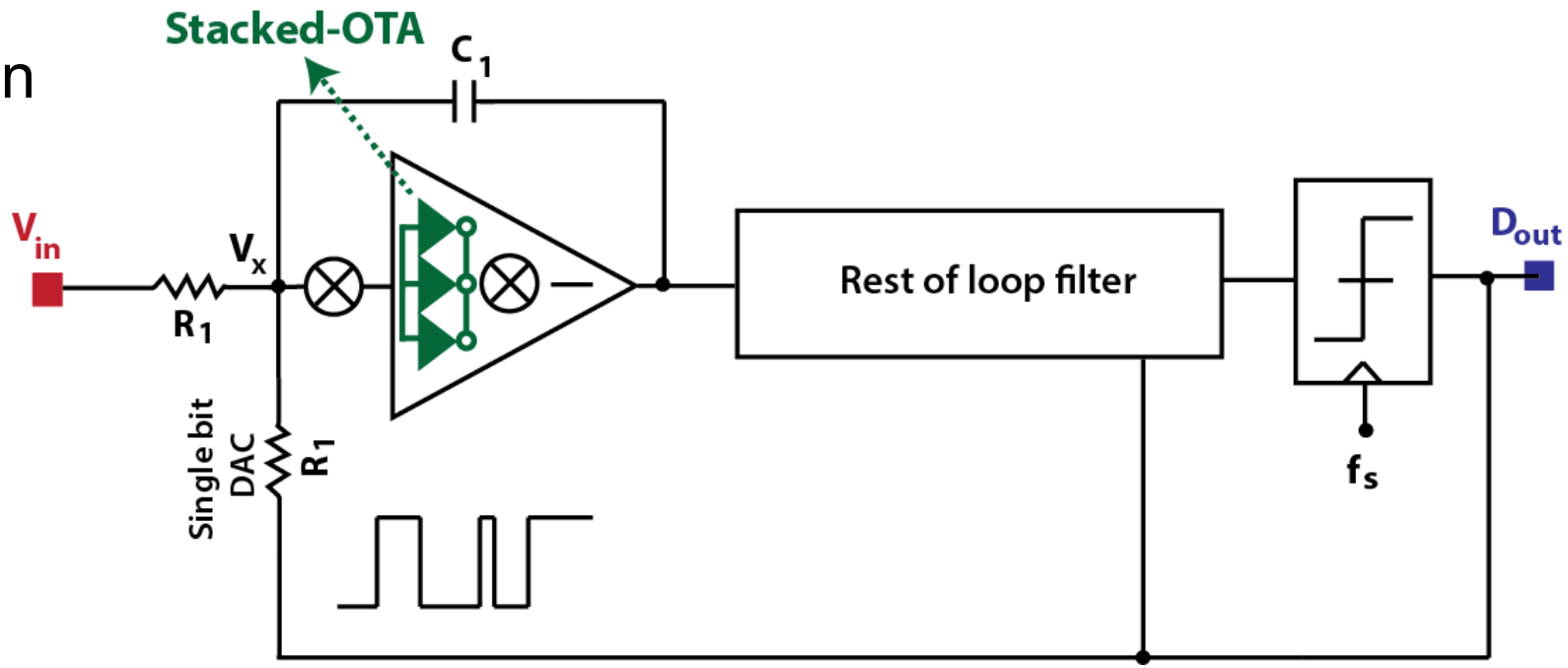
- ✘ Unwanted notches at multiples of f_{chop}



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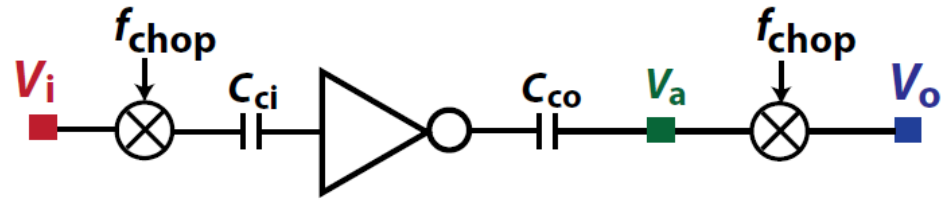
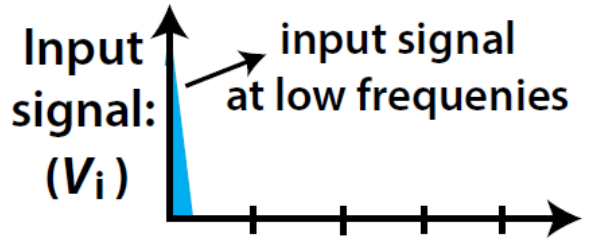
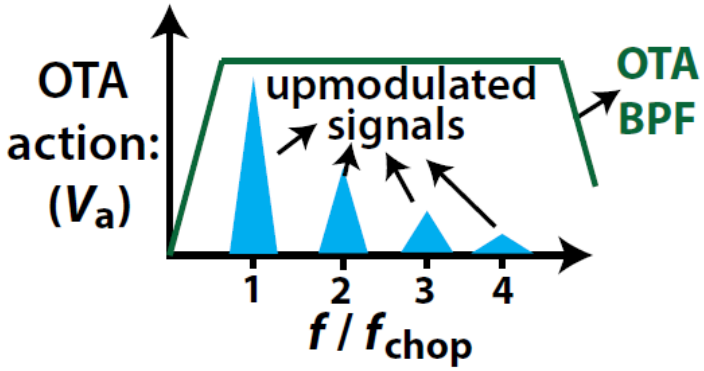
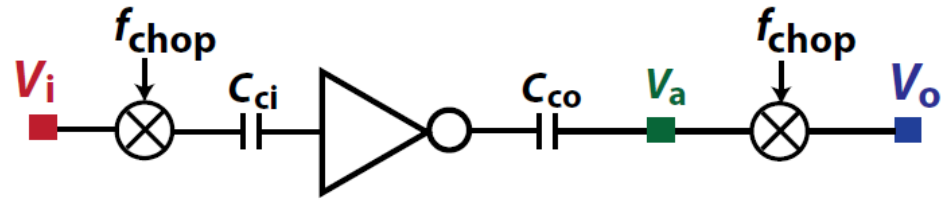


Signal response of AC-coupled OTA with chopped inputs:





CTΔΣM with Stacking: Challenges



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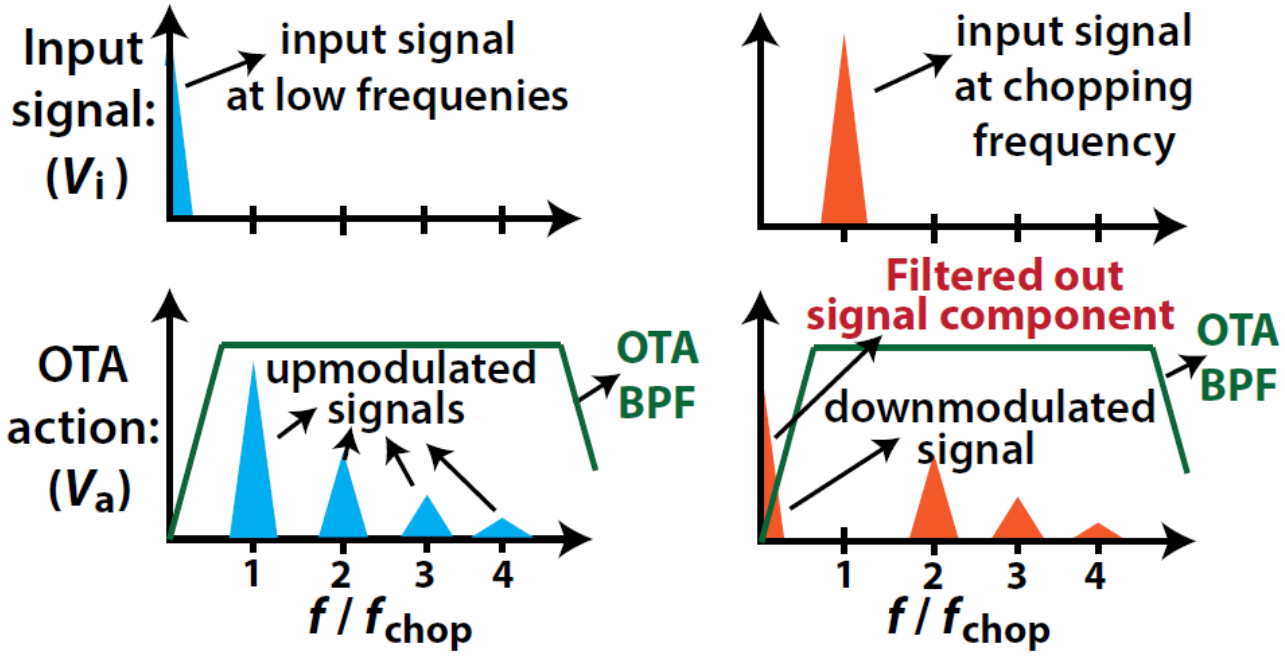

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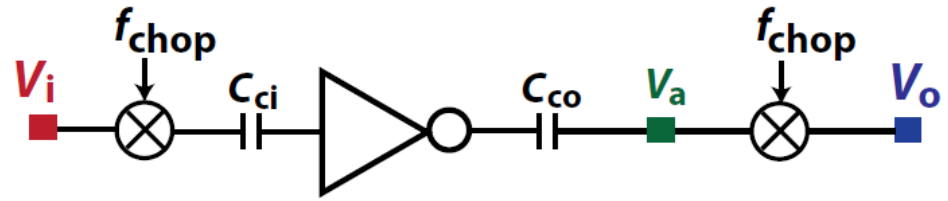

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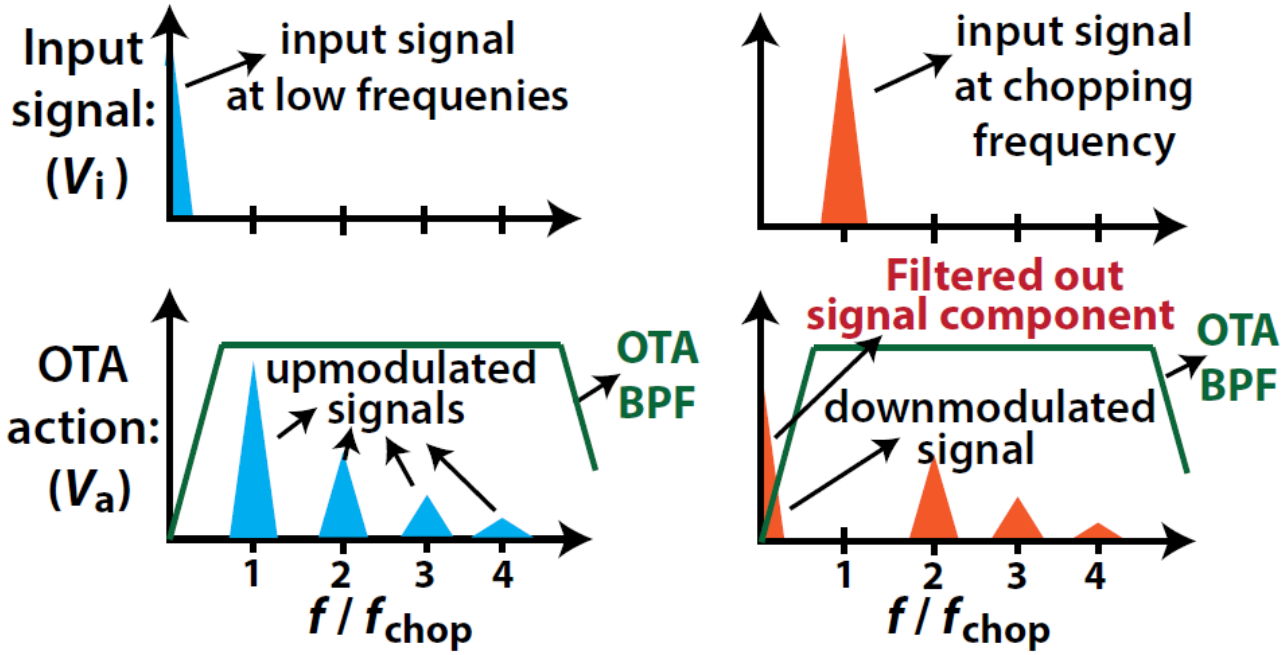
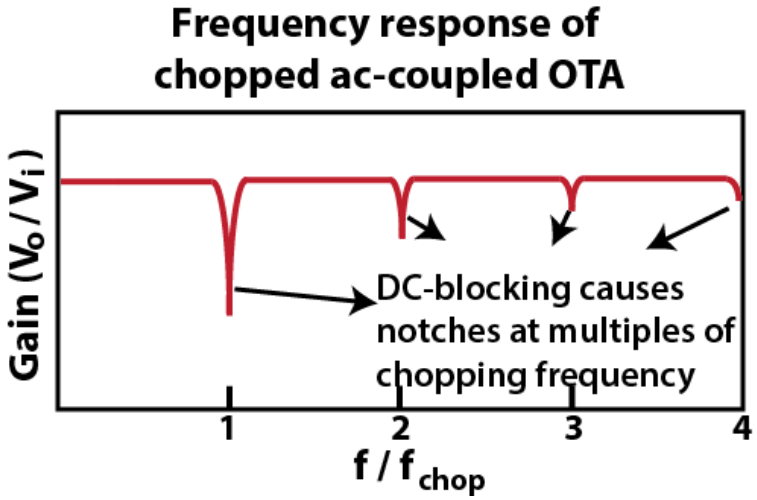
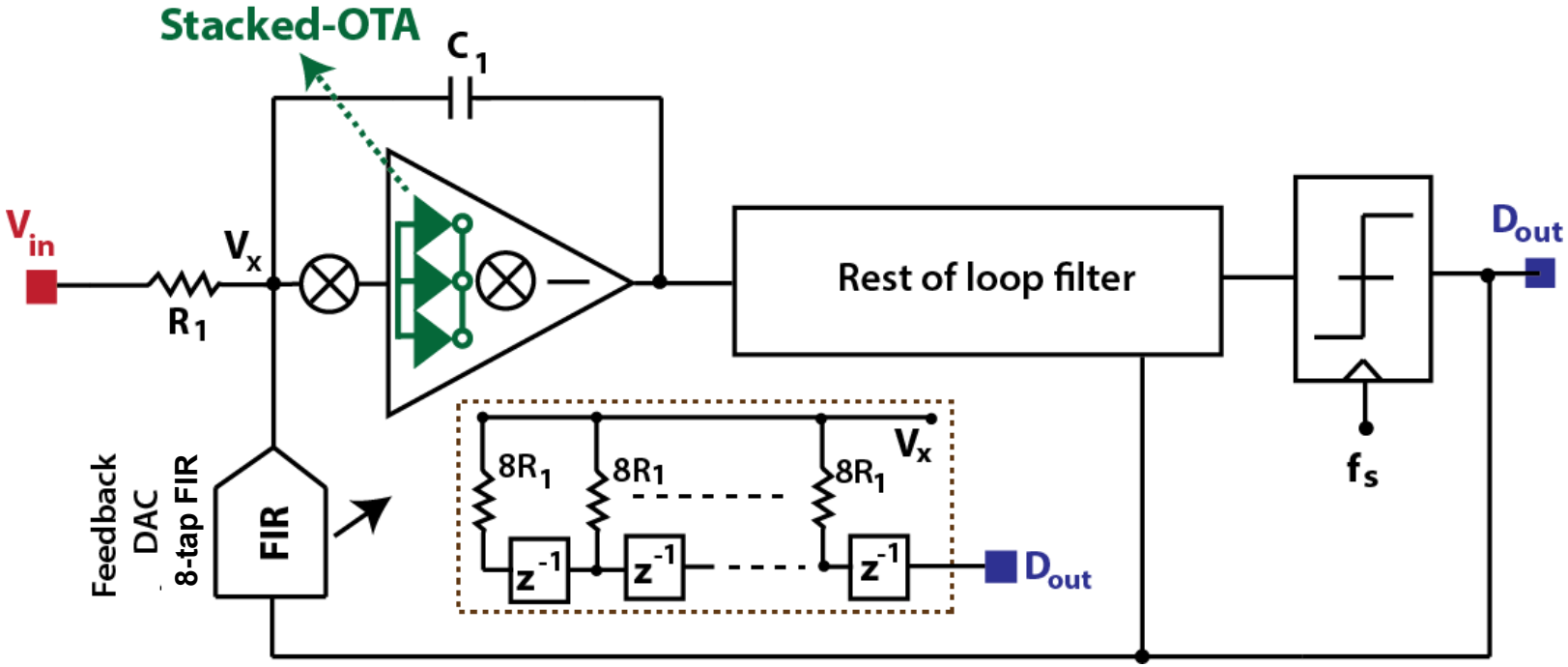




Key challenge: unwanted notches due to ac-coupled OTA

Proposed CTΔΣM with Stacking

FIR Feedback in CTDSM



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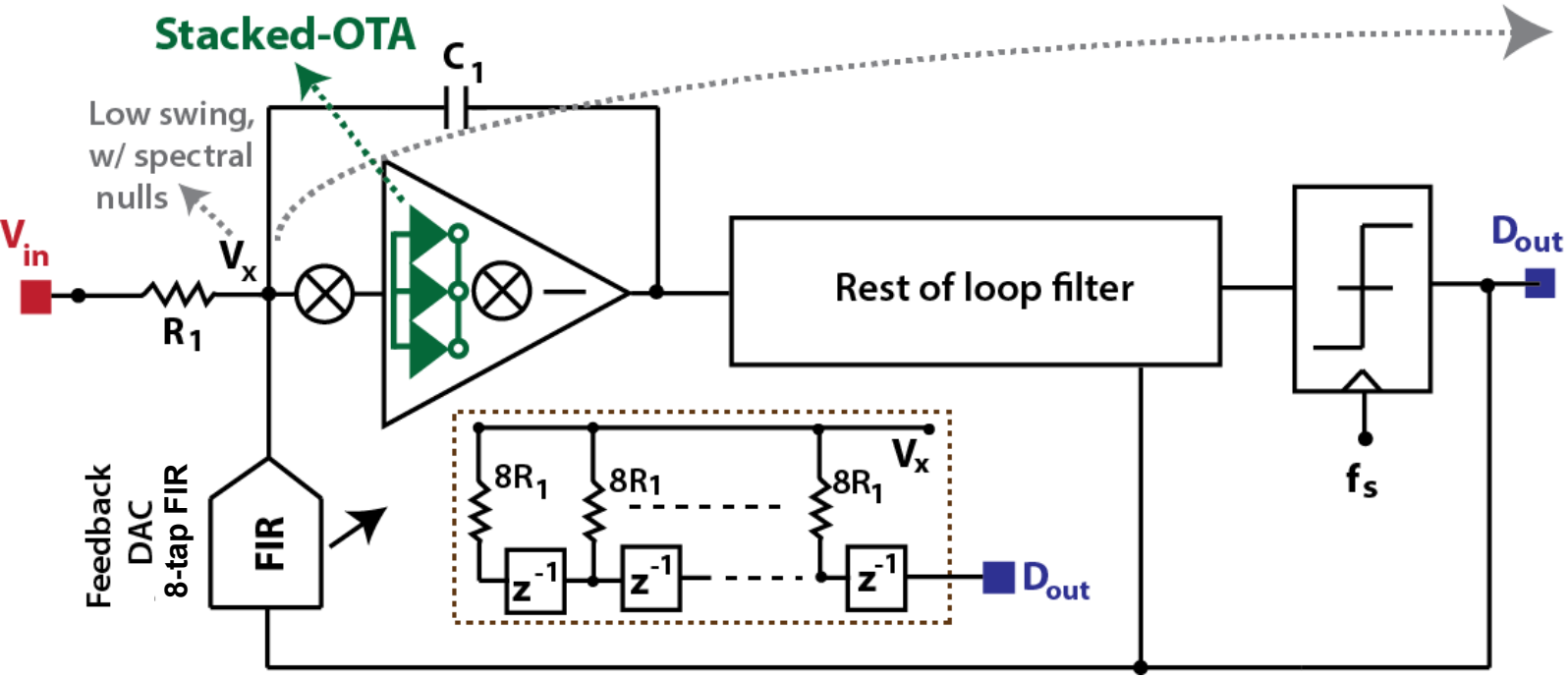

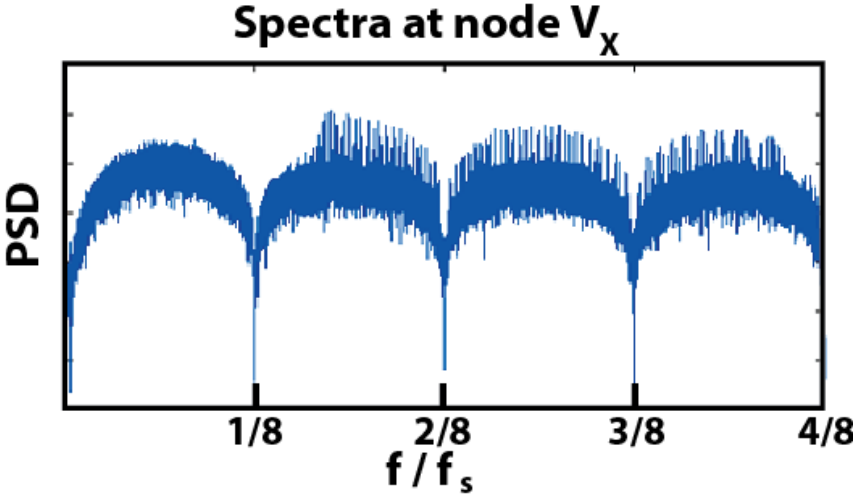

Prior work [Billa ISSCC'16]:

→ $f_{\text{chop}} = f_s/2N_{\text{FIR}}$ to mitigate chopping artifacts (N_{FIR}: # filter taps)

FIR DAC feedback with low swing and spectral nulls

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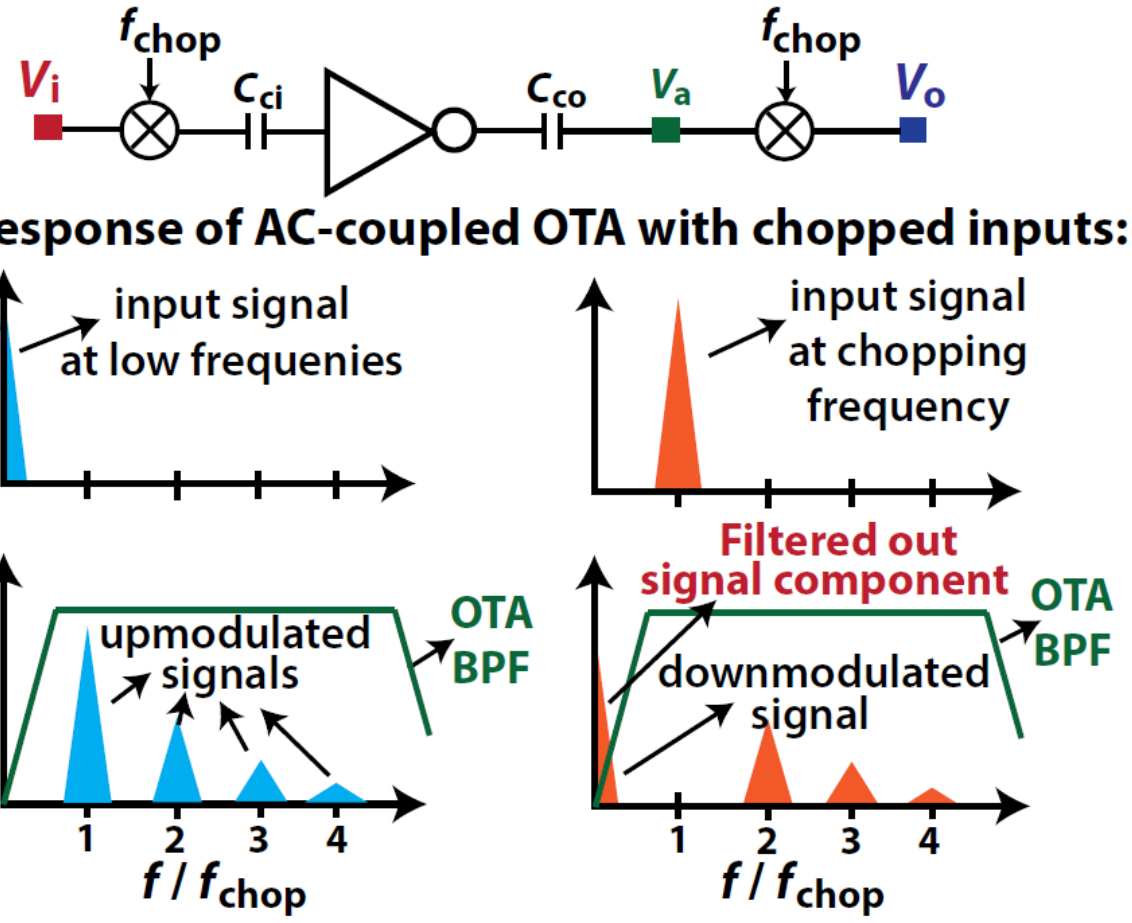
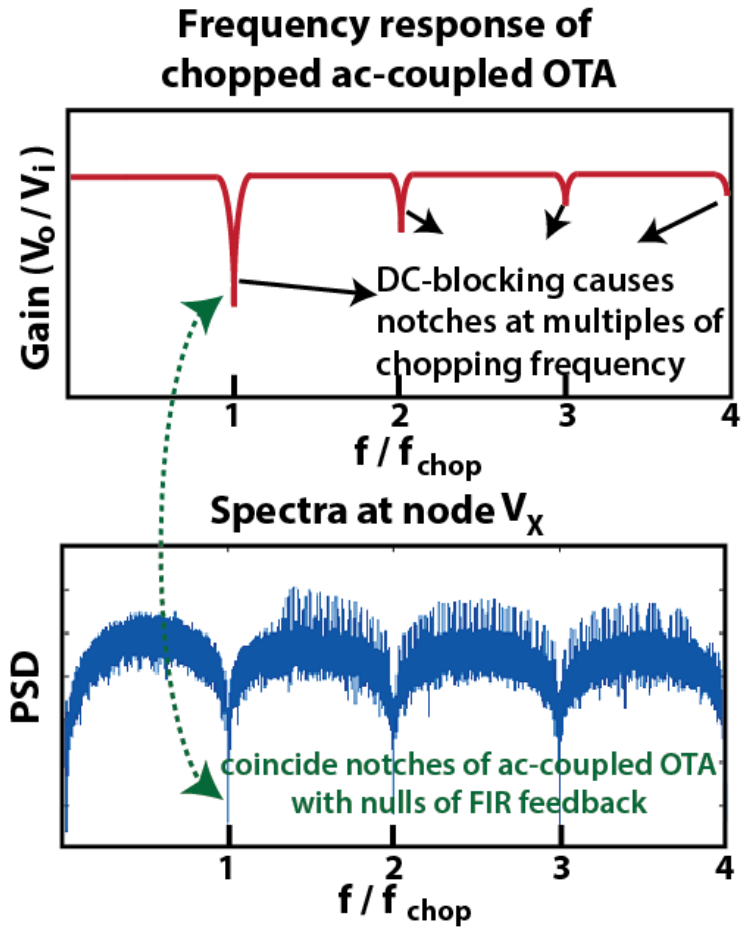




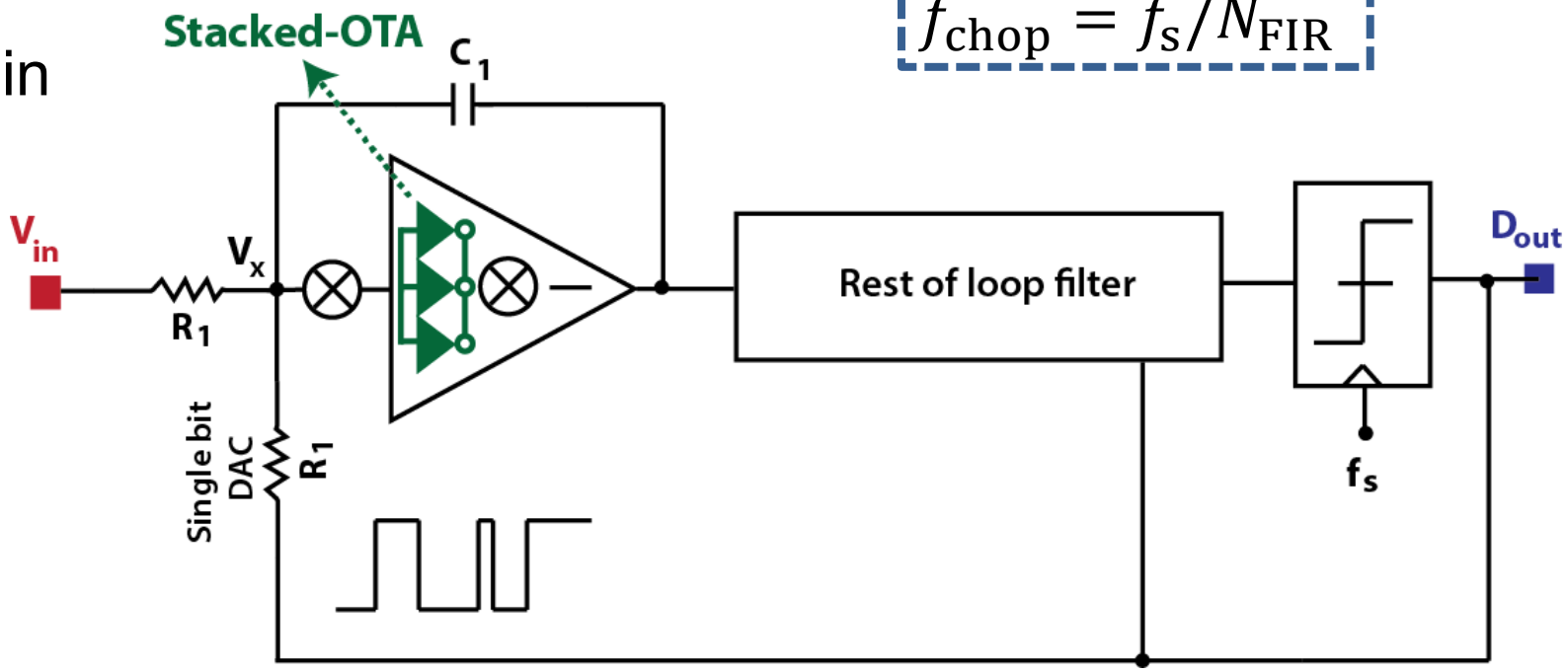
FIR DACs with $f_{chop} = f_s / N_{FIR}$ mitigates the unwanted notches issue

CTΔΣM with Stacking: Challenges

- ✘ AC-coupling blocks DC; integrator needs high DC gain
- ➔ Use chopping

- ✘ Step response is poor with large coupling capacitors
- ➔ Use FIR DACs
- ✘ Unwanted notches at multiples of f_{chop}
- ➔ Use FIR DACs

$$f_{\text{chop}} = f_s / N_{\text{FIR}}$$

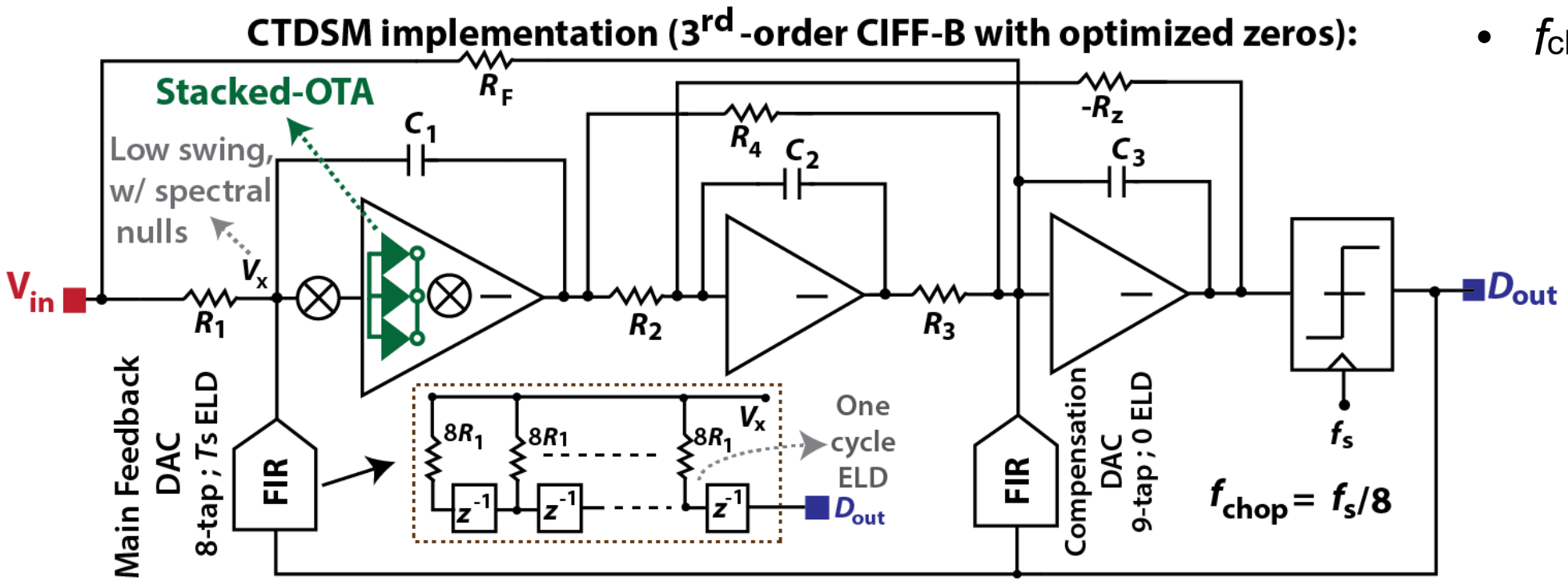


Use FIR DAC feedback with low swing and spectral nulls

CTΔΣM Architectural Implementation

3rd-order CIFF-B with optimized zeros (cascade of integrators feedforward and feedback)

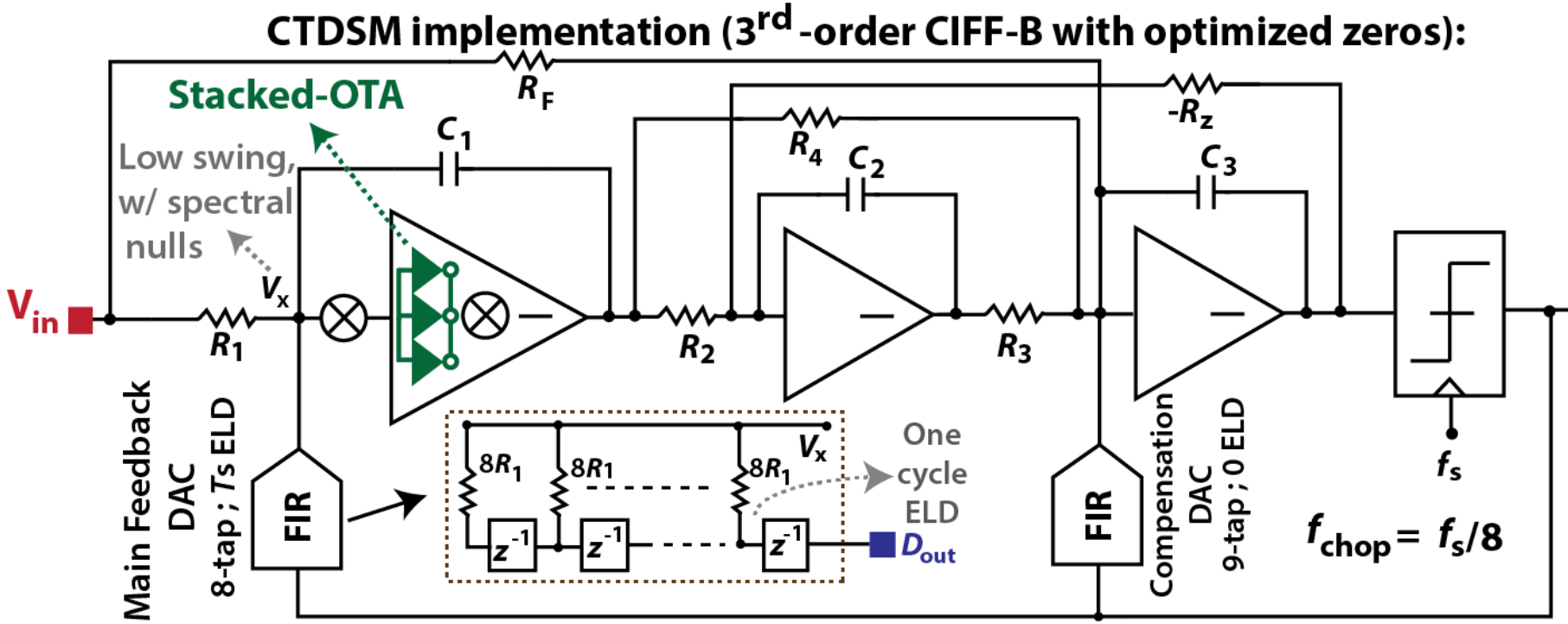
- f_s = 7.2 MHz
- *OSR* = 150
- f_{chop} = 900 kHz



3rd-order active-RC CTDSM with FIR DAC

CTΔΣM Architectural Implementation

3rd-order CIFF-B with optimized zeros (cascade of integrators feedforward and feedback)



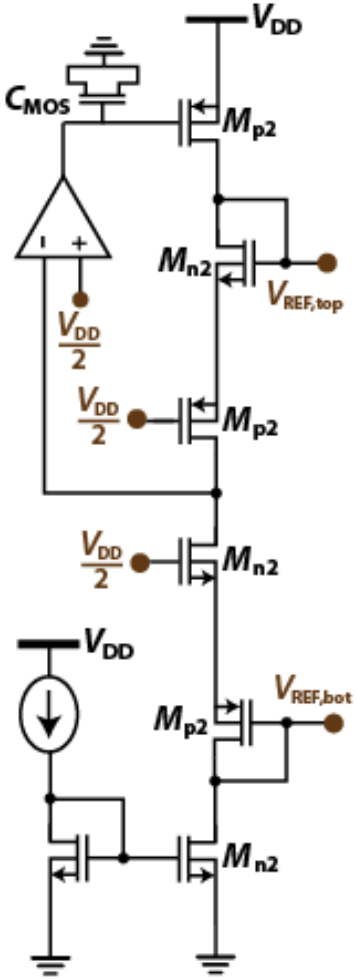
- f_s = 7.2 MHz
- *OSR* = 150
- f_{chop} = 900 kHz

- Full clock cycle ELD at main DAC
- Single compensation DAC restores NTF with FIR feedback and compensates for main DAC ELD

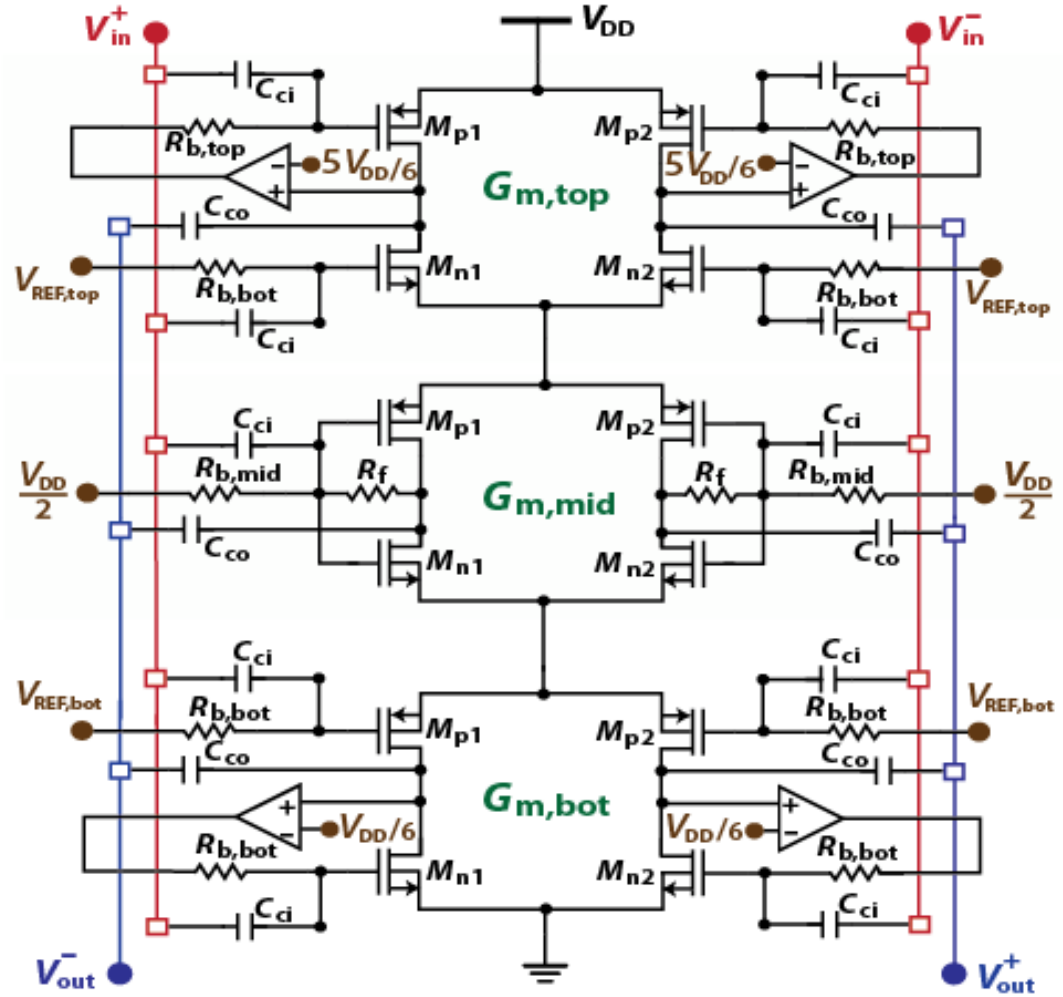
No extra fast path DAC or summing network is needed

Tail-less Stacked-OTA

Replica biasing network:

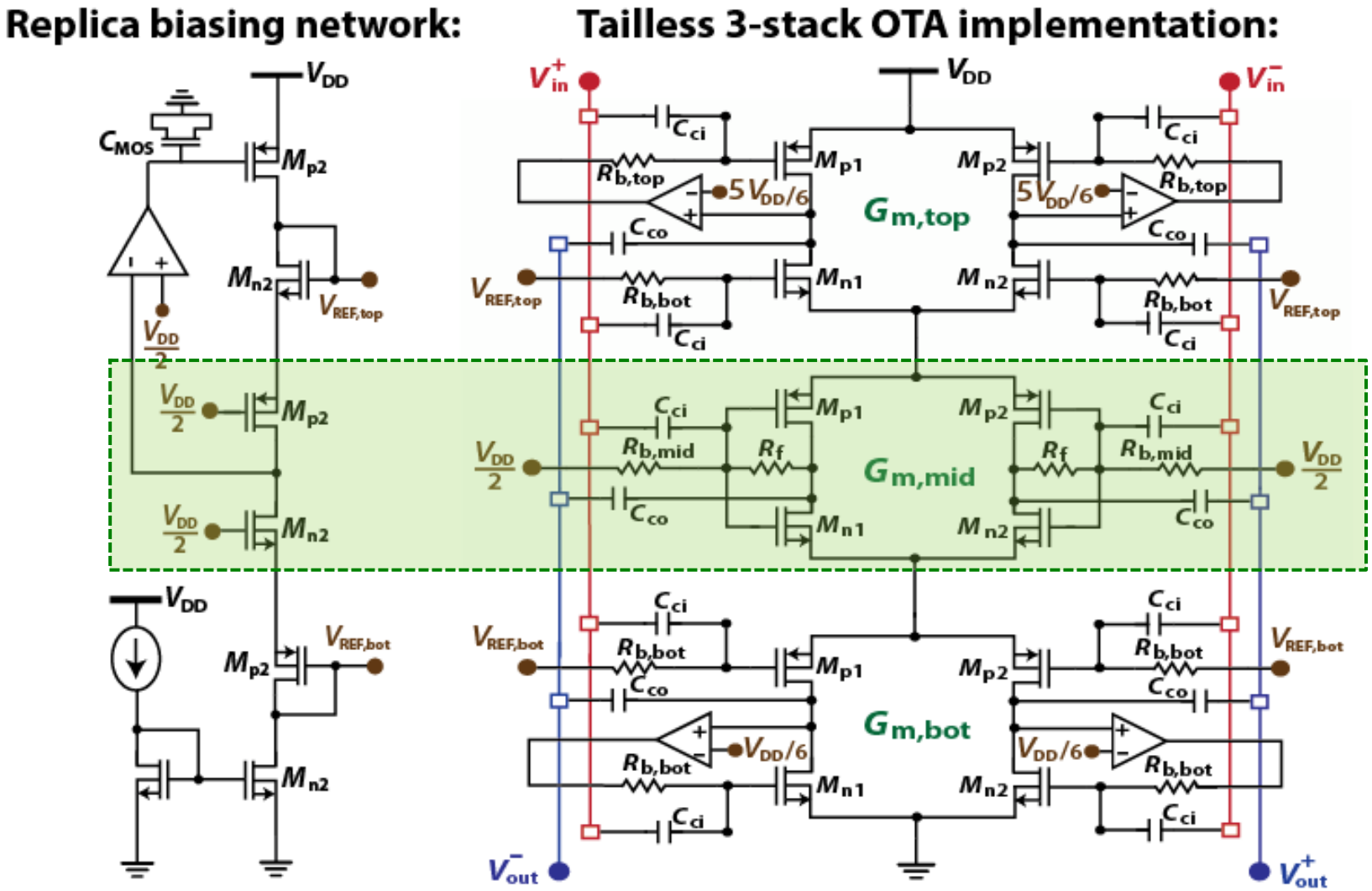


Tailless 3-stack OTA implementation:



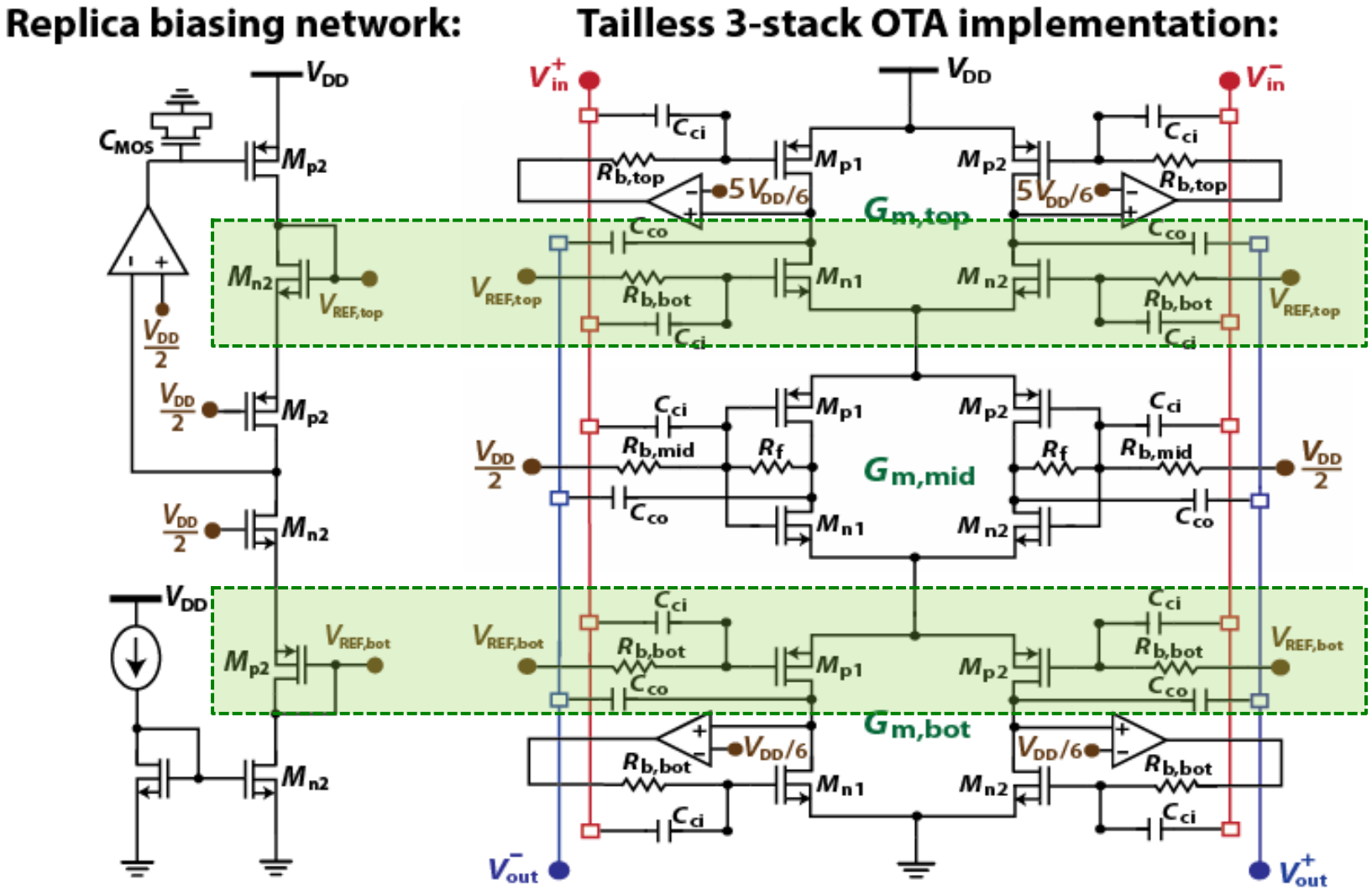
Tail-less operation
[Shen VLSI'19]

Tail-less Stacked-OTA



- ✓ Central inverter is self-biased

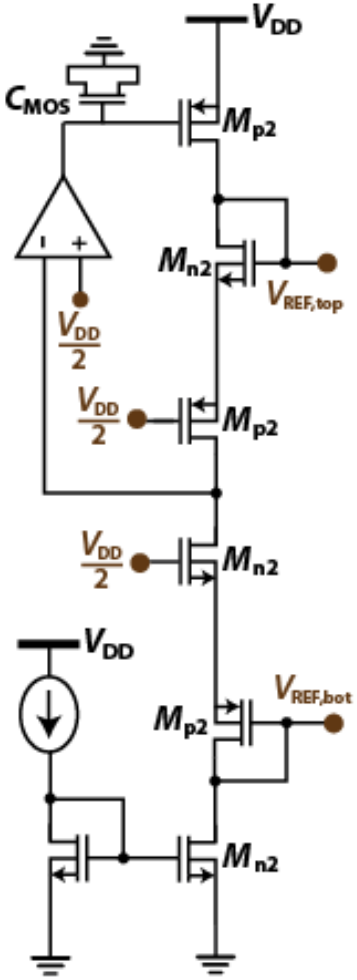
Tail-less Stacked-OTA



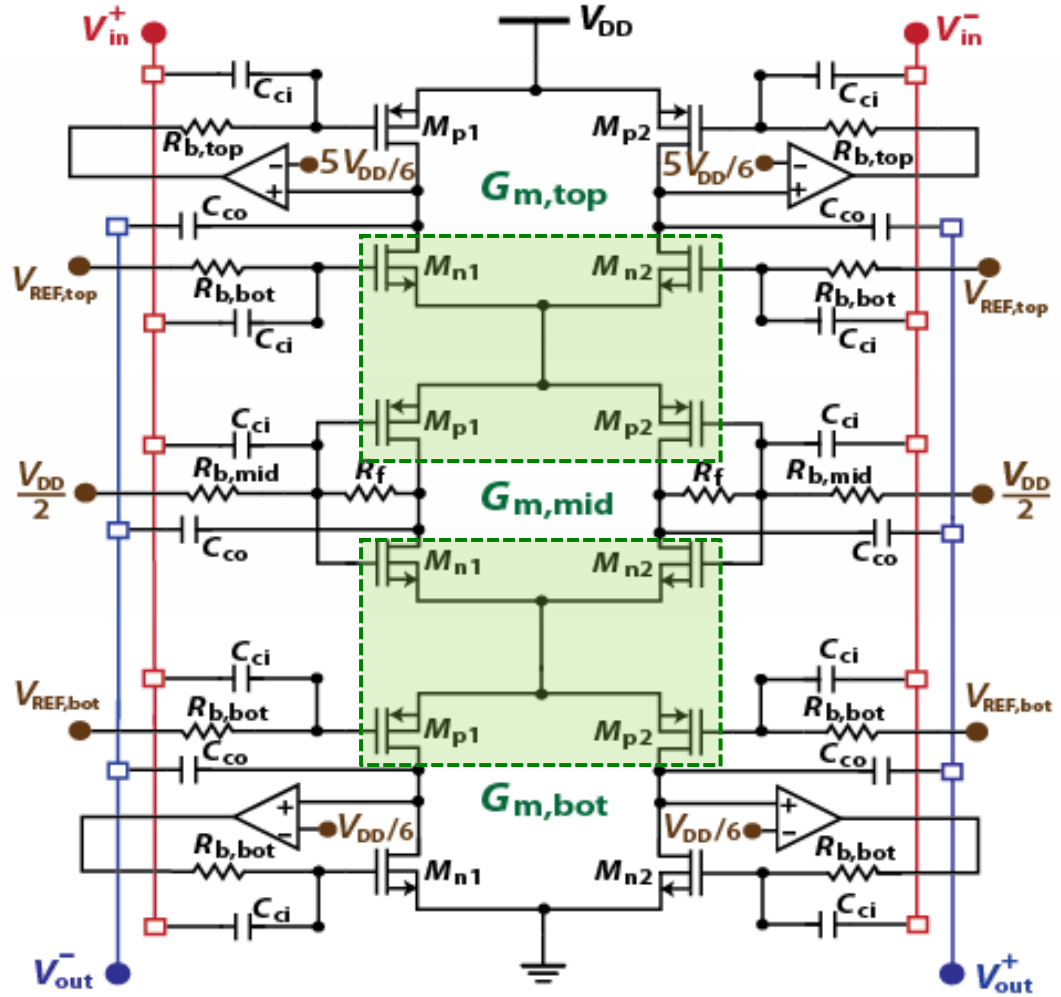
- ✓ Central inverter is self-biased
- ✓ Replica network biases intermediate transistors and sets the current.

Tail-less Stacked-OTA

Replica biasing network:



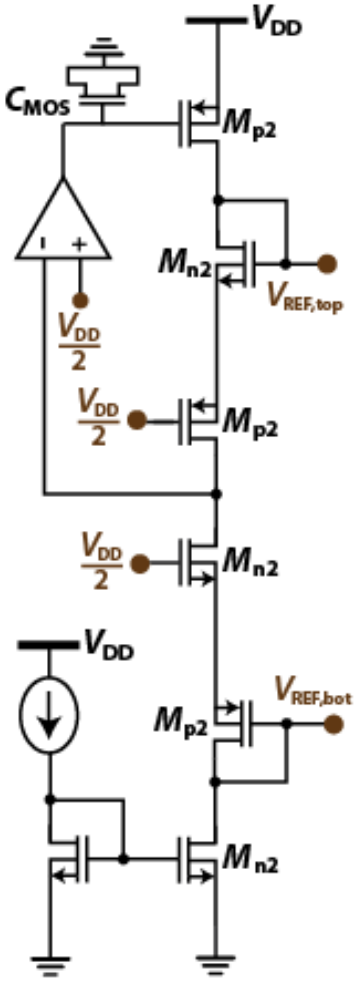
Tailless 3-stack OTA implementation:



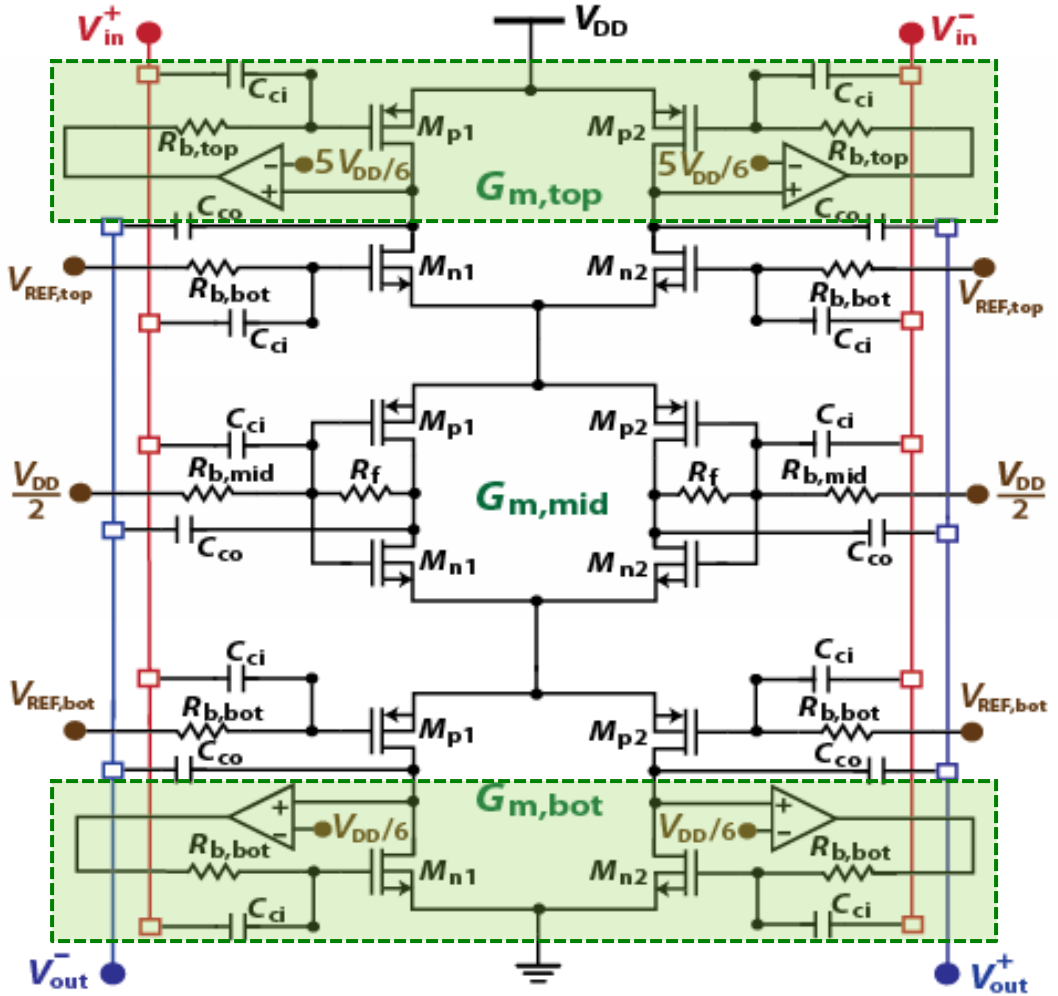
- ✓ Central inverter is self-biased
- ✓ Replica network biases intermediate transistors and sets the current.
- ✓ Good CM rejection for intermediate diff-pairs from ‘self-feedback’.

Tail-less Stacked-OTA

Replica biasing network:



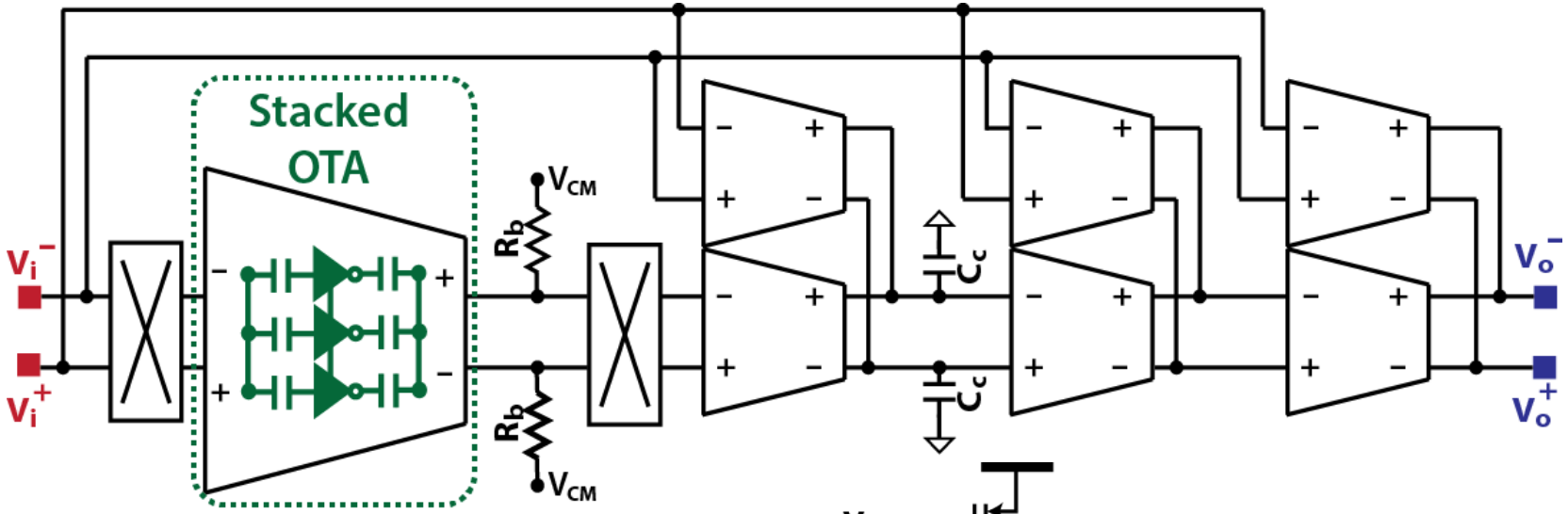
Tailless 3-stack OTA implementation:



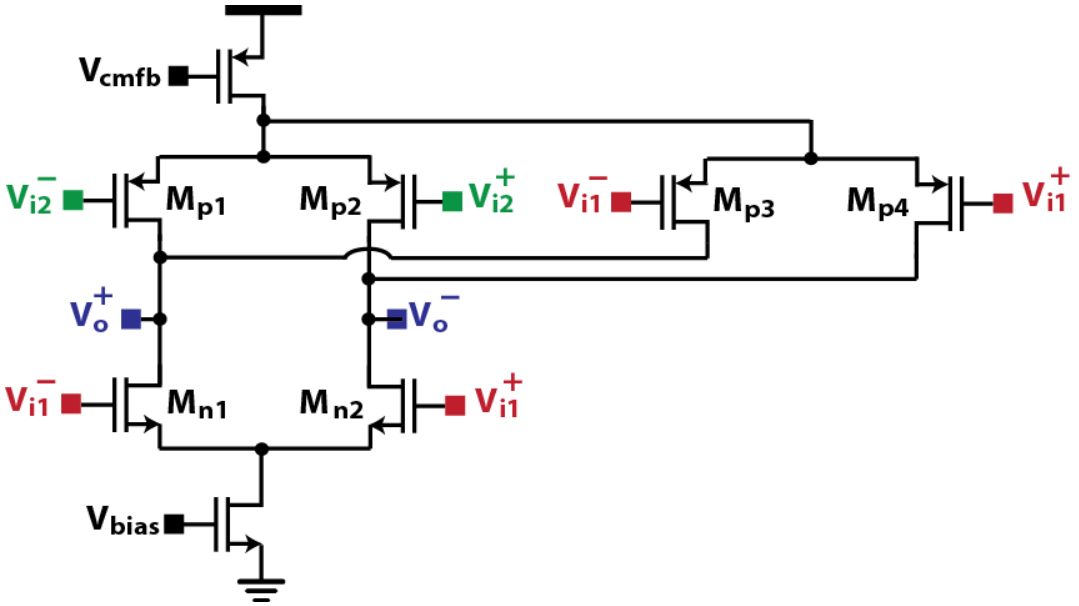
- ✓ Central inverter is self-biased
- ✓ Replica network biases intermediate transistors and sets the current.
- ✓ Good CM rejection for intermediate diff-pairs from ‘self-feedback’.
- ✓ Individual CM rejection loops for top and bottom diff.-pairs

First Integrator Implementation

First integrator opamp:
4-stage feedforward compensated

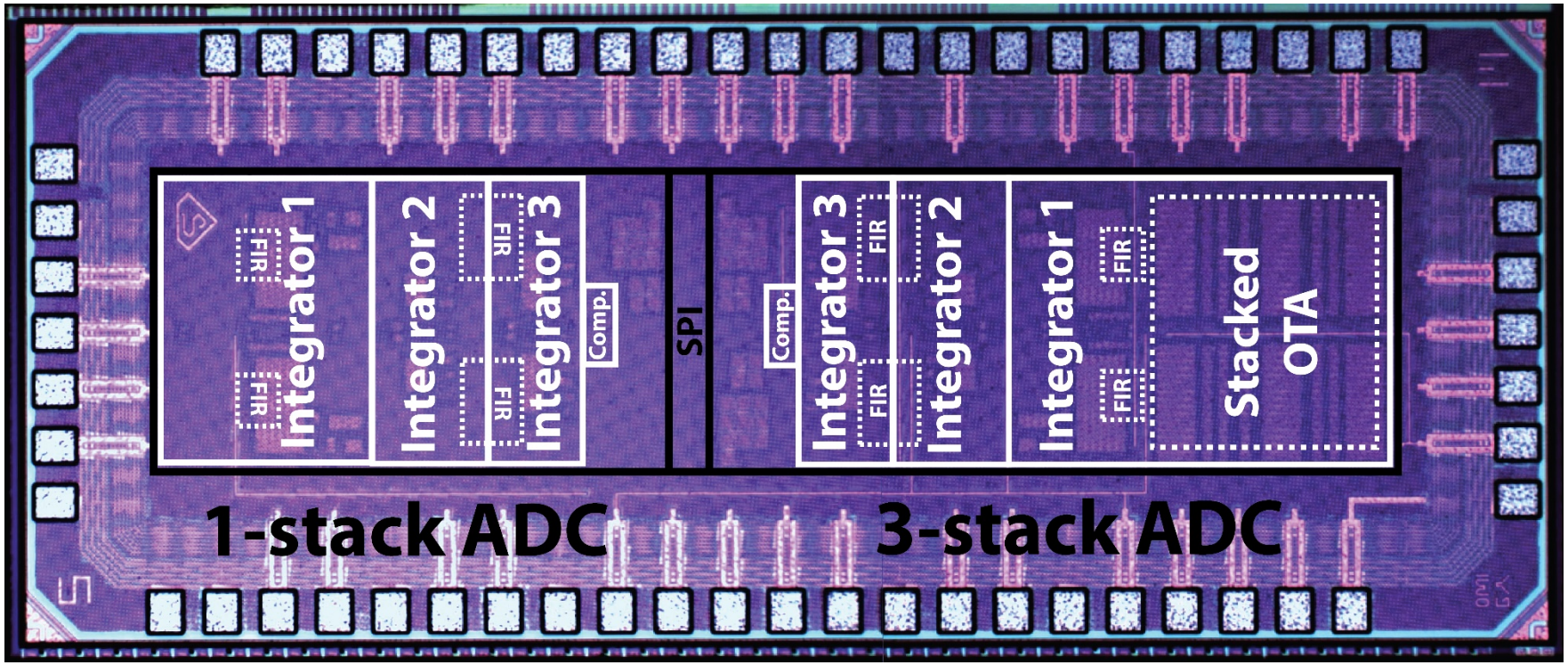


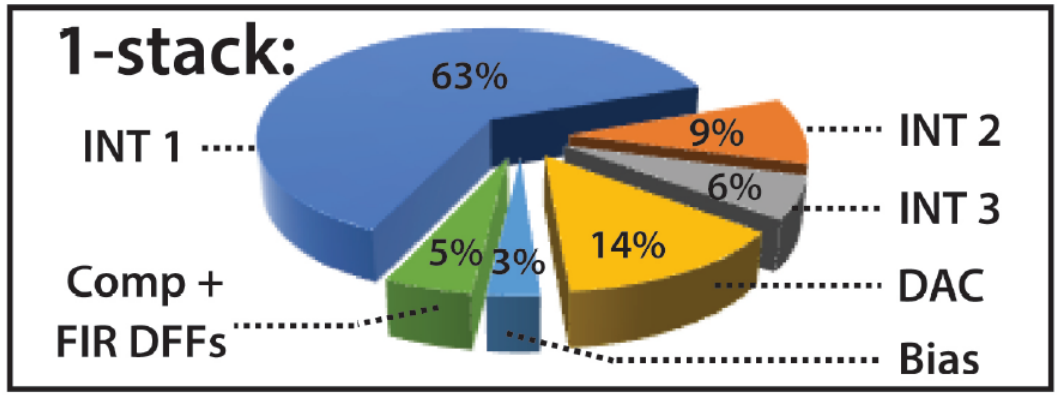
Feed-forward stage:

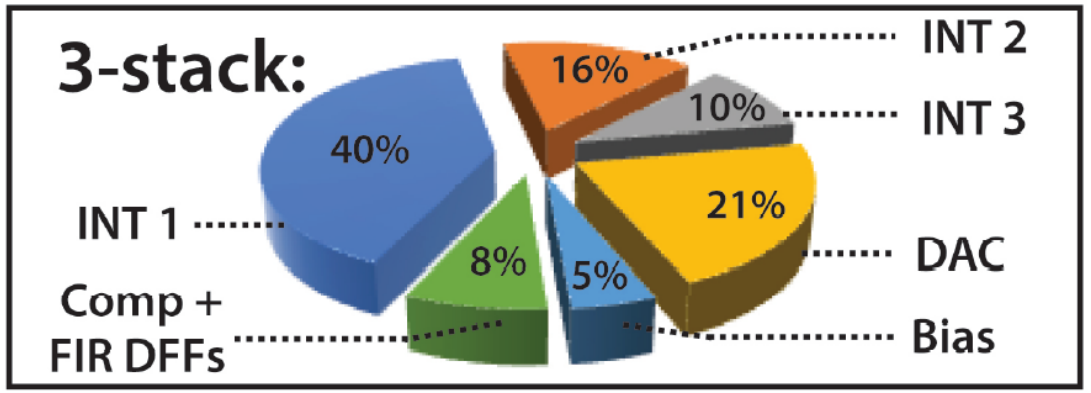


All other OTAs used are dual-tail inverter-based

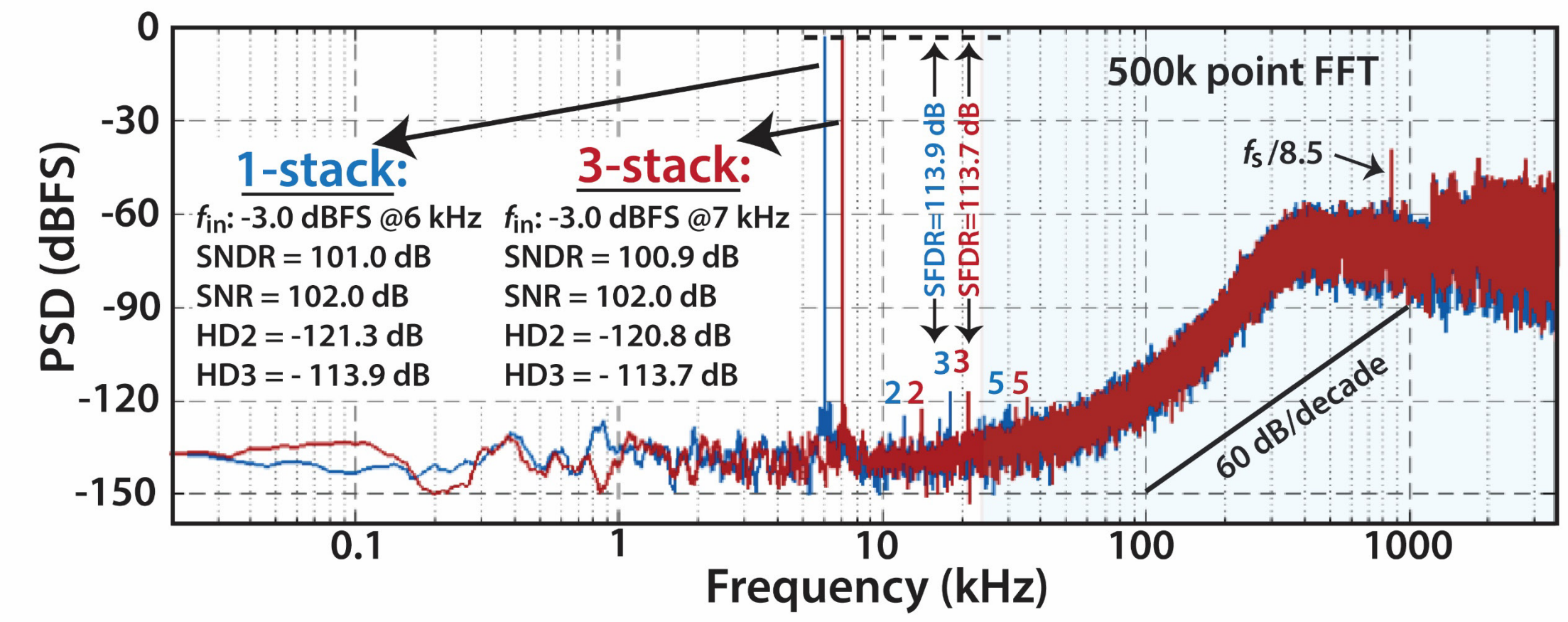
Chip Micrograph & Power Breakdown





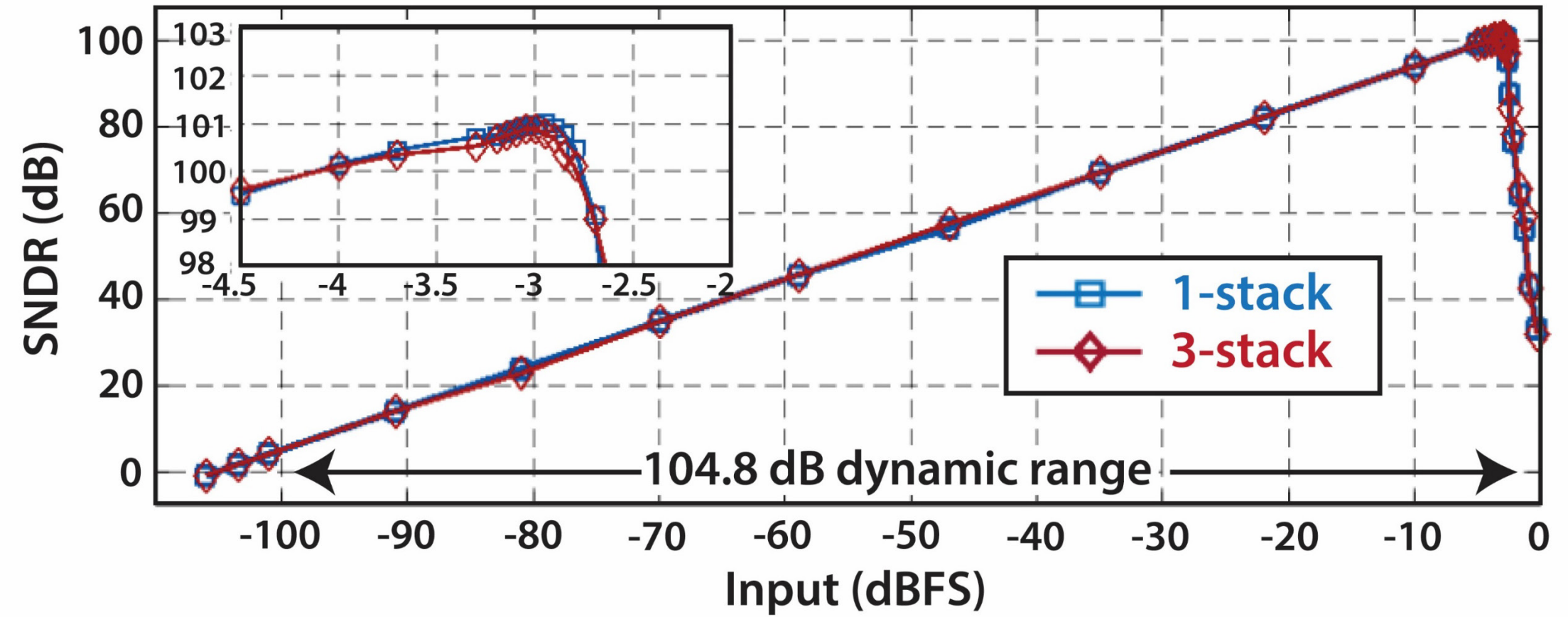


Measurement: ADC Spectra



~101 dB SNDR from both ADCs

Measurements: ADC Dynamic Range

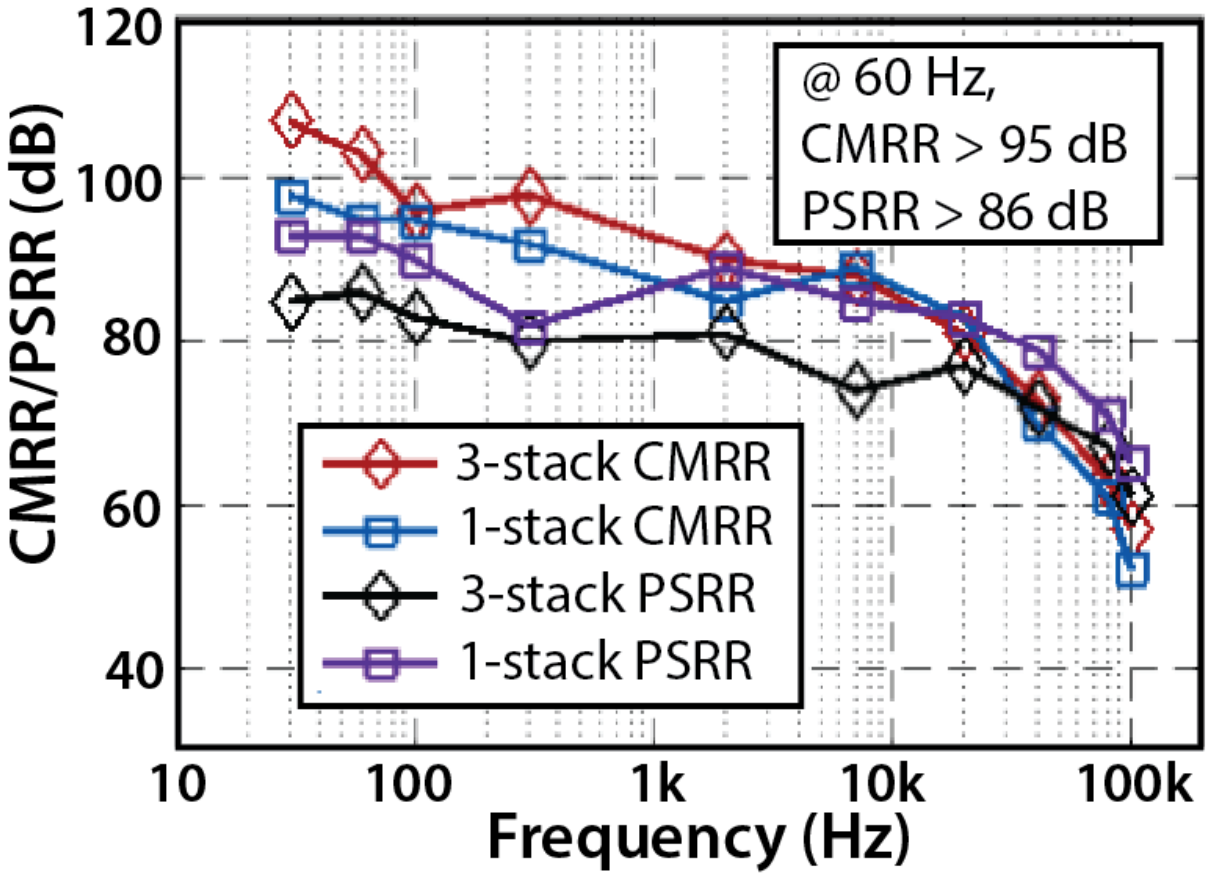


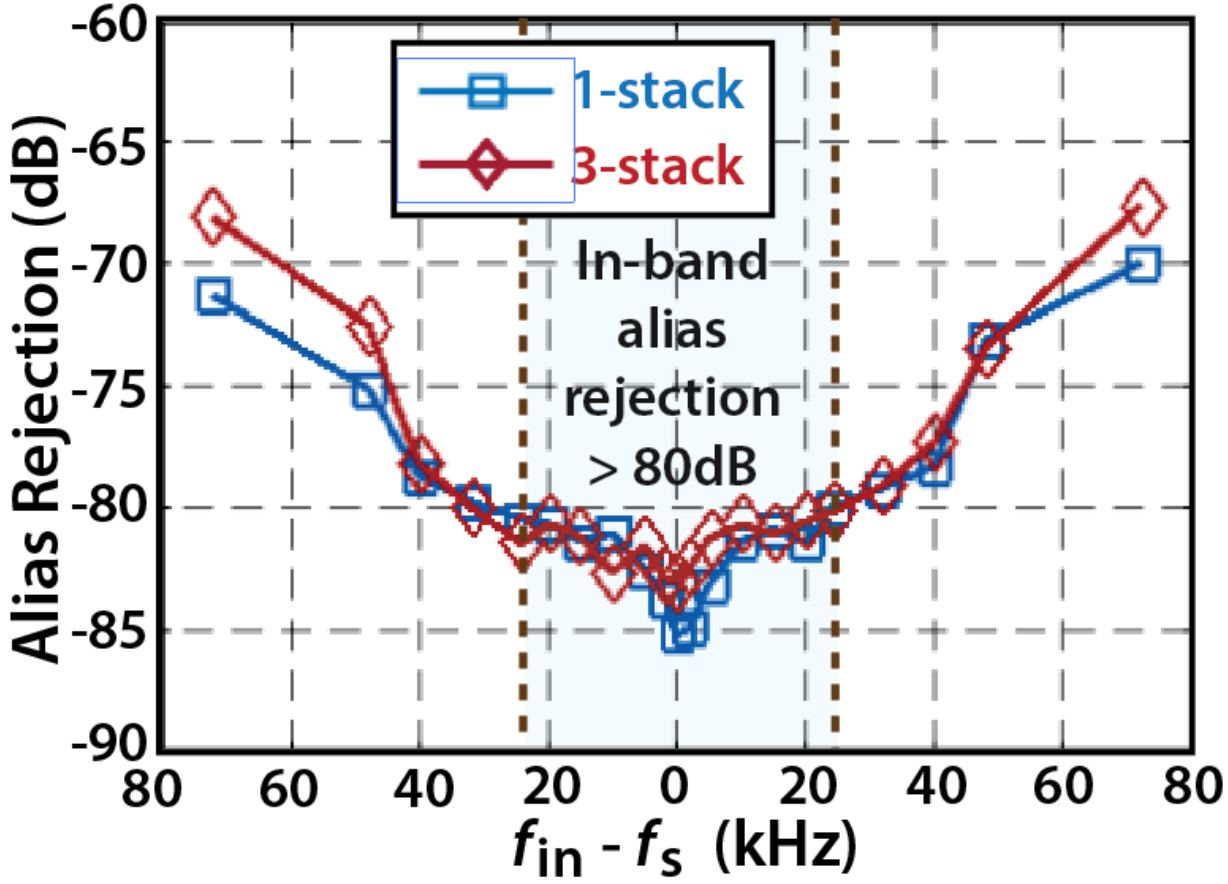
Theoretical ↑ FoM
10log(3) = 4.8 dB

184.9 $\mathrm{FoM_{DR}}$ from the 1-stack
187.2 $\mathrm{FoM_{DR}}$ from the 3-stack

Measured ↑ $\mathrm{FoM_{DR}}$
2.3 dB

Measurements: CMR, anti-aliasing





Measurements Summary

	Eland VLSI'20	Jang ISSCC'20	Billa JSSC'20	Gonen VLSI'19	Chandra. ISSCC'18	This Work	
						1-stack	3-stack
Topology	DT 2b Zoom	CT 1.5b Neg.-R FIR DAC	CT 1b MASH FIR DAC	CT 1b Zoom	CT 6b w/ gain stage	**CT 1b FIR DAC OTA-stacking**	
Input	switch-cap	resistive	resistive	resistive	cap-coup.	**resistive**	**resistive**
Tech. (nm)	160	65	180	160	40	**65**	**65**
Area (mm^2)	0.27	0.28	0.64	0.27	0.053	**0.25**	**0.39**
Supply (V)	1.8	1.2	1.8	1.8	1.2	**1.2**	**1.2**
BW (kHz)	20	24	24	20	5	**24**	**24**
f_s (MHz)	3.5	8	6.144	5.12	0.2	**7.2**	**7.2**
SNR_{max} (dB)	107.5	101	101.7	108.1	94.3	**102.0**	**102.0**
$SNDR_{max}$ (dB)	106.5	99.4	100.9	106.4	93.5	**101.0**	**100.9**
DR (dB)	109.8	103.5	104	108.5	96.5	**104.8**	**104.8**
SFDR (dB)	-	110.2	108	-	102.5	**113.9**	**113.7**
Power (μW)	440	134	550	618	4.5	**232**	**139**
FoM_{SNDR}	183.1	181.9	179.6	181.5	184	**181.1**	**183.3**
FoM_{DR}	186.4	186	182.7	183.6	187	**184.9**	**187.2**

State-of-the-art FoM among comparable works is reported from 3-stack version

Measurements Summary

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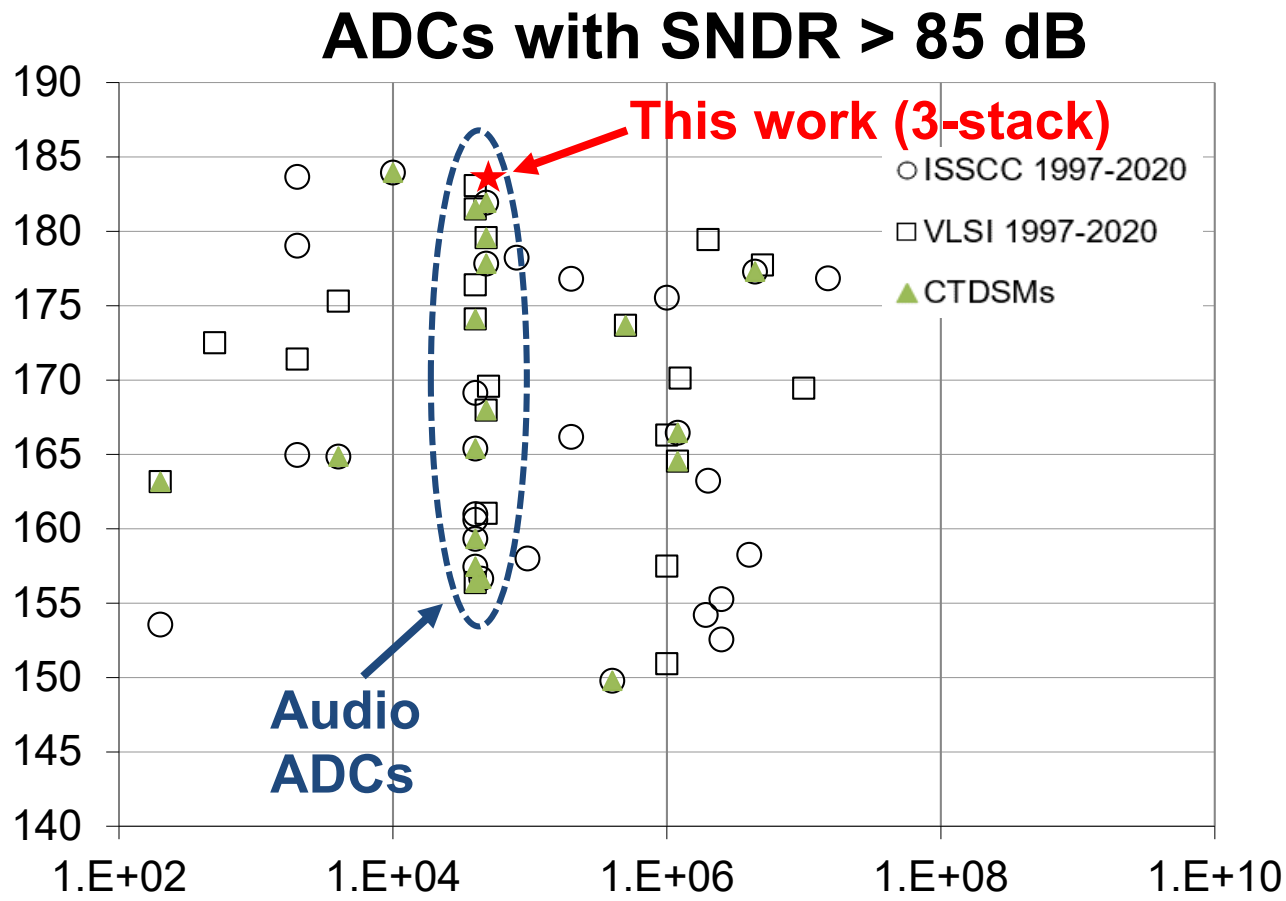

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Conclusion

OTA-Stacking for Noise Efficiency Enhancement

"A fundamental technique to overcome noise-power trade-off for oversampling ADCs"

Demonstrated a 139 µW, 104.8-DR Audio CTΔΣM

- ✓ CTDSMs benefit from both increase in supply and stacking
- ✓ FIR feedback with spectral nulls makes OTA-stacking viable
- ✓ A 2.3 dB FoM improvement in an ADC by 3-fold stacking was demonstrated
- ✓ State-of-the-art 187.2 dB FoM from 3-stack ADC

Can be ubiquitously incorporated to improve performance of almost all sensor front-ends!

Acknowledgements

UCSD Center for Wireless Communications for student support

Thank You!

Somok Mondal
Email: somondal@ucsd.edu