A 13.9-nA ECG Amplifier Achieving 0.86/0.99 NEF/PEF Using AC-Coupled OTA-Stacking

Somok Mondal, *Student Member, IEEE*, and Drew A. Hall, *Senior Member, IEEE*

***Abstract*— An ultra-low power electrocardiogram (ECG) recording front-end intended for implantable sensors is presented. The noise-limited, high power first stage of a two-stage amplifier utilizes stacking of operational transconductance amplifiers (OTAs) for noise and power efficiency improvements. The proposed technique involves upmodulated/chopped signals being applied to ac-coupled, stacked inverter-based OTAs that inherently sum the individual transconductances while reusing the same current, thereby enhancing the noise efficiency. Two prototype designs were fabricated in a 180-nm CMOS process. The three-stack version consumes 13.2 nW and occupies 0.18 mm^2, whereas the five-stack implementation consumes 18.7 nW and occupies 0.24 mm^2. State-of-the-art NEF and PEF metrics of less than unity, 0.86 and 0.99, respectively, are reported for the five-stack version. These correspond to ∼3× improvement in terms of energy efficiency compared to prior ultra-low power, sub-100-nW amplifiers.**

***Index Terms*— Chopper amplifier, current reuse, electrocardiogram (ECG), inverter-based operational transconductance amplifier (OTA), low power, noise efficiency.**

I. Introduction

THE Internet-of-Things (IoT) concept has created widespread interest in miniaturized sensor nodes ranging from biological sensors for healthcare monitoring [1]–[7] to physical sensors for infrastructure, industrial, and environmental monitoring [8]–[10], as shown in Fig. 1(a). From a healthcare perspective, there is a significant interest in implantable devices due to their unobtrusive nature, improved environmental artifact tolerance, and that some biological signals can be only be obtained *in vivo* [11], [12]. With respect to an electrocardiogram (ECG) recording, the focus of this article, the key benefits associated with implantable operation include a stronger signal [13], better rejection of interference (*e.g.,* 50/60 Hz) [2], and immunity to motion artifacts and baseline wander due to a more robust electrode-tissue contact [14], [15].

However, to realize the unobtrusive form factor, there are constraints on the allowable battery capacity. For example, the state-of-the-art commercial, 190−μWh thin-film battery (7−mm^3), [16] enables a one-year lifetime when the sensor is limited to 20 nW. Similarly, state-of-the-art energy harvesters offering 7.4-μW/cm^3 power density [17] translate to a 3-mm^3 device for the same 20-nW power budget. This is a very challenging aspect for the realization of implantable devices that acquire high fidelity bio-signals and simultaneously require long lifetimes. While several microwatt-level ECG analog front end (AFEs) for wearable applications were reported over the last decade [18]–[20], recent AFEs intended for implantable applications must deal with even more stringent power budgets [1], [2].

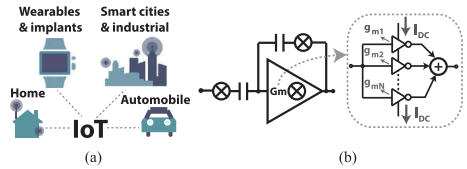

Fig. 1. (a) Examples of IoT sensor-node applications. (b) Block diagram of the proposed OTA-stacking technique.

For most sensors, including ECG, the amplifiers in the AFE sense weak, low-bandwidth signals and are noise-limited. Improving their noise efficiencies has always been an important design objective, often quantified using metrics such as the noise efficiency factor (NEF) and power efficiency factor (PEF). To improve the energy efficiency, a new technique based on operational transconductance amplifier (OTA)-stacking with chopping, as shown in Fig. 1(b), was proposed in [21] and is implemented here. This is an extension of the classical current reuse technique where the transconductances are summed [22]–[24]. The proposed technique fits nicely with capacitively coupled amplifier topologies used for biopotential recordings and, despite a shortcoming of increased area, which only marginally impacts the overall device form factor considering the large battery dimension needed for high longevity, is a useful technique for implantable ECG sensors in which ultra-low power operation is critical.

To explore the design space, prototype ultra-low power ECG amplifiers with three- and five-stack versions were designed and fabricated in a 180 nm CMOS process. The three- and five-stack designs consume 13.2 and 18.7 nW, respectively. State-of-the-art NEF and PEF metrics of less than unity, 0.86 and 0.99, respectively, are reported. The rest of this article is organized as follows: Section II briefly reviews the NEF and PEF metrics and prior art. Section III introduces the proposed stacking technique. Section IV describes the circuit architecture followed by implementation details in Section V. Measurement results and a conclusion are presented in Sections VI and VII, respectively.

Manuscript received May 21, 2019; revised August 20, 2019 and November 9, 2019; accepted November 21, 2019. Date of publication December 13, 2019; date of current version January 28, 2020. This article was approved by Associate Editor Azita Emami. This work was supported in part by the UCSD Center for Wireless Communications and in part by a DURIP Award from the Office of Naval Research under Award N00014-18-1-2350. *(Corresponding author: Drew A. Hall.)*

The authors are with the Department of Electrical and Computer Engineering, University of California at San Diego, La Jolla, CA 92093 USA (e-mail: drewhall@ucsd.edu).

Color versions of one or more of the figures in this article are available online at http://ieeexplore.ieee.org.

Digital Object Identifier 10.1109/JSSC.2019.2957193

II. Amplifier Noise Efficiency: Background

We briefly review the NEF and PEF metrics and relevant prior work to set the stage for the proposed work. The NEF, introduced in [27], captures the noise-current tradeoff

$$NEF = v_{\mathrm{ni,rms}}\sqrt{\frac{2I_{\mathrm{tot}}}{V_{\mathrm{T}}4k_{\mathrm{B}}T\pi BW}} \tag{1}$$

where V_{T} is the thermal voltage, k_{B} is Boltzmann's constant, T is the temperature, I_{tot} is the amplifier's current, BW is its bandwidth, and $v_{\mathrm{ni,rms}}$ is its input-referred noise. The NEF benefits from maximizing the transconductance efficiency $g_{\mathrm{m}}/I_{\mathrm{D}}$, where g_{m} is the transistor's transconductance and I_{D} is the drain current. A common technique to achieve this is to bias the transistors in subthreshold [28]. Correspondingly, a theoretical limit NEF_{o} is set [29], which for a fully differential topology with κ, the gate coupling coefficient, being 0.7, and considering only the input pair's thermal noise, evaluates to

$$NEF_{\mathrm{o}} = \sqrt{2/\kappa^2} \cong 2.02. \tag{2}$$

This implies that even with optimal sizing, a designer can, *at best*, achieve an NEF of 2.02. Overcoming this limit has therefore been the subject of intense research [19]–[24].

The concept of current reuse is commonly employed in this regard and has taken several forms over the years. The most simplistic form is to use inverter-based OTAs to double the transconductance [30], [31] and reduce the NEF limit to 1.43. Stacking can further increase the extent of the current reuse. To the best of our knowledge, this was originally proposed in a patent [25] and although not intended for noise benefit, the same current was reused among independent amplifiers in a multi-channel configuration to save power. More recently, this idea was proposed in [26] by stacking differential pairs for orthogonal current reuse among multiple channels. An analogous single-channel version was subsequently proposed with chopper amplifiers in [22] by applying the same input modulated/chopped at different frequencies onto stacked differential pairs. For the ADC in [23], inverter-based OTAs were stacked and a closed-loop, switched capacitor amplifier was realized using split arrays of feedback and sampling networks corresponding to each stacked stage. A technique involving an ac-coupled OTA with applicability for capacitively coupled, closed-loop chopper amplifiers was proposed by Mondal and Hall [21], which is the basis behind the implementation in this article. Another recent work [24] has also utilized the stacking concept for a closed-loop amplifier and is a continuous-time counterpart to [23] using split-capacitor arrays. Aside from amplifiers, this stacking technique has also been used in a crystal oscillator to leverage the g_{m}-boosting and sustain oscillation with lower power [32].

While both the NEF and the PEF are used in practice as metrics, the PEF, defined in [33] as NEF^2V_{DD}, is more relevant in quantifying a low-power design since it captures the actual noise–power tradeoff with V_{DD} being the supply voltage. Incidentally, the previous best reported PEF was from a low supply (0.45 V) design using a simple dual-tail inverter-based OTA with twofold current reuse [34]. Although prior work with six-fold amplifier stacking [22], [24] has reported superior NEFs, the PEFs are worse. This stems from overheads of associated summation circuits, resulting in the NEF not scaling aggressively enough to counter the required increase in supply voltage.

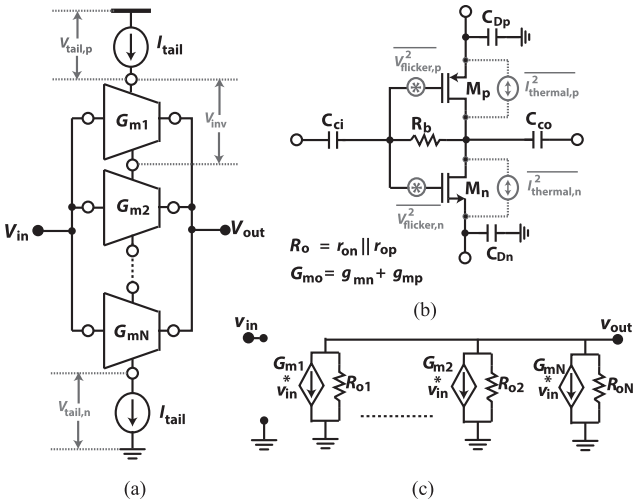

Fig. 2. Schematic of the proposed (a) stacked OTA, (b) ac-coupled inverter-based transconductor, and (c) equivalent small-signal model.

Other techniques to improve the PEF include removing the tail source to operate the first stage of a two-stage amplifier at a lower supply voltage (0.2 V) [35] and dynamically reconfiguring the amplifier for data-dependent power savings [3]. The former requires an additional common-mode rejection (CMR) circuit with power overhead. Furthermore, the CMR functionality is inevitably compromised being only possible for low frequencies and requires the chopping frequency to be much higher than the desired CMR frequency range, which is not always feasible at such low power levels. Dual supply generation is another shortcoming. The latter work relies on an ECG specific quasi-periodicity signal property and is not generalizable to all applications. Another NEF/PEF reduction technique was proposed in [36] by sharing parallel OTAs for the reference electrode but is applicable only for neural array applications.

A common drawback of prior amplifier stacking implementations is the use of additional power-consuming circuits for the output summation. In [22], fourth-order filters are required and the implementation is open loop with limited linearity. In [23], [24], active circuits are required to sum the currents. Another significant shortcoming is the single gain stage, which is a consequence of the proposed implementation in which the summation currents are driven onto arrays of feedback capacitors of the same amplifier and is needed to realize the g_{m}-boosting. The closed-loop gain, gain accuracy, and linearity are limited if the open-loop single-stage gain is not high enough. Noise attenuation from succeeding stages is also lowered. Finally, circuit complexity is increased if additional loops (*e.g.,* impedance boosting, offset rejection, and so on) also needed to be arrayed.

III. OTA-Stacking Principle

The proposed OTA-stacking principle and the resulting noise-efficiency benefits are explained in this section with

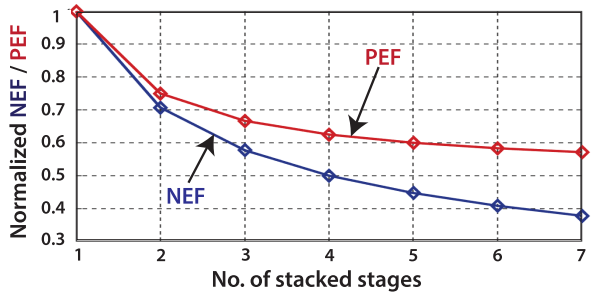

Fig. 3. Tradeoffs associated with the number of stacked stages.

the help of a single-ended version for simplicity. As shown in Fig. 2(a), multiple OTA stages are stacked on top of one another. Each stage is realized as an inverter that traditionally offers a $2\times$ transconductance improvement ($g_{mp} + g_{mn}$) and, as shown in Fig. 2(b), is self-biased through the same, reused dc current, I_{tail}. Since all the transistors operate in subthreshold carrying the same current, each stage has an identical small-signal equivalent circuit exhibiting the same transconductance $G_{mo} = 2g_m = 2\kappa I_{tail}/V_T$ and the same output impedance, R_o. Furthermore, the inputs and outputs are all ac-coupled through capacitors, C_{ci} and C_{co}, respectively. The adjacent stacked stages, on the other hand, are decoupled from one another using $C_{Dp,Dn}$. In a differential implementation, as will be discussed later, this decoupling occurs inherently with the relevant nodes being virtual grounds in the differential-mode operation. This ac-coupling and decoupling results in the simplified small-signal equivalent circuit shown in Fig. 2(c) in which all the individual transconductances G_{mi} sum and the output impedances appear in parallel. Thus, the overall compound transconductance G_m from stacking N stages is increased by the factor N and the compound output impedance R_{out} is reduced by $1/N$. The open-loop gain of this stacked OTA remains the same as that of a single stack, $A_v = G_m R_{out} = G_{mo} R_o$.

A. Input-Referred Noise

Although OTA-stacking does not offer any improvement in the gain, it results in lower noise. Since the thermal noise currents from each stacked transistor shown in Fig. 2(b) are uncorrelated, they sum at the output. Henceforth, due to the G_m-boosting, the total input-referred thermal noise power spectral density (PSD) from stacking N inverter-based OTAs is

$$\overline{v_{ni,thermal}^2} = \frac{4k_B T\gamma}{2Ng_m} \tag{3}$$

where γ is a technology-dependent noise coefficient. Thus, there is a reduction in the thermal noise power by a factor of $1/N$. The flicker noise, henceforth referred to as $1/f$ noise, can be found by modeling each transistor's noise contribution as a voltage source in series with the gate, as shown in Fig. 2(b). Assuming that these flicker noise sources also result in uncorrelated output noise currents that add up, the total input-referred $1/f$ noise PSD from stacking N inverter-based OTAs is

$$\overline{v_{ni,1/f}^2} = \frac{1}{4Nf}\left[\frac{K_n}{C_{ox}(WL)_n} + \frac{K_p}{C_{ox}(WL)_p}\right] \tag{4}$$

TABLE I
EFFECT ON CIRCUIT PARAMETERS WITH $N\times$ INVERTER STACKING

Parameter	Effect	Parameter	Effect
G_m	$\uparrow N\times$	R_o	$\downarrow N\times$
A_v	–	BW	$\uparrow N\times$
$\overline{v_{ni,thermal}^2}$	$\downarrow N\times$	$\overline{v_{ni,1/f}^2}$	$\downarrow N\times$
NEF	$\downarrow \sqrt{N}\times$	PEF [#]	$\downarrow 2/(1+1/N)\times$
$V_{DD,min}$	$\uparrow (N+1)\times$	Area	$\uparrow N\times$

[#] For $V_{inv} = V_{tail}$

where $K_{n,p}$ are technology-dependent noise constants for NMOS and PMOS devices, respectively, C_{ox} is the oxide capacitance per unit area, W and L are the transistor sizes, and f is the frequency. Thus, the $1/f$ noise is also reduced by the same $1/N$ factor due to OTA-stacking. However, $1/f$ noise from stacked devices may exhibit partial correlation, and hence, the noise reduction is not direct. This is because the $1/f$ noise is known to have a dependence on the drain current and its fractional changes due to charge traps [37] and the drain current flowing through one device in a stack is also dependent upon the noise of the other devices. It may be noted that the actual noise reduction factor in (4) cannot be measured and hence cannot be conclusively stated. Nevertheless, chopping removes the $1/f$ noise, whereas the white noise, which is uncorrelated, has obvious benefits from the proposed stacking.

B. NEF/PEF Improvement

With chopping, the reduction in thermal noise by a factor $1/N$ discussed in (3) translates to an improvement over the NEF_o in (2) by a factor $\sqrt{2N}$, given that the other amplifier parameters, such as BW and I_{tot} in (1), remain the same. Thus, the theoretical NEF limit for a three stack of inverters is improved by $\sqrt{6}$ to 0.82 and a five stack is improved by $\sqrt{10}$ to 0.63. These improvements suggest that larger N would continue to improve the amplifier's efficiency. While the NEF does continue to benefit from increasing N, the PEF saturates since one also needs to increase the supply voltage to accommodate the increased number of stacked stages. For the stacked-OTA in Fig. 2(a), one can express the minimum operable supply $V_{DD,min}$ as

$$V_{DD,min} = NV_{inv} + V_{tail} \tag{5}$$

where V_{inv} and V_{tail} are the voltage headrooms allotted to each inverter and the combination of the two tail current sources (*i.e.* $V_{tail,p}+V_{tail,n}$ in Fig. 2). With the NEF $\propto 1/\sqrt{N}$, it follows that the PEF corresponding to the minimum supply voltage in (4) is

$$PEF \propto V_{inv} + \frac{V_{tail}}{N}. \tag{6}$$

As N becomes large, V_{tail}/N is small relative to V_{inv}, and thereby, further increasing N only marginally improves the PEF. For illustrative purposes, plots of the normalized NEF and PEF with $V_{inv} = V_{tail}$ (*i.e.* equal headroom across the drain–source terminals of each transistor) are shown in Fig. 3. It may be noted that a minimum PEF can be obtained by

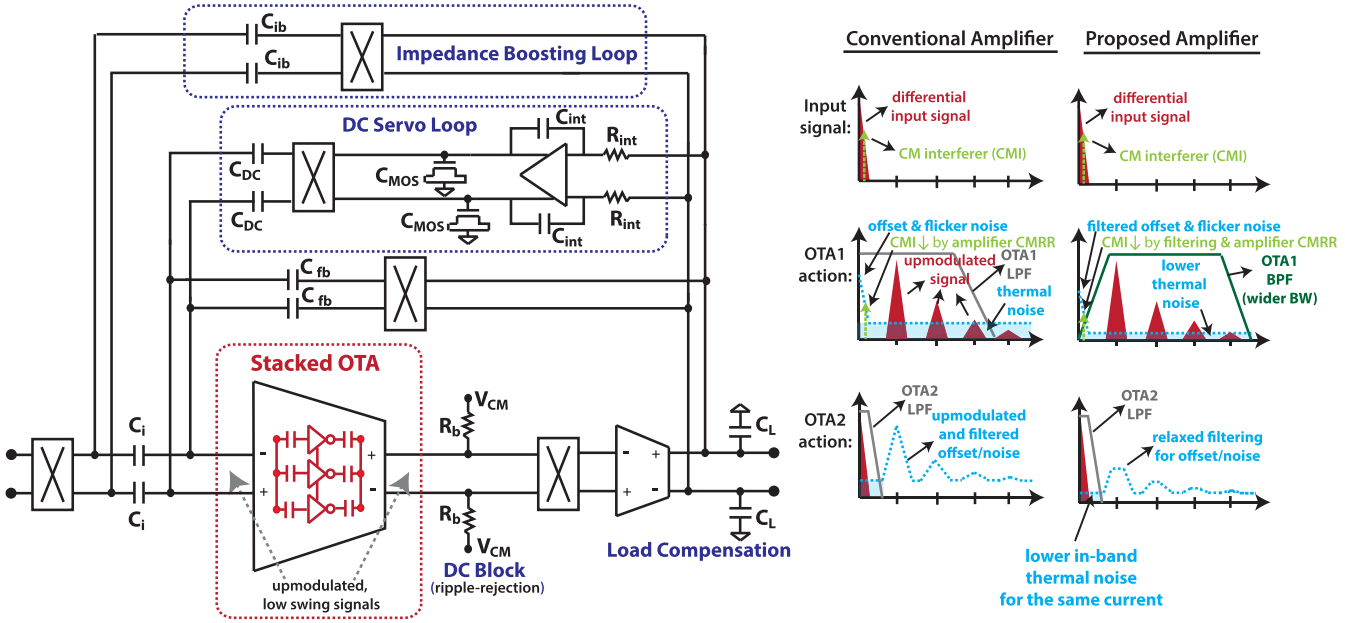

Fig. 4. Chopper-stabilized ECG amplifier: architecture and illustration of functional benefits.

removing the tail source altogether without any OTA-stacking; however, tail sources are necessary to establish a well-defined nanoampere-level current and to achieve good CMR. Overall, OTA-stacking helps in that it diminishes the tail source's power contribution. It may also be noted that a single-ended amplifier exhibits a lower NEF limit of 0.7 [38] for one stack, which improves similarly with stacking and should be used, if the application permits.

C. OTA-Stacking Tradeoffs

Table I summarizes the effect of OTA-stacking on various amplifier parameters. The G_m-boosting also results in an $N\times$ increase in the bandwidth. Although the bandwidth requirement for the targeted application is not important, there are benefits with respect to chopping in which a higher bandwidth is needed by the stage processing the upmodulated chopped signals. This aids in easier settling of upmodulated signals, thereby reducing the chopper settling spikes/ripple. A potential drawback of the OTA-stacking is that it leads to a slight increase in the input parasitic capacitance degrading the feedback factor and, thus, the input-referred noise in a closed-loop amplifier. Inevitable drawbacks are the increase in area and supply voltage, which needs to be traded for improvements in the power efficiency.

IV. ECG Acquisition Amplifier

A. Application-Specific Requirements

An important requirement while amplifying weak ECG signals is to introduce minimal noise. The noise specification typically depends on the downstream signal processing. Early ECG AFEs, such as [18], targeted an input-referred noise floor ~60 nV/$\sqrt{\text{Hz}}$ to ensure high accuracy at the expense of microwatt-level power consumption. However, the stringent power budget of a few tens of nanowatts is more critical for implantable sensors. Ultra-low-power AFEs exhibiting 1400- and 250-nV/$\sqrt{\text{Hz}}$ noise floors have hence been reported in [1] and [2], respectively, and are applicable for arrhythmia detections. Accurate QRS-detection with a noise floor of 126 nV/$\sqrt{\text{Hz}}$ has been demonstrated in [3]. In this article, a 150-nV/$\sqrt{\text{Hz}}$ noise floor is targeted while meeting a stringent power budget of less than 20 nW.

Aside from the power budget, there are additional requirements as follows. 1) The $1/f$ noise that would otherwise be dominant in the bandwidth of interest must be mitigated. 2) Due to electrode polarization, a large dc offset appears at the amplifier inputs and must be rejected to avoid saturating the amplifier. 3) Implantable ECG devices use electrodes that are in direct contact with subcutaneous tissue [39]. The associated electrode-tissue impedances are typically high (~100 kΩ) for implantable electrodes [40], and hence, the input impedance of the AFE should be sufficiently higher to prevent signal attenuation and avoid other issues/artifacts arising from electrode mismatch. 4) The recording environment is often prone to interference (*e.g.,* 50-/60-Hz power line interference) and motion artifacts, and thus, high amplifier CMR ratio (CMRR) and power supply rejection ratio (PSRR) are also important. It turns out that these additional considerations while being accounted for by using standard techniques have only a minimal impact on the power consumption compared to the noise specification. Improving the thermal noise efficiency by OTA-stacking offers significant benefits.

A few key challenges need to be addressed to employ the proposed OTA-stacking technique for an ECG amplifier. Since the ECG is a slowly varying signal (BW of ~250 Hz), ac-coupling at such frequencies would require large capacitors, possibly prohibitively large for an on-chip implementation. Furthermore, although OTA-stacking offers higher current reuse, it limits the transistor's headroom lowering the allowable swing. The first concern can be

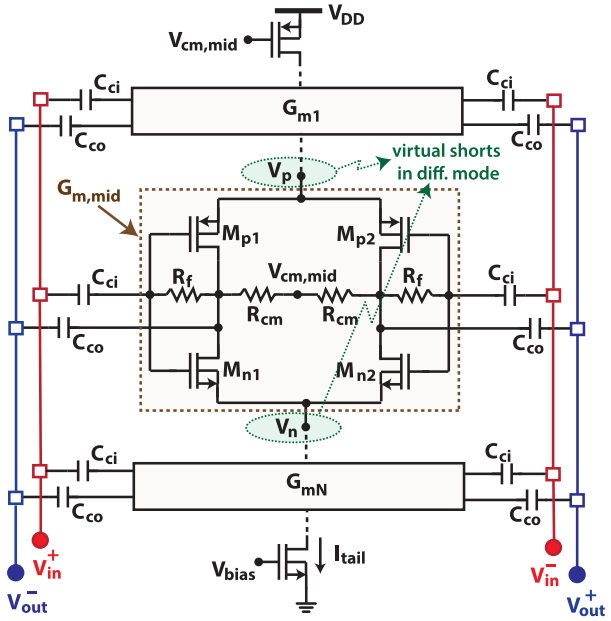

Fig. 5. Circuit implementation of the fully differential stacked-OTA.

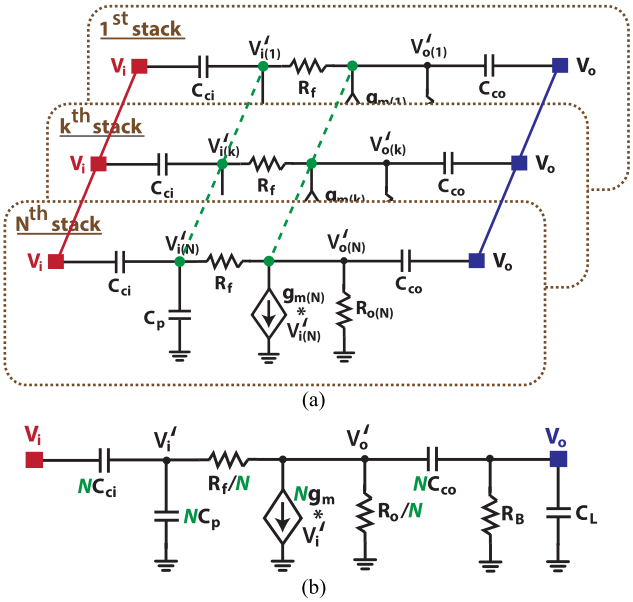

Fig. 6. Differential-mode (a) small-signal model of the stacked-OTA and (b) equivalent simplified circuit.

resolved by upmodulating the baseband signals to a higher frequency using the well-established technique of chopper stabilization, which is also required to mitigate the $1/f$ noise. The limited headroom issue can be addressed by using OTA-stacking only at low swing nodes, such as the first stage of a two-stage amplifier.

B. Architectural Overview

The capacitively coupled chopper amplifier architecture shown in Fig. 4 is similar to the ones presented in [41] and [42]. Since the target specs are such that the noise requirement is far more stringent than the bandwidth, the first stage usually consumes a significant portion of the power budget and is a prime candidate for OTA-stacking. It is also clear that this stacked-OTA only processes upmodulated, low swing signals. As a result, the ac-coupling is naturally simplified since the signal of interest lies at the chopping frequency and the implementation is now possible using smaller, on-chip capacitors. Ensuring the operation of all stacked transistors in saturation becomes much easier with the associated voltage swings being negligible and helps maintain high linearity. The low swing also helps in that the G_m-boosting is strictly valid only for small signals.

Down-chopping is performed at an intermediate node before the second stage to suppress distortion due to chopper settling errors using the inherent feedback [41]. With the first stage outputs ac-coupled, the second stage requires additional biasing resistors R_b to set its dc input common-mode voltage. The coupling capacitors of the stacked-OTA along with these biasing resistors result in high-pass filtering. The placement of R_b before the down-chopper ensures that the relevant up-modulated signals remain unaffected. Moreover, the dc-blocking between the first and second stages adds a ripple-rejection functionality to the amplifier [4]. It may be noted that the stacked-OTA also requires resistors for self-generation of the bias potentials that similarly adds to the dc-blocking action. Since low-frequency common-mode interferers are not up-modulated by chopping, these are high-pass filtered by the first stage thereby further improving the CMR. To summarize, contrary to a conventional amplifier, the first stage acts as a bandpass filter rather than a low-pass filter with additional benefits of wider bandwidth and, more importantly, lower noise due to the OTA-stacking.

The closed-loop gain is set by the ratio between the input and feedback capacitors C_i/C_{fb}. A dc servo loop (DSL) is implemented to suppress the otherwise amplified dc electrode offsets appearing at the amplifier output by integrating them and canceling at the input. The integrator is adopted from [43], which is fully realizable with on-chip components. The amplifier's high-pass cutoff frequency is set by the resistor R_{int} and capacitor C_{int}, whereas the DSL OTA's noise is band limited using large-valued MOS-capacitors, C_{MOS}. To address the degraded impedance at the input due to chopping before C_i, a positive feedback loop compensates the charge transfer boosting the input impedance [42]. The two-stage amplifier is load compensated for reasons discussed in Section V.

V. Circuit Description

The details of key circuit blocks and the associated design considerations are discussed next.

A. OTA Implementation

The fully differential version of the implemented stacked-OTA circuit is shown in Fig. 5. Each of the inverters is self-biased using resistive feedback through R_f, implemented as pseudoresistors. All the inverters' transistors have their body-source terminals tied together to avoid threshold voltage

variation from the body effect. This ensures symmetry to simplify and maintain robust operation from the self-biasing. The top transistors in the stack would otherwise have larger drain–source voltage V_{DS}, while the bottom ones would be pushed closer to triode. Deep n-well (DNW) devices were used to allow this body-source tie for the NMOS transistors. For both the three- and five-stack versions, transistors are sized such that nominally each inverter is allocated ~220-mV headroom leaving ~250 mV for the two-tail sources. This guarantees that all the transistors in subthreshold, considering the associated swing, are always in saturation ($V_{DS} > 100$ mV) across process corners, including the most critical slow–slow corner. Although the first-stage transistors are at the edge of saturation, the linearity is not compromised due to the negligible signal swing. The isolated DNWs have an area overhead that is negligible (<0.01 mm^2 for all transistors) compared to the coupling capacitor's area.

For the common-mode feedback (CMFB), a resistive divider senses the common-mode voltage of the central inverter to bias the top PMOS tail source. With this CMFB, the number of stacked stages is chosen to be odd as vertical symmetry is maintained. The overall amplifier is designed such that the dc gain from the first stage is ~25 dB, while the second stage is ~45 dB, and thus, the swing at the intermediate node is negligible. The second stage is implemented as a traditional inverter-based OTA with CMFB as in [1]. For higher intrinsic gain, I/O transistors are used in the second stage.

B. AC-Coupling/Decoupling of Stacked-OTAs

For proper ac-coupling, the capacitor values for C_{Ci} and C_{Co} shown in Fig. 5 need to be selected such that their impedances at the chopping frequency (1.5 kHz) are sufficiently smaller than the remaining impedance seen at that node. In other words, the high-pass cutoff frequency ω_{HPF} should be low enough to not affect the up-modulated signals. From the differential-mode small-signal model and the equivalent reduced circuit shown in Fig. 6, it can be found that the dominant contributors to ω_{HPF} are the feedback resistor R_f and capacitor C_{Ci}. Thus, ω_{HPF} is independent of N and expressed as

$$\omega_{HPF} \approx \frac{1}{(R_f + R_o)/(1+G_{mo}R_o)C_{ci}}. \tag{7}$$

With R_f implemented by pseudoresistors with high impedance, meeting this ac-coupling criterion is easy in practice. Additional constraints from attenuation of the open-loop gain perspective, however, need to be considered. As evident from Fig. 6, the mid-band gain, A_{v1}, of the stacked-OTA is attenuated by capacitive dividers

$$A_{v1} \approx \frac{C_{Ci}}{C_{Ci} + C_p} G_{mo} R_o \frac{NC_{Co}}{NC_{Co} + C_L} \tag{8}$$

where C_p is the total input gate capacitance of each inverter stage and C_L is the load seen by the overall OTA. With chopping, there is no need to increase the area of the transistors for $1/f$ noise reasons, and thus, C_p can be kept to a minimal size due to the ultra-low nanoampere bias current. Minimizing the output attenuation, however, has implications for the compensation used and is discussed later. It may also be noted from (8) that an increase in N with the same loading helps slightly lower the output attenuation. Considering these aspects, C_{Ci} and C_{Co} were chosen to be 9.5 and 11 pF, respectively. While these values are larger than the minimum required values (C_p and C_L of 150 and 800 fF, respectively), the large coupling capacitors aid in the noise reduction and CMR, as discussed later. The input side coupling here is realized using multiple additional, but smaller capacitors, unlike prior works, such as [24], where multiples/arrays of the otherwise larger amplifier input capacitors C_i, typically ~25 pF, for the application are used. Thus, the input coupling area overhead is lowered compared to prior work using stacked amplifiers. Additional area is needed for the output side coupling but with the benefit of the summation being performed passively without any power overhead.

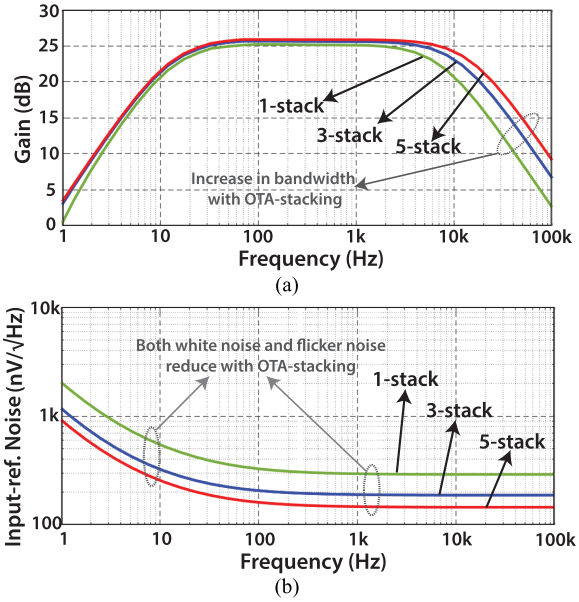

Fig. 7. Simulation of the stacked-OTA showing (a) open-loop frequency response and (b) input-referred noise.

Decoupling of the adjacent stages occurs inherently due to a fundamental property of differential amplifiers. The source nodes of the intermediate differential pairs (V_p and V_n in Fig. 5) act as virtual grounds for small signals in the differential mode. Explicit capacitors for decoupling are therefore not needed. Furthermore, since this decoupling occurs only with respect to the differential-mode operation while not affecting the common-mode operation, high CMRR and PSRR, as also analyzed later, are maintained.

The simulated open-loop frequency response of this ac-coupled stacked-OTA loaded by the second stage is shown in Fig. 7(a). The bandpass nature is evident with a high-pass corner set by the dc-blocking action and the low-pass bandwidth being expanded due to the G_m-boosting. It is worth noting that this bandwidth expansion from OTA-stacking is also leveraged here to enable chopping at lower power levels. Assuming similar loading conditions, a one-stack version has ~5-kHz bandwidth, which would not suffice to process the third (at 4.5 kHz) and higher harmonics of the

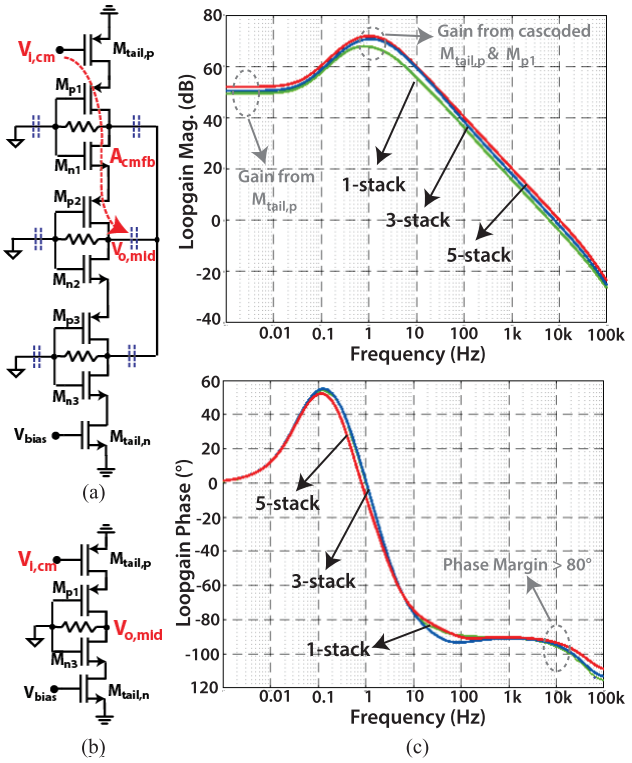

Fig. 8. Common-mode (a) half-circuit, (b) equivalent simplified circuit for a three-stack OTA, and (c) simulated CMFB loop-gain using stb analysis.

upmodulated signal. This becomes feasible with the >12-kHz bandwidth offered by the three- and five-stack versions implemented here. The improvements for both the $1/f$ and white noise are also shown in the simulated input-referred noise plots of Fig. 7(b) leading to a lower NEF and PEF.

C. Load Compensation

The mid-band gain expression for the stacked-OTA in (8) indicates that it is important to minimize the load capacitance seen by the first stage to avoid unwanted attenuation. The use of conventional Miller compensation in this regard is problematic since the effective load $C_c(1 - A_{v2})$ for a compensation capacitor C_c and second stage gain of A_{v2} would be very large. To avoid using a correspondingly large stacked-output coupling capacitor C_{co}, load compensation is instead employed.

The first stage offers low gain and high bandwidth, which is advantageous since it processes upmodulated chopped signals. The high-gain and low-bandwidth second-stage filters out the unwanted upmodulated components, meanwhile also ensuring that the swing is minimized. Compared to Miller compensation, which has the dominant pole associated with the first stage and wherein a higher second stage g_m aids the compensation, load compensation needs a lower second stage g_m, thereby making it easier to push the power burden solely onto the first stage in low-bandwidth applications.

D. DC Servo-Loop

The offset cancellation using a DSL further benefits from the higher supply V_{DD} required for OTA-stacking. The maximum offset that can be canceled can be expressed as $(C_{DC}/C_{in})V_{DD}$, where C_{DC} and C_{in} are the servo loop and the closed-loop amplifier's input capacitance, as shown in Fig. 4. This implies that with higher V_{DD}, a smaller offset canceling capacitor C_{DC} is needed for the same offset cancellation range. The closed-loop input-referred noise $\overline{v_{ni,amp}^2}$ degrades as

$$\overline{v_{ni,amp}^2} = \left(\frac{C_{in} + C_{fb} + C_{DC}}{C_{in}}\right)^2 \overline{v_{ni}^2}. \tag{9}$$

Since the input capacitance at the virtual ground node is dominated by C_{DC}, there is a reduced degradation of the closed-loop input-referred noise to reject the same amount of offset.

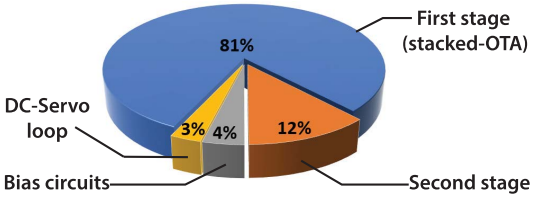

Fig. 9. Power distribution for the ECG amplifiers.

TABLE II
DEVICE SIZES AND COMPONENT VALUES

Stage 1 (stacked-OTA)			
$M_{pi}\left(\frac{W_p}{L_p}\right)$	$\frac{176\ \mu m}{0.18\ \mu m}$	$M_{ni}\left(\frac{W_n}{L_n}\right)$	$\frac{77\ \mu m}{0.18\ \mu m}$
C_{ci}	9.5 pF	C_{co}	11 pF
Capacitors			
C_i	23 pF	C_{fb}	400 fF
C_{DC}	1.8 pF	C_L	6 pF
C_{int}	4.5 pF	C_{ib}	400 fF
Currents			
Stage 1	11.25 nA	**Stage 2**	1.65 nA
Bias	560 pA	**DC-Servo**	420 pA

E. CMFB Stability

Since the gain from the tail current source to the central inverter, as highlighted in the common-mode half circuit of a three-stack inverter in Fig. 8(a), sees multiple stacked/cascoded devices, it may appear at first glance that the stability of the CMFB loop would be difficult to ensure due to very high gain and/or multiple poles. However, as a result of ac-coupling, all the inputs are shorted to ground, and more importantly, all the outputs are shorted together. Thus, the intermediate transistors do not impact the common-mode response, and hence, the CMFB stability behavior is analogous to the one-stack equivalent, as shown in Fig. 8(b). It should be noted the assumption of perfect ac-coupling has been made, which is valid in the vicinity of the unity gain frequency of the CMFB loop and in general is the case for all frequencies above the cutoff set by the output coupling capacitor and the high output impedance (<1 Hz in this design). The simulated CMFB loop gain is shown in Fig. 8(c). The dc loop gain is determined solely by the tail source (since the inverter OTAs have a direct dc path through R_f with unity gain at dc), while the mid-band gain is determined by the cascode of the tail source and the adjacent inverter. Both the three- and five-stack

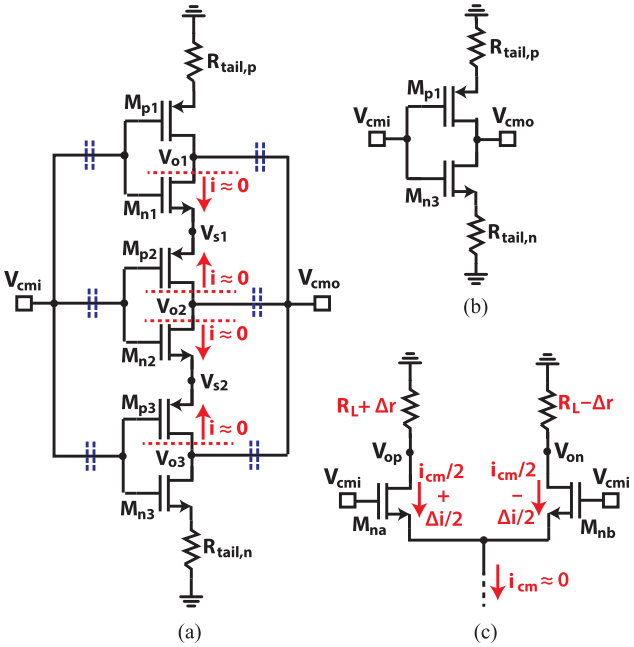

Fig. 10. Common-mode (a) half-circuit, (b) equivalent simplified circuit for a three-stack OTA, and (c) CMR by a mismatched differential pair.

versions exhibit similar frequency responses and the phase margin is greater than 80°.

F. Design Summary

The power breakdown of the two OTAs and the auxiliary components are summarized in Fig. 9 and are identical for both the three- and the five-stack versions. The DSL OTA is implemented as a simple NMOS input fully differential amplifier. All dc biasing resistors are implemented as high-impedance pseudoresistors. The common-mode voltage V_{CM} to bias the second stage is generated using a reference ladder with four series diode-connected PMOS devices in sub-threshold. The bias currents for the OTAs are set by a constant-g_{m} circuit using an external resistor. All capacitors in Fig. 4 (except C_{MOS}) and the coupling capacitors in Fig. 5 are implemented by MIM capacitors. All design values are identical for the three- and the five-stack amplifiers and summarized in Table II.

G. Amplifier Non-Idealities With OTA-Stacking

While offering reduced noise levels, it is important to ensure that the proposed OTA-stacking does not deteriorate other amplifier performance metrics. The potential amplifier non-idealities with OTA-stacking arising from mismatch and the presence of interferences are discussed in this section.

The headroom for each stacked inverter is minimal. It is hence possible that the swing and linearity at the amplifier's first stage output can get severely compromised due to the dc offsets resulting from mismatch. However, since each ac-coupled inverter has its own dc feedback through R_{f}, individual high-pass filtering avoids amplification of the offset from saturating the stacked inverters' outputs.

The behavior of the stacked-OTA from the CMR perspective is analyzed next. At low frequencies, the CMR is very good

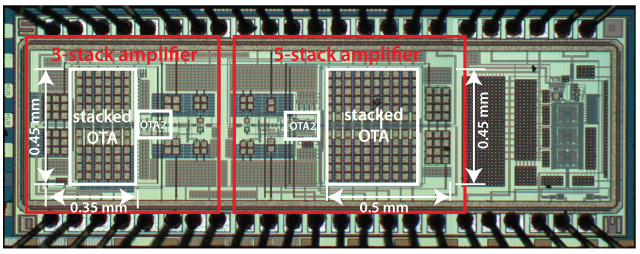

Fig. 11. Annotated chip micrograph.

due to the high-pass filtering as common-mode signals are not upmodulated by chopping. Additionally, in general, and at higher frequencies, the self-feedback mechanism, which results from the outputs being ac-coupled, assists in maintaining a good CMR. This mechanism can be understood from the common-mode half-circuit of a three-stack OTA in Fig. 10(a), which is redrawn and annotated differently for the ease of explanation. Assuming perfect ac-coupling, it is evident that there can be no common-mode small-signal current flowing across the intermediate stacked transistors $M_{\mathrm{n1,2}}$ and $M_{\mathrm{p2,3}}$ since the nodes $V_{\mathrm{o1,2,3}}$ are at the same potential. As such, the equivalent simplified circuit shown in Fig. 10(b) results. Thus, the common-mode response (*e.g.,* the common-mode gain) is mostly determined by the top- and bottom-most transistors and the associated tail current sources. Although low impedances are seen looking into the source nodes of other intermediate transistors at $V_{\mathrm{s1,2}}$, implying the absence of a conventional source degeneration, the associated common-mode gain contribution from these intermediate stages is still very low.

In practice, mismatch causes additional non-idealities with respect to common-mode-to-differential-mode conversion. Although, with chopping, these unwanted signal components are later up-modulated and filtered out, it is still important that their signal levels are low in the first stage. The impact of mismatch among intermediate differential pairs, in this case, is also reduced due to the above-mentioned self-feedback. This can be understood by first considering the CMR mismatched differential pair carrying a common-mode small-signal current i_{cm}, as shown in Fig. 10(c). In a traditional differential amplifier, the high impedance of the tail source causes the common-mode current to be minimal ($i_{\mathrm{cm}} \approx 0$). As such, the absolute difference Δi (*e.g.,* due to g_{m} mismatch) among the otherwise equally split versions of this small current is also small, thereby causing the resultant differential component $\Delta i\, R_{\mathrm{L}}$ to be small. Impedance mismatch Δr also results in a low differential amplitude $i_{\mathrm{cm}}\Delta r$. In the case of the stacked-OTA, the common-mode current associated with each intermediate differential pair is minimized by the self-feedback, thereby assisting the mismatch-related CMR in a similar fashion. Good CMRR/PSRR is henceforth maintained with the high tail source impedances aiding the CMR for M_{p1} and M_{n1} and the self-feedback doing the same for $M_{\mathrm{n1,2}}$ and $M_{\mathrm{p2,3}}$.

VI. Measurement Results

Measurement results from prototype amplifiers with three- and five-stack versions are presented in this section. Fabricated

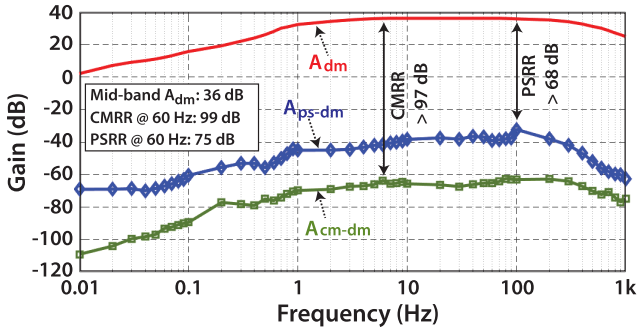

Fig. 12. Measured five-stack amplifier frequency response.

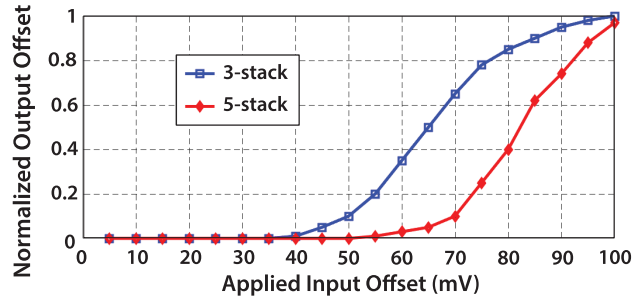

Fig. 13. Measured dc offset tolerance.

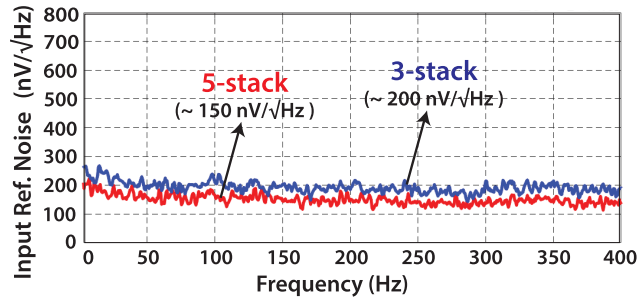

Fig. 14. Measured amplifier input-referred noise.

in a TSMC 180-nm CMOS process, the two amplifiers occupy a 2×1 mm^2 area, including pads. The total active area occupied by the three- and five-stack amplifiers is 0.18 and 0.24 mm^2, respectively, and mostly dominated by the MIM capacitors. An annotated chip micrograph is shown in Fig. 11. The nominal supply voltages selected for the three- and five-stack versions are 0.95 and 1.35 V, respectively. It should be noted that in comparison with the prior best reported PEF work [34] in which a 0.45-V supply (0.2 V for inverter and 0.25 V for tail sources) was used for a four-transistor inverter-based OTA, the supply voltages here are higher (analogous headroom allotment would lead to 0.85- and 1.25-V supply for three and five stacks, respectively). The supply voltages were chosen to maintain robust operation and consistent linearity, as discussed next.

Both the amplifiers exhibit a measured closed-loop mid-band gain of 36 dB with a bandwidth of 240 Hz. The measured frequency response of the five-stack amplifier is shown in Fig. 12. The CMRR and PSRR for both versions measured over multiple chips ($n = 10$) is greater than 95 and 68 dB, respectively. The input impedance of the five-stack amplifier was boosted from 9 to 93 MΩ, whereas the three-stack was

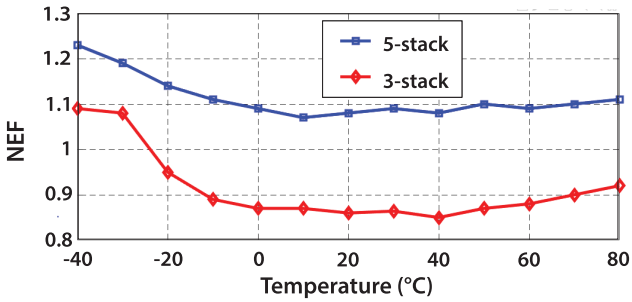

Fig. 15. Temperature sensitivity of the amplifier.

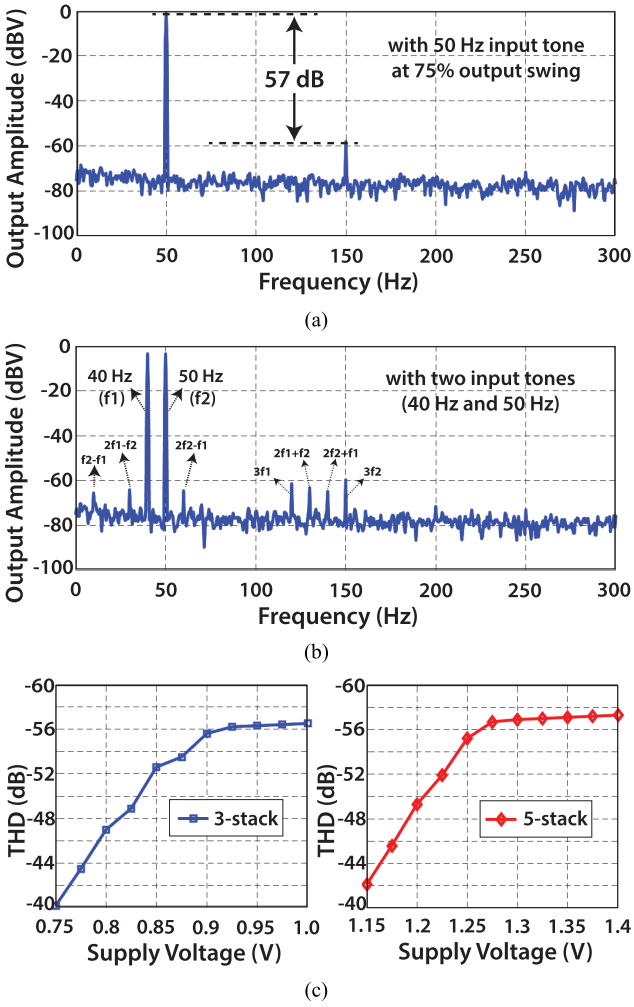

Fig. 16. Linearity of (a) single tone and (b) two tones. (c) Linearity versus supply voltage.

boosted to 87 MΩ. The benefits of the increased supply voltage for the DSL (with the same C_{DC} for both versions to provide more than ±50-mV offset cancellation) were also observed through measurement. The measured residual offset at the amplifiers' outputs normalized by the respective supplies versus the applied dc input is plotted in Fig. 13. Offsets of ±50 and ±70 mV can be tolerated by the three- and five-stack versions, respectively, without saturating the amplifier.

The measured input-referred noise PSDs are shown in Fig. 14. Both the amplifiers consume an ultra-low 13.9-nA current that would typically result in a white noise PSD

TABLE III
PERFORMANCE SUMMARY AND COMPARISON

	JSSC'17 [35]	JSSC'16 [1]	JSSC'15 [2]	JSSC'18 [24]	ISSCC'13 [34]	JSSC'17 [4]	This work	
							3-stack	5-stack
Application	ECG/EEG	ECG	ECG	–	EEG	EEG	ECG	
Technology	180 nm	65 nm	65 nm	180 nm	180 nm	40 nm	180 nm	
Supply (V)	0.2 / 0.8	0.6	0.6	1	0.45	1.2	0.95	1.35
Area (mm^2)	1	0.2	0.6	0.29	0.25	0.071	0.18	0.24
Power (nW)	790	1	16.8	250	730	2,000	13.2	18.7
Current (nA)	987	1.67	28	250	1,622	1,666	13.9	
Gain (dB)	58	32	51–96	25	52	26	36	
BW (Hz)	670	370	250	10,000	10,000	5,000	240	
CMRR (dB)	85	60	80	84	73	-	> 95	
PSRR (dB)	74	63	67	76	80	-	> 68	
THD (%)	0.3 (75% out)	-	2.8	-	0.53 (90% out)	0.02 (40 mV_p in)	0.19 (75% out)	0.16 (75% out)
Peak Ripple/V_{DD}	-	-	-	-	-	-100 dB	-81 dB	-85 dB
Input-Referred Noise (nV/√Hz)	36	1,400	253	43	29	40	194	158
NEF	2.1	2.1	2.64	1.07	1.57	4.9	1.08	**0.86**
PEF	1.6 / 1.8*	2.64	4.1	1.14	1.12	28	1.12	**0.99**
Blocks/features under comp.	LNA, chop PGA, AA-filt	LNA	LNA, chop DSL	LNA	LNA, VGA	LNA, DSL Chop, Imp Ripple-rej.	LNA, chopping, DSL, Imp-boost, Ripple-rej.	

* With DC-DC converter overhead

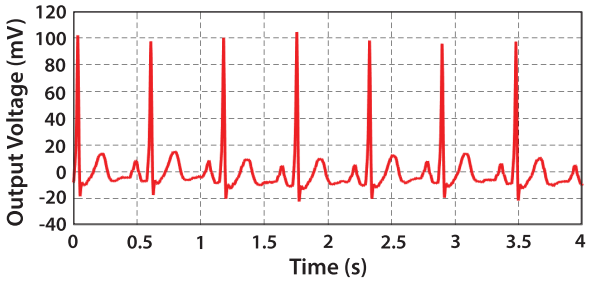

Fig. 17. Measured ECG from a human subject recorded from $N = 5$ amplifier.

of 350 nV/√Hz using a single-stack inverter-based OTA. The improvements with further stacking are clearly seen. The input-referred noise floor exhibited by the three-stack amplifier is ∼200 nV/√Hz, while that for the five-stack amplifier with further current reuse is lowered to ∼150 nV/√Hz. The corresponding measured NEF and PEF for the three-stack version are 1.08 and 1.12, respectively. These are improved to 0.86 and 0.99, respectively, for the five-stack version. To demonstrate robust operation over temperature, measurements of the NEF were taken from −40 to +80 °C. As evident from Fig. 15, the NEF for both amplifiers remains consistent over a −10 to +70 °C temperature range. This is readily acceptable for body implanted operation where the temperature sensitivity requirement is relaxed due to proximity to the human body.

The measured linearity for the five-stack version is shown in Fig. 16(a) and (b). With an output swing of 75% of the supply voltage, the amplifier has a measured total harmonic distortion (THD) of 0.16% (56.7-dB SFDR or 9-bit linearity), which suffices for ECG recording. Based on simulations, the linearity is limited by the 1.5-nA second stage rather than the DSL pseudoresistors. Fig. 16(b) shows the two-tone linearity measurements. The resultant intermodulation tones are as expected and have low amplitudes consistent with the linearity measured from the single-tone test. This implies that there is no unwanted crosstalk between the stacked OTAs that would otherwise have resulted in degraded and possibly additional intermodulation products. The amplifiers' linearity performance with supply variation is shown in Fig. 16(c), justifying selected supply voltage. For the five-stack amplifier, good linearity above 1.25 V is maintained, implying a robust operation at the chosen 1.35-V supply. For each of these measurements, the input amplitude of a 50-Hz tone is adjusted to maintain an output swing that is 75% of the supply voltage used.

The fabricated chip has also been used to perform ECG recordings from a human subject using a standard three-electrode setup with the third electrode grounded. A measured ECG waveform in Lead II electrode configuration is shown in Fig. 17.

The performance of the prototype amplifiers is summarized and compared with the existing state-of-the-art work in Table III. It should be noted that the PEF improvement is not as drastic compared to prior works as expected from the theory presented in Section II. This is because the prior state-of-the-art PEF was reported from amplifiers with power consumption in a microwatt range in which the reported power of peripheral circuits was minimal (*e.g.,* a few nanowatts is reported for biasing circuits in [34]). A substantial power is consumed in this article to ensure robust operation and meet application needs mentioned earlier. Nevertheless, the measured NEF and PEF compared to prior works from the five-stack version are the best reported, to the best of our knowledge, and significantly better ∼3× compared to nanowatt-level ultra-low-power amplifiers [1], [2].

VII. CONCLUSION

A novel technique for improving the power efficiency of a two-stage op-amp with chopping was presented. The benefits

were demonstrated for an amplifier intended for an implantable ECG application. The proposed OTA-stacking technique could also be extended for other applications, such as local field potential (LPF) or spike recording AFEs [33], [41], Wheatstone bridge sensors [44], and continuous-time ADCs such as [45] that require a capacitively coupled chopper-stabilized input stage. The proposed G_{m}-boosting resulting in lower noise also assists chopping due to the associated higher bandwidth to process the upmodulated signals and the high-pass filtering to minimize chopper ripple. The self-biased feedback mechanism helps maintain a good CMR. Compared to prior works, a two-stage implementation is feasible and output summations are realized passively without any power overhead. With the stacking of five OTAs, the best reported NEF of 0.86 and PEF of 0.99 are achieved from an amplifier consuming only 13.9-nA.

REFERENCES

[1] P. Harpe, H. Gao, R. van Dommele, E. Cantatore, and A. H. M. van Roermund, "A 0.20 mm^2 3 nW signal acquisition IC for miniature sensor nodes in 65 nm CMOS," *IEEE J. Solid-State Circuits*, vol. 51, no. 1, pp. 240–248, Jan. 2016.

[2] Y.-P. Chen *et al.*, "An injectable 64 nW ECG mixed-signal SoC in 65 nm for arrhythmia monitoring," *IEEE J. Solid-State Circuits*, vol. 50, no. 1, pp. 375–390, Jan. 2015.

[3] S. Mondal, C.-L. Hsu, R. Jafari, and D. Hall, "A dynamically reconfigurable ECG analog front-end with a 2.5× data-dependent power reduction," in *Proc. IEEE Custom Integr. Circuits Conf. (CICC)*, Apr./May 2017, pp. 1–4.

[4] H. Chandrakumar and D. Marković, "An 80-mVpp linear-input range, 1.6-GΩ input impedance, low-power chopper amplifier for closed-loop neural recording that is tolerant to 650-mVpp common-mode interference," *IEEE J. Solid-State Circuits*, vol. 52, no. 11, pp. 2811–2828, Nov. 2017.

[5] L. B. Leene and T. G. Constandinou, "A 0.006 mm^2 1.2 μW analog-to-time converter for asynchronous bio-sensors," *IEEE J. Solid-State Circuits*, vol. 53, no. 9, pp. 2604–2613, Sep. 2018.

[6] K. Kim *et al.*, "A 0.5V 9.26 μW 15.28 mΩ/vHz bio-impedance sensor IC with 0.55° overall phase error," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 2019, pp. 364–366.

[7] H. Jiang, X. Zhou, S. Kulkarni, M. Uranian, R. Seenivasan, and D. A. Hall, "A sub-1 μW multiparameter injectable BioMote for continuous alcohol monitoring," in *Proc. IEEE Custom Integr. Circuits Conf. (CICC)*, Apr. 2018, pp. 1–4.

[8] M. Maruyama, S. Taguchi, M. Yamanoue, and K. Iizuka, "An analog front-end for a multifunction sensor employing a weak-inversion biasing technique with 26 nVrms, 25 aCrms, and 19 fArms input-referred noise," *IEEE J. Solid-State Circuits*, vol. 51, no. 10, pp. 2252–2261, Oct. 2016.

[9] S. Jeong *et al.*, "A 12nW always-on acoustic sensing and object recognition microsystem using frequency-domain feature extraction and SVM classification," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 2017, pp. 362–363.

[10] H. Jiang, C. Huang, M. Chan, and D. A. Hall, "A 2-in-1 temperature and humidity sensor achieving 62 fJ·K^2 and 0.83 pJ·(%RH)^2," in *Proc. IEEE Custom Integr. Circuits Conf. (CICC)*, Austin, TX, USA, Apr. 2019, pp. 1–4.

[11] M. Gray *et al.*, "Implantable biosensors and their contribution to the future of precision medicine," *Vet. J.*, vol. 239, pp. 21–29, Sep. 2018.

[12] G. S. Wilson and R. Gifford, "Biosensors for real-time *in vivo* measurements," *Biosensors Bioelectron.*, vol. 20, no. 12, pp. 2388–2403, Jun. 2005.

[13] C. Zellerhoff, E. Himmrich, D. Nebeling, O. Przibille, B. Nowak, and A. Liebrich, "How can we identify the best implantation site for an ECG event recorder?" *Pacing Clin. Electrophysiol.*, vol. 23, no. 10, pp. 1545–1549, Oct. 2000.

[14] J. Riistama and J. Lekkala, "Characteristic properties of implantable Ag/AgCl- and Pt-electrodes," in *Proc. 26th Annu. Int. Conf. IEEE Eng. Med. Biol. Soc.*, vol. 1, Sep. 2004, pp. 2360–2363.

[15] J. G. Webster, "Reducing motion artifacts and interference in biopotential recording," *IEEE Trans. Biomed. Eng.*, vol. BME-31, no. 12, pp. 823–826, Dec. 1984.

[16] Cymbet. *EnerChipTM Solid State Batteries*. Accessed: Aug. 10, 2019. [Online]. Available: https://www.cymbet.com/products/enerchip-solid-state-batteries/

[17] M. Wahbah, M. Alhawari, B. Mohammad, H. Saleh, and M. Ismail, "Characterization of human body-based thermal and vibration energy harvesting for wearable devices," *IEEE J. Emerg. Sel. Topics Circuits Syst.*, vol. 4, no. 3, pp. 354–363, Sep. 2014.

[18] R. F. Yazicioglu, P. Merken, R. Puers, and C. Van Hoof, "A 60 μW 60 nV$\sqrt{Hz}$ readout front-end for portable biopotential acquisition systems," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 2006, pp. 109–118.

[19] X. Zou, X. Xu, L. Yao, and Y. Lian, "A 1-V 450-nW fully integrated programmable biomedical sensor interface chip," *IEEE J. Solid-State Circuits*, vol. 44, no. 4, pp. 1067–1077, Apr. 2009.

[20] R. F. Yazicioglu, S. Kim, T. Torfs, H. Kim, and C. Van Hoof, "A 30 μW analog signal processor ASIC for portable biopotential signal monitoring," *IEEE J. Solid-State Circuits*, vol. 46, no. 1, pp. 209–223, Jan. 2011.

[21] S. Mondal and D. A. Hall, "An ECG chopper amplifier achieving 0.92 NEF and 0.85 PEF with AC-coupled inverter-stacking for noise efficiency enhancement," in *Proc. IEEE Int. Symp. Circuits Syst. (ISCAS)*, May 2017, pp. 1–4.

[22] Y.-P. Chen, D. Blaauw, and D. Sylvester, "A 266 nW multi-chopper amplifier with 1.38 noise efficiency factor for neural signal recording," in *Symp. VLSI Circuits Dig. Tech. Papers*, Jun. 2014, pp. 1–2.

[23] M. Steiner and N. Greer, "A 22.3b 1kHz 12.7 mW switched-capacitor ΔΣ modulator with stacked split-steering amplifiers," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Jan./Feb. 2016, pp. 284–286.

[24] L. Shen, N. Lu, and N. Sun, "A 1-V 0.25-μW inverter stacking amplifier with 1.07 noise efficiency factor," *IEEE J. Solid-State Circuits*, vol. 53, no. 3, pp. 896–905, Mar. 2018.

[25] G. Cecchin and F. H. Hilbert, "Stacked differential amplifiers," U.S. Patent 3,603,894 A, Sep. 7, 1971.

[26] B. Johnson and A. Molnar, "An orthogonal current-reuse amplifier for multi-channel sensing," *IEEE J. Solid-State Circuits*, vol. 48, no. 6, pp. 1487–1496, Jun. 2013.

[27] M. S. J. Steyaert and W. M. C. Sansen, "A micropower low-noise monolithic instrumentation amplifier for medical purposes," *IEEE J. Solid-State Circuits*, vol. SSC-22, no. 6, pp. 1163–1168, Dec. 1987.

[28] R. R. Harrison, "A low-power, low-noise CMOS amplifier for neural recording applications," in *Proc. IEEE Int. Symp. Circuits Syst.*, vol. 5, May 2002, p. 5.

[29] W. Wattanapanitch, M. Fee, and R. Sarpeshkar, "An energy-efficient micropower neural recording amplifier," *IEEE Trans. Biomed. Circuits Syst.*, vol. 1, no. 2, pp. 136–147, Jun. 2007.

[30] M. Bazes, "Two novel fully complementary self-biased CMOS differential amplifiers," *IEEE J. Solid-State Circuits*, vol. 26, no. 2, pp. 165–168, Feb. 1991.

[31] M. S. Chae, Z. Yang, M. R. Yuce, L. Hoang, and W. Liu, "A 128-channel 6 mW wireless neural recording IC with spike feature extraction and UWB transmitter," *IEEE Trans. Neural Syst. Rehabil. Eng.*, vol. 17, no. 4, pp. 312–321, Aug. 2009.

[32] S. Iguchi, T. Sakurai, and M. Takamiya, "A low-power CMOS crystal oscillator using a stacked-amplifier architecture," *IEEE J. Solid-State Circuits*, vol. 52, no. 11, pp. 3006–3017, Nov. 2017.

[33] R. Müller, S. Gambini, and J. M. Rabaey, "A 0.013mm^2, 5 μW, DC-coupled neural signal acquisition IC with 0.5 V supply," *IEEE J. Solid-State Circuits*, vol. 47, no. 1, pp. 232–243, Jan. 2012.

[34] D. Han, Y. Zheng, R. Rajkumar, G. S. Dawe, and M. Je, "A 0.45 V 100-channel neural-recording IC with sub-μW/channel consumption in 0.18 μm CMOS," *IEEE Trans. Biomed. Circuits Syst.*, vol. 7, no. 6, pp. 735–746, Dec. 2013.

[35] F. M. Yaul and A. P. Chandrakasan, "A noise-efficient 36 nV$\sqrt{Hz}$ chopper amplifier using an inverter-based 0.2-V supply input stage," *IEEE J. Solid-State Circuits*, vol. 52, no. 11, pp. 3032–3042, Nov. 2017.

[36] V. Majidzadeh, A. Schmid, and Y. Leblebici, "Energy efficient low-noise neural recording amplifier with enhanced noise efficiency factor," *IEEE Trans. Biomed. Circuits Syst.*, vol. 5, no. 3, pp. 262–271, Jun. 2011.

[37] K. K. Hung, P. K. Ko, C. Hu, and Y. C. Cheng, "A unified model for the flicker noise in metal-oxide-semiconductor field-effect transistors," *IEEE Trans. Electron Devices*, vol. 37, no. 3, pp. 654–665, Mar. 1990.
[38] J. Holleman, "Design considerations for neural amplifiers," in *Proc. 38th Annu. Int. Conf. IEEE Eng. Med. Biol. Soc. (EMBC)*, Aug. 2016, pp. 6331–6334.
[39] R. Arzbaecher, D. Hampton, M. C. Burke, and M. C. Garrett, "Subcutaneous ECG monitors and their field of view," *J. Electrocardiol.*, vol. 43, no. 6, pp. 601–605, 2010.
[40] S. A. Desai, J. D. Rolston, L. Guo, and S. M. Potter, "Improving impedance of implantable microwire multi-electrode arrays by ultrasonic electroplating of durable platinum black," *Frontiers Neuroeng.*, vol. 3, p. 5, May 2010.
[41] T. Denison, K. Consoer, W. Santa, A.-T. Avestruz, J. Cooley, and A. Kelly, "A 2 μW 100 nV$\sqrt{Hz}$ chopper-stabilized instrumentation amplifier for chronic measurement of neural field potentials," *IEEE J. Solid-State Circuits*, vol. 42, no. 12, pp. 2934–2945, Dec. 2007.
[42] Q. Fan, F. Sebastiano, J. H. Huijsing, and K. A. A. Makinwa, "A 1.8 μW 60 nV$\sqrt{Hz}$ capacitively-coupled chopper instrumentation amplifier in 65 nm CMOS for wireless sensor nodes," *IEEE J. Solid-State Circuits*, vol. 46, no. 7, pp. 1534–1543, Jul. 2011.
[43] J. Yoo, L. Yan, D. El-Damak, M. A. B. Altaf, A. H. Shoeb, and A. P. Chandrakasan, "An 8-channel scalable EEG acquisition SoC with patient-specific seizure classification and recording processor," *IEEE J. Solid-State Circuits*, vol. 48, no. 1, pp. 214–228, Jan. 2013.
[44] H. Jiang, K. A. A. Makinwa, and S. Nihtianov, "An energy-efficient 3.7nV$\sqrt{Hz}$ bridge-readout IC with a stable bridge offset compensation scheme," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 2017, pp. 172–173.
[45] H. Chandrakumar and D. Markovic, "A 15.2-ENOB continuous-time $\Delta\Sigma$ ADC for a 7.3μW 200mV$_{pp}$-linear-input-range neural recording front-end," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 2018, pp. 232–234.

Somok Mondal (S'16) received the B.Tech. (Hons.) and M.Tech degrees in electronics and electrical communication engineering from IIT Kharagpur, Kharagpur, India, in 2013. He is currently pursuing the Ph.D. degree in electrical engineering with the University of California at San Diego, La Jolla, CA, USA.

His current research interests include low-power analog and RF integrated circuit design for Internet-of-Things (IoT) and biomedical applications.

Drew A. Hall (S'07–M'12–SM'19) received the B.S. degree (Hons.) in computer engineering from the University of Nevada, Las Vegas, NV, USA, in 2005, and the M.S. and Ph.D. degrees in electrical engineering from Stanford University, Stanford, CA, USA, in 2008 and 2012, respectively.

From 2011 to 2013, he worked as a Research Scientist at the Integrated Biosensors Laboratory, Intel Corporation, Santa Clara, CA, USA. Since 2013, he has been with the University of California at San Diego, La Jolla, CA, USA, where he is currently an Associate Professor with the Department of Electrical and Computer Engineering and an Affiliate Professor of bioengineering. His research interests include bioelectronics, biosensors, analog circuit design, medical electronics, and sensor interfaces.

Dr. Hall is also a fellow of Tau Beta Pi. He was a co-recipient of the First Place in the inaugural international IEEE Change the World Competition and the First Place in the BME-IDEA invention competition, both in 2009. He received the Analog Devices Outstanding Designer Award in 2011, the Undergraduate Teaching Award in 2014, the Hellman Fellowship Award in 2014, an NSF CAREER Award in 2015, the NIH Trailbalzer Award in 2019, and the Best Poster Award at Biomedical Circuits and Systems Conference (BioCAS) 2019.