A 0.4-V 0.93-nW/kHz Relaxation Oscillator Exploiting Comparator Temperature-Dependent Delay to Achieve 94-ppm/°C Stability

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***Abstract*— This paper presents the analysis and design of a relaxation oscillator that counteracts the complementary-to-absolute-temperature (CTAT) property of the comparator delay with the proportional-to-absolute-temperature (PTAT) property of the *RC* core to realize temperature-stabilized operation. By using a feedback bias network to linearize the comparator CTAT delay, thus improving the overall temperature stability by 20×, this technique enables a comparator with ∼20× less bandwidth and an overall oscillator with ∼5× lower power than conventional approaches. In a 0.18-μm silicon on insulator CMOS process, this design consumes 1.14 nW from a 0.4-V supply operating at 1.22 kHz, with a temperature coefficient (TC) as low as 40 ppm/°C ($\mu = 94$ ppm/°C for $n = 5$) achieving state-of-the-art efficiency (0.93 nW/kHz) for kilohertz-range relaxation oscillators.**

***Index Terms*— Internet-of-things (IoT), low power, low voltage, relaxation oscillator, temperature coefficient (TC).**

I. Introduction

DISTRIBUTED internet-of-things (IoT) nodes, such as unattended sensors and smart home appliances, are required to operate for long periods of time (e.g., years) from low-volume batteries or energy harvesters [1], [2]. Oscillators are a core block in all IoT nodes used for timers, clocking, and network synchronization. Due to dynamic power limitations and low throughput needs, clock frequencies on the order of a few kilohertz are used in many such applications. Since these oscillators are always on, they must be very low power (e.g., ∼nW), compatible with low supply voltages commonly used in IoT nodes (e.g., 0.4 V), and temperature stable to support accurate clocking (i.e., <±500 ppm for the sleep timer of a Bluetooth Low Energy link [1]). Comparator-based relaxation oscillators are a commonly used architecture to generate such kilohertz-range clocks because of their high power efficiency [1], [3].

The operation of a comparator-based relaxation oscillator is illustrated in Fig. 1(a). A bias resistor, R, in conjunction with a beta-multiplier is used to set a reference current, I_{ref}, and a reference voltage, V_{ref} ($= RI_{\text{ref}}$). An integration capacitor, C_{int}, is charged by a mirrored version of I_{ref}, and repeatedly reset by a continuous-time comparator after crossing V_{ref}, as shown in Fig. 1(b). Thus, the oscillation period, T_{OSC}, is

$$T_{\text{OSC}} = \tau_{\text{RC}} + \tau_{\text{comp}} + \tau_{\text{buf}} + \tau_{\text{rst}} \tag{1}$$

where τ_{RC} is the time constant formed by R and C_{int}, τ_{comp} is the comparator delay defined as the time taken to assert the comparator output once V_{int} exceeds V_{ref}, τ_{buf} is the digital buffer delay, and τ_{rst} is the reset time that includes discharging the capacitor and resetting the comparator, buffer, and switch. Note that resetting the comparator, as will be discussed more in Section III-C, is much faster than τ_{comp}. Since the TC of τ_{RC} can be accurately controlled (e.g., TC ≈ 0) using two trimmed resistors to counteract the TCs of each other [4], [5], and both τ_{buf} and τ_{rst} are often negligible for kilohertz-range oscillators, τ_{comp}, which depends on temperature, becomes significant in the overall temperature stability. Most prior works strived to minimize τ_{comp} by increasing the bandwidth, and therefore the comparator power, to make τ_{comp} a small fraction of the oscillation period (e.g., $\tau_{\text{comp}}/T_{\text{OSC}} < 0.4\%$ in [6]). Other techniques, including feed-forward comparator delay cancellation [4], integrated error feedback [5], and a duty-cycled high-bandwidth comparator [7], have also been used to break this tradeoff. However, they require either redundant comparators or complex digital control logic.

This paper begins by deriving equations for the comparator delay considering the ramp-shaped integration voltage at the comparator input. Based on the analysis, a relaxation oscillator with a two-stage comparator [common gate (CG) stage + common source (CS) stage] is proposed that intentionally utilizes a

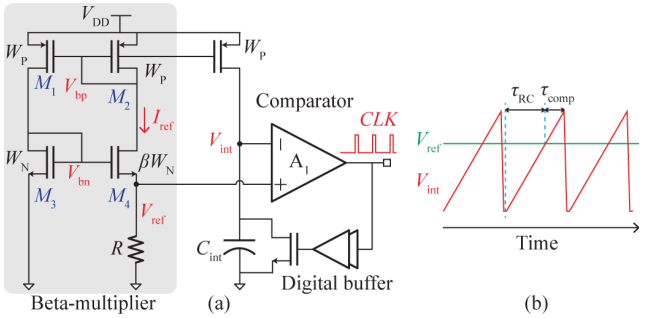

Fig. 1. (a) Schematic of a typical comparator-based relaxation oscillator. (b) Illustration of delay components, where τ_{buf} and τ_{rst} are too trivial to show.

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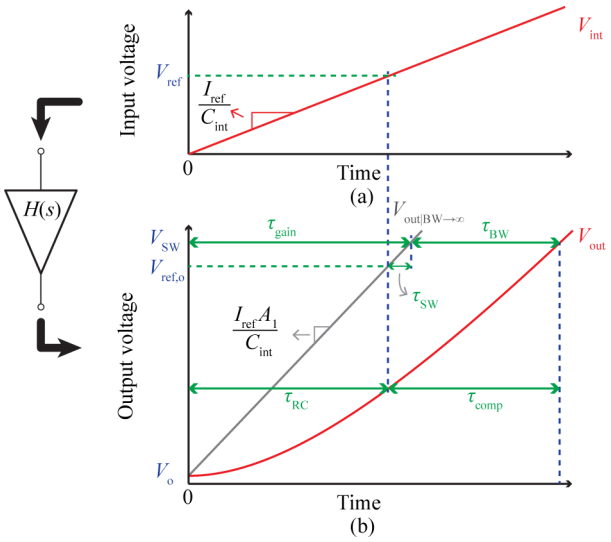

Fig. 2. Model of the comparator delay following an integrator and driving a buffer. Waveforms at (a) input and (b) output.

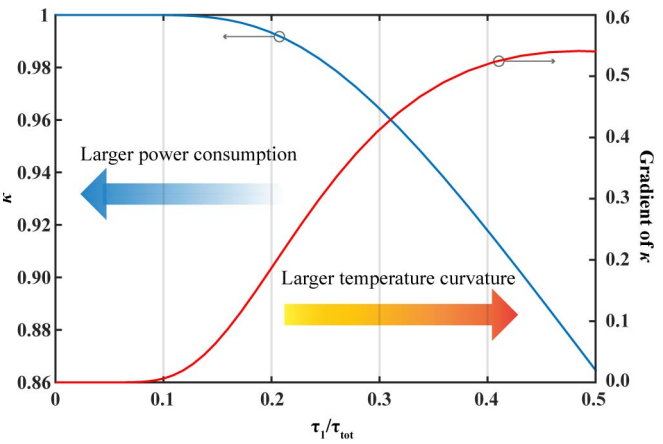

Fig. 3. Numerical solutions for κ versus τ_1/τ_{tot}.

proportional-to-absolute-temperature (PTAT) *RC* core, whose delay is counteracted via the linearized complementary-to-absolute-temperature (CTAT) delay of the proposed comparator. Since the comparator delay no longer must be small relative to the clock period, its bandwidth, and therefore power, can be reduced while maintaining temperature stability. The proposed technique has been verified through analysis (Section II), simulations (Section III), and measurement results (Section IV).

II. Comparator Delay Analysis

A. Comparator Delay Model

The comparator input voltage, V_{int}, is a ramp that can be written as

$$V_{int}(t) = \frac{I_{ref}}{C_{int}} \cdot t \cdot u(t) \tag{2}$$

where $u(t)$ is the unit step function, as shown in Fig. 2(a). The transfer function of the comparator, assuming a single-stage linear, time-invariant continuous-time system, can be written as

$$H(s) = \frac{A_1}{1 + s\tau_1} \tag{3}$$

where A_1 and τ_1 are the dc gain and time constant of the comparator, respectively. By converting (2) into the s-domain and multiplying by (3), the output behavior of the comparator can be expressed as

$$\Delta V_{out}(s) = \frac{I_{ref}}{sC_{int}} H(s) \tag{4}$$

where ΔV_{out} is the change in the output voltage. This is graphically illustrated in Fig. 2(b) along with an additional curve corresponding to a comparator with infinite bandwidth ($V_{out|BW\to\infty}$) for comparison. Note that both curves start at a voltage V_o and increase until triggering the buffer and resetting the ramp by reaching V_{SW}, which is defined as the switching threshold of the subsequent buffer. Since all of the time constants are annotated on the output waveform [Fig. 2(b)], V_{ref} is also referred to the output as $V_{ref,o}$ for convenience, where $V_{ref,o}$ is defined as the voltage that the comparator with infinite bandwidth reaches when the inputs are equal (i.e., $V_{int} = V_{ref}$). The time constants τ_{RC} and τ_{comp} are annotated in Fig. 2(b) based on the definitions provided in Section I, namely, that τ_{RC} ends when V_{int} crosses V_{ref} and τ_{comp} starts immediately afterward and ends when V_{out} crosses V_{SW}.

The infinite bandwidth comparator curve allows one to decouple the effect of finite gain and finite bandwidth, as shown in Fig. 2(b), where τ_{gain} is the time taken for $V_{out|BW\to\infty}$ to cross V_{SW} and τ_{BW} is the remaining time that V_{out} takes to cross V_{SW}. The sum of τ_{gain} and τ_{BW} is the total delay, τ_{tot}, which is the time V_{out} takes to increase from V_o to V_{SW}. Note that $\tau_{tot} \approx T_{OSC}$ [based on (1), just excluding τ_{buf} and τ_{rst}]. By substituting $V_{SW} - V_o$ for ΔV_{out} in (4), and taking the inverse Laplace transform, one can derive τ_{tot}, and, more importantly τ_{BW}, as

$$\tau_{tot} = \underbrace{\frac{C_{int}(V_{SW} - V_o)}{I_{ref}A_1}}_{\tau_{gain}} + \underbrace{\underbrace{1 - e^{-\frac{\tau_{tot}}{\tau_1}}}_{\kappa}\tau_1}_{\tau_{BW}} \tag{5}$$

where κ is a scaling factor bounded between 0 and 1 as shown in Fig. 3. Finally, with $\tau_{BW} = \kappa\tau_1$ from (5), τ_{comp} can be written as

$$\tau_{comp} = \tau_{BW} + \underbrace{(V_{SW} - V_{ref,o})\frac{C_{int}}{I_{ref}A_1}}_{\tau_{SW}} = \kappa\tau_1 + \tau_{SW} \tag{6}$$

where τ_{SW} is the additional time that V_{out} takes to reach V_{SW} even with an infinite bandwidth comparator. Note that in practice, $V_{ref,o} - V_{SW}$ can be either positive or negative. It is also worth pointing out that the underlying assumption of a linear, time-invariant system may not hold for all implementations, especially, considering the large input swing; however, to accurately calculate τ_{SW}, A_1 only needs to be constant over a small range, $V_{SW} - V_{ref,o}$, which is easily achieved in practice. This is the motivation for deriving τ_{comp} with respect to τ_{SW} instead of τ_{gain}, which would require A_1 to be linear over the entire range.

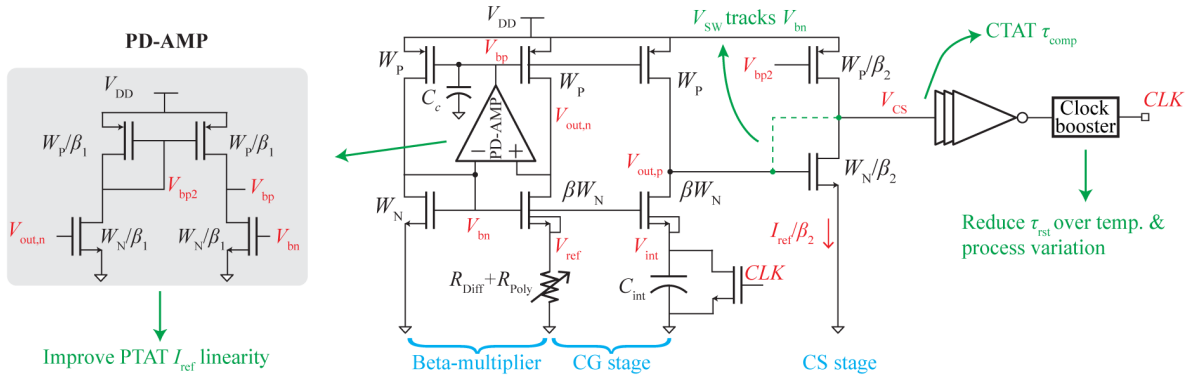

Fig. 4. Schematic of proposed relaxation oscillator employing a two-stage comparator along with PD-AMP in feedback to improve PTAT current temperature linearity.

The key takeaway from this analysis is that the comparator delay consists of two terms: one relating to the finite bandwidth ($\tau_{BW} = \kappa\tau_1$) and another dependent on the following buffer stage switching threshold (τ_{SW}). Rather than trying to minimize τ_{BW} to lessen its effect on the oscillator's temperature stability, which would require burning additional power, we propose to compensate it, along with τ_{SW}, instead. Section II-B analyzes the temperature dependence of (6), and Section III demonstrates a method to compensate (6) by linearizing $\kappa\tau_1$ with a PTAT current while canceling τ_{SW} with a two-stage comparator.

B. Temperature Dependence of the Comparator Delay

To analyze the temperature dependence of τ_{comp}, the TC of $\kappa\tau_1$ and τ_{SW} are examined separately to isolate their individual contributions. Assuming operation in subthreshold saturation and neglecting channel length modulation, the current generated by the beta-multiplier in Fig. 1 is

$$I_{ref} = \frac{\ln(\beta) n k_B T}{q R} \tag{7}$$

where k_B is Boltzmann's constant, n is the subthreshold slope factor ($\approx$1.5 in this process), q is the elementary charge, β is the size ratio between M_4 and M_3, and T is the temperature. Thus, (7) is a linear PTAT current. For a comparator biased with I_{ref}, τ_1 is

$$\tau_1 = r_o C_o = \frac{V_A C_o}{I_{ref}} \tag{8}$$

where V_A is the early voltage, which has minimal temperature dependence [3], r_o is the output resistance, and C_o is the load capacitance. Simulation shows that C_o, which consists of C_{db} of the transistor and the gate capacitance of the next stage, changes by only 2.2% over the -20 to 70 °C range. By substituting (7) into (8) and taking the partial derivative around room temperature ($T_0 = 300$ K), τ_1 has a CTAT dependence with a first-order TC of

$$\alpha_{\tau 1} = -\frac{1}{T_0}. \tag{9}$$

Since κ, as shown in Fig. 3, is dependent on τ_1, it also changes with temperature. If τ_1 is large, κ is PTAT and when multiplied by the CTAT τ_1 results in a negative second-order TC. Since κ becomes increasingly sensitive to τ_1 as τ_1 increases [Fig. 3 (red curve)], the second-order TC of $\kappa\tau_1$ also becomes significant. Thus, this imposes a design tradeoff where decreasing τ_1 requires a more power-hungry comparator while increasing τ_1 relaxes the comparator bandwidth requirement but leads to larger temperature curvature. By designing τ_1/τ_{tot} to be small, κ approaches unity while the gradient of κ with respect to τ_1 approaches zero. Thus, κ can be approximated as a constant that does not affect the temperature dependence. In summary, $\kappa\tau_1$ exhibits a CTAT dependence with slightly larger than the first-order curvature that, to the first order, can be counteracted by designing a linear PTAT τ_{RC} by trimming R to be PTAT.

The TC of τ_{SW} depends on two factors: $C_{int}/I_{ref}A_1$ and $V_{SW} - V_{ref,o}$. It can be shown that the first term is

$$\frac{C_{int}}{I_{ref}A_1} = \frac{C_{int}}{I_{ref}g_m r_o} = \frac{C_{int}}{\ln(\beta)V_A} R \tag{10}$$

where g_m is the transconductance. Thus, (10) has the same temperature dependence as R. Since V_{SW} and $V_{ref,o}$ are determined by the circuit implementation, they are discussed later in Section III. However, the trick is that if the circuit is designed to have V_{SW} track $V_{ref,o}$, then τ_{SW} is zero and the temperature dependence does not matter, as shown in (6). In summary, this analysis shows a technique to design a relaxation oscillator by leveraging the CTAT dependence of $\kappa\tau_1$ while canceling τ_{SW}, which deviates from conventional approaches that minimize the entire τ_{comp}/T_{OSC} by making the comparator have higher bandwidth.

III. Relaxation Oscillator Circuit Design

A 1.2-kHz relaxation oscillator has been designed employing a power efficient comparator with a linear temperature-dependent delay from -20 to 70 °C using the previously-described analysis.

A. High Linearity PTAT Reference Generator

The beta-multiplier circuit shown in Fig. 1 is commonly used to generate a PTAT current. To ensure proper operation, each transistor must be in subthreshold saturation

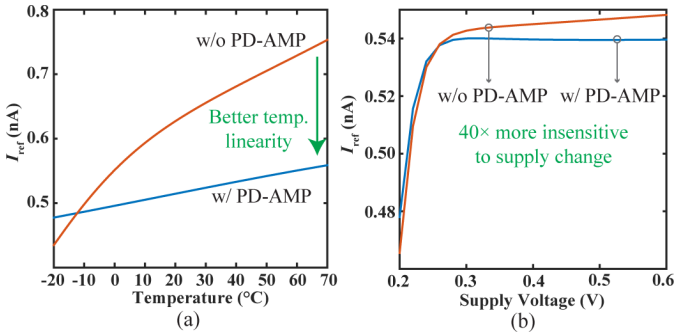

Fig. 5. Simulation results showing (a) reference current versus temperature and (b) reference current versus supply voltage.

($V_{DSAT} > 4V_T$). Changes in the transistor threshold voltage, V_t, due to temperature and process variation also imposes a limitation on the minimum supply voltage, $V_{DD,min}$. It can be shown that

$$\begin{aligned} V_{DD,min} &= V_{DSAT,M2} + V_{DSAT,M4} + \ln(\beta)V_T + \Delta V_{bp} \\ &= [8 + \ln(\beta)]V_T + \frac{\partial V_{bp}}{\partial T}\Delta T + \frac{\partial V_{bp}}{\partial V_{t,P}}\Delta V_{t,P} \end{aligned} \quad (11)$$

where ΔV_{bp} is the change in the drain voltage due to both temperature and process variation, and $\Delta V_{t,P}$ is the change in threshold voltage due to process variation. Thus, a smaller β factor leads to lower $V_{DD,min}$ where we choose $\beta = 2$, resulting in $R = 47$ MΩ and $I_{ref} = 0.54$ nA at room temperature. Compared to $\beta = 3$ or 4, this saves 17.5 and 30 mV voltage headroom at 70 °C, respectively, but more importantly, a smaller β also leads to a lower R and thus a smaller area.

The sensitivity of V_{bp} due to temperature and threshold voltage change can be derived from

$$V_{bp} = V_{DD} - nV_T \ln\left[\frac{\ln(\beta)n}{(n-1)RK_P V_T}\right] - |V_{t,P}| \quad (12)$$

where K_P is the PMOS transistor transconductance parameter inclusive of the sizing. The first-order temperature dependence of V_{bp} is

$$\frac{\partial V_{bp}}{\partial T} \approx -\frac{nk_B}{q} + \frac{\partial |V_{t,P}|}{\partial T} = -0.99 \text{ mV/°C}, \quad (13)$$

which matches with simulation results (−1.02 mV/°C). Since the total temperature range is 90 °C, the drift in V_{bp} due to the temperature change is 92 mV [i.e., the second term in (11)]. Furthermore, V_{bp} changes directly proportional with the threshold voltage deviation due to process variation [i.e., $\partial V_{bp}/\partial V_{t,P} = 1$ in (11) accounting for another 45 mV (simulation shows $\Delta V_{t,P}$ is 45 mV)]. Adding all of these numbers together, the minimum supply voltage should be >363 mV to ensure proper operation. Therefore, we choose a 0.4-V supply. All transistors were carefully sized to ensure M_1 and M_4 are in saturation at the highest temperature (worst case) and Monte Carlo simulations were conducted to check the circuit operation across process variation.

Without compensation, I_{ref} does not achieve as good of temperature linearity as indicated by (7) due to channel length modulation and drain-induced barrier lowering. Consequently, this non-linear PTAT current would ruin the linearity of the CTAT comparator delay, thereby degrading the temperature stability. To remedy this, a pseudo-differential amplifier (PD-AMP) that forces the PMOS transistors to have the same V_{DS} was inserted into the bias circuit (Fig. 4). As illustrated in Fig. 5(a), the linearity of I_{ref} is improved by 25× from −20 to 70 °C in simulation. The feedback also improves the I_{ref} sensitivity to changes in the supply voltage (i.e., power supply rejection ratio), as the change modulates V_{DS} of each transistor, and therefore the current. Simulation shows I_{ref} variation reduces from 1% to 0.025% for supply voltages from 0.3 to 0.6 V [Fig. 5(b)]. The PD-AMP is implemented by scaling the original bias circuit by a factor of β_1 to ensure the transistors in PD-AMP have the same headroom as the rest of the bias circuit. Since temperature drift is generally slow, the bandwidth requirement for the PD-AMP is greatly relaxed. Thus, we choose $\beta_1 = 3$ to reduce the power overhead.

B. Two-Stage τ_{SW}-Canceling Comparator

The first stage of the comparator is a CG amplifier that reuses part of the reference circuit. This stage does not add any power and, as such, has been widely used [3], [8], [9]; however, it suffers from long and temperature-sensitive delay, especially when the bias current is low. Rather than burning additional power to minimize the comparator delay, the technique described in Section II is applied. Since the R-branch and the C-branch are matched, $V_{out,n} = V_{out,p}$ when $V_{int} = V_{ref}$ assuming infinite bandwidth. Therefore, $V_{out,n}$ maps to $V_{ref,o}$ in the model in Section II and V_{SW} is calculated by shorting the input and output of the buffer stage [10]. If the CG stage feeds into the inverter chain directly, then V_{SW} is the voltage when the inverter input and output is connected. Assuming n is the same for both PMOS and NMOS transistors, the switching point of the inverter is

$$V_{SW,inv} \approx \frac{1}{2}\left[V_{DD} - nV_T \ln\left(\frac{K_N}{K_P}\right) - |V_{t,P}| + V_{t,N}\right]. \quad (14)$$

Using the same method as in (13), it can be shown that $V_{out,n}$ ($\approx V_{bn}$) only depends on the threshold voltage of the NMOS transistor, which has a CTAT temperature dependence. Thus, $V_{SW,inv}$ will not track $V_{out,n}$, and $V_{SW,inv} - V_{out,n}$ is PTAT due to $-|V_{t,P}|$ term in (14). Simulations show that $V_{SW,inv} - V_{out,n}$ have a strong PTAT temperature dependence (6500 ppm/°C). When setting R to be PTAT, τ_{SW} exhibits a significant positive second-order TC due to the cross multiplying between two PTAT terms with large TCs according to (6) and (10). Although $\kappa\tau_1$ can be designed to be CTAT to counteract the PTAT RC core, therefore, minimizing the first-order TC of T_{OSC}, it is the curvature over temperature that cannot be easily compensated. For example, when designing $\kappa\tau_1/T_{OSC} = 22\%$, the strong second-order TC of τ_{comp} is only scaled by ~22% when adding into T_{OSC}, and consequently the oscillator can achieve, at best, a temperature stability of ~28 800 ppm (the second-order TC is 12.5 ppm/°C^2) over the 90 °C range. This simulation is conducted using an ideal resistor with a first-order TC; as such, the non-linearity

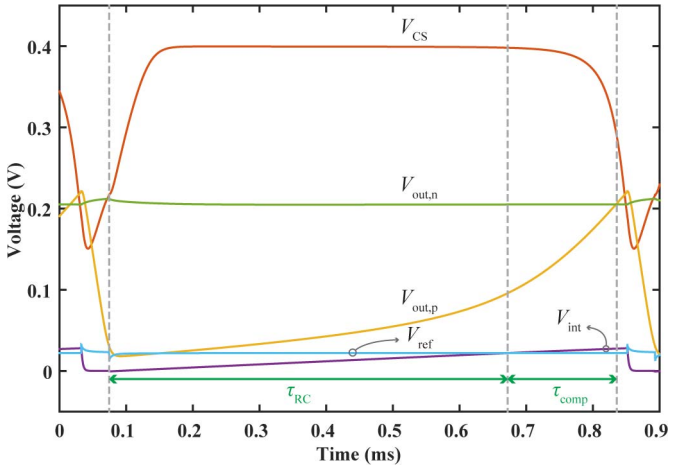

Fig. 6. Simulated waveforms for one oscillation cycle.

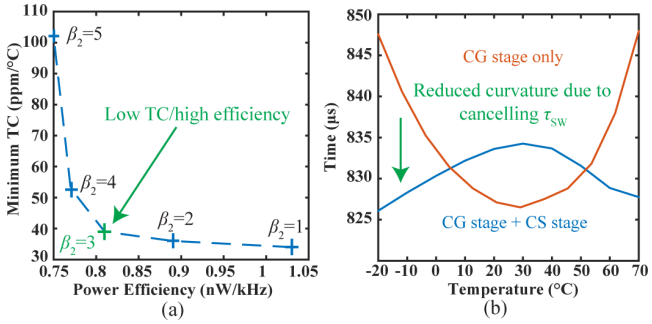

Fig. 7. Simulation results showing (a) TC versus power efficiency for different sizing ratios and (b) T_{OSC} versus temperature showing curvature.

from the resistor is isolated while examining the comparator temperature dependence. This is why conventionally designs have added more current to minimize $\kappa\tau_1$, while using a near-zero TC resistor to mitigate the curvature of τ_{SW}. Unfortunately, this is not power efficient and the residue TC (both first- and second-order) of τ_{SW} limits the overall temperature stability. Furthermore, more current in the CG amplifier means sourcing more current in all three branches of the circuit, which is very inefficient.

To cancel τ_{SW}, a CS stage is added to the existing CG comparator (Fig. 4). As shown in Fig. 6, this CS stage is off during most of a cycle since $V_{out,p}$ is low. It does not turn on until $V_{out,p}$ approaches $V_{out,n}$. Thus, it behaves more like a dynamic buffer rather than a continuous-time amplifier. The switching voltage, $V_{SW,CS}$, is approximately $V_{out,n}$, and as such $V_{SW,CS} - V_{out,n}$, and consequently τ_{SW} is canceled. Since V_{bn} tracks the NMOS V_t, τ_{sw} is zero. To ensure good matching, large devices were used and interdigitated in the layout. It should be noted that the PMOS in the CS stage can be biased by either V_{bp} or V_{bp2} from the PD-AMP, which is equal to V_{bp} assuming perfect matching. We used V_{bp2} for layout convenience. With a canceled τ_{SW}, biasing the CG comparator with I_{ref} results in well-controlled CTAT time constant and thus a CTAT τ_{comp}.

Like a current-starved inverter, the delay of the CS stage is inversely proportional to the bias current scale factor β_2. Through proper sizing, we chose $\beta_2 = 3$ to maintain low power while reducing the temperature stability degradation due

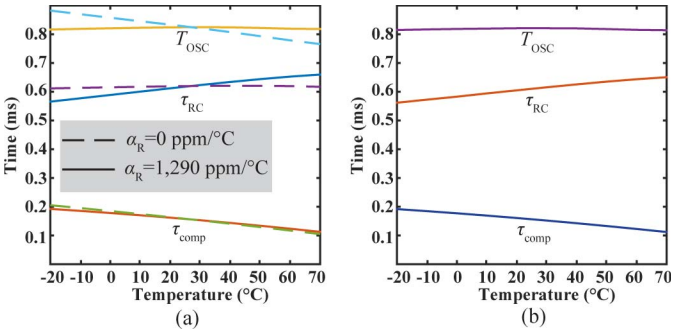

Fig. 8. Simulated delays with (a) ideal resistors and (b) actual RDAC.

to longer τ_{buf} and τ_{rst} [Fig. 7(a)]. As shown in Fig. 4, including the CS amplifier, the whole buffer chain has four stages to minimize the overall buffer propagation delay τ_{buf} (10 μs at room temperature) and sharpen the transition edges. The additional CS stage reduces the overall TC curvature by 8× in simulation due to the canceled τ_{SW} while still maintaining $\kappa\tau_1/T_{OSC} = \sim 22\%$ [Fig. 7(b)]. The simulation also shows that the second-order curvature flips after adding the CS stage, which is expected because canceling τ_{SW} removes the positive second-order TC of τ_{SW} and manifests the smaller negative second-order TC of $\kappa\tau_1$. A 50-point Monte Carlo simulation with process variation and mismatch showed that the TC varied from 33 to 121 ppm/°C over −20 to 70 °C after calibration—a significant improvement over the ∼2000 ppm/°C of the circuit in Fig. 1(a) for the same I_{ref}.

To illustrate the effectiveness of controlling τ_{comp}, two cases were simulated. As shown in Fig. 8(a), when R is set to a zero TC, τ_{RC} is constant while τ_{comp} is CTAT, and thus T_{OSC} is CTAT. When R is set to a positive TC, τ_{RC} becomes PTAT while τ_{comp} remains CTAT (but with a smaller TC), and the overall T_{OSC} is the temperature insensitive. The second-order TC of τ_{comp} degrades from −7.73 to −15.8 ppm/°C^2 after using the PTAT resistor. As a result, the second-order TC of T_{OSC} degrades from −1.76 to −4.27 ppm/°C^2 accordingly. This is as expected because the non-zero TC of the resistor modulates κ over temperature and creates a second-order nonlinearity. Note that C_{int} is ∼13 pF, which results in $\tau_{RC} \approx 610$ μs (74% of T_{osc}) at room temperature [Fig. 8(a)], $\tau_{comp} \approx 183$ μs (22% of T_{osc}), and the remaining 4% of T_{OSC} is made up of τ_{buf} and τ_{rst}, which have little impact on the overall temperature stability. In summary, the additional circuits (PD-AMP and CS stage) increase the power by 34% but improve the temperature stability by 50× compared to the original circuit for the same I_{ref}. Compared to the conventional approach of reducing $\tau_{comp}/T_{OSC} < 1\%$ with 20× larger I_{ref}, this technique saves ∼20× comparator power and ∼5× total power.

C. Bias Resistor DAC and Clock Booster

To compensate the CTAT comparator delay, the bias resistor must be trimmed, like other relaxation oscillators that are trimmed to yield zero-TC, though in this case to yield a PTAT *RC* core. All modern CMOS technologies have polysilicon resistors (always PTAT) and diffusion resistors (either PTAT or CTAT, depending on grain size and doping

concentration [11]), and thus modern processes support PTAT resistors with adjustable TC, α_R, via two series PTAT resistors with different TCs (e.g., α_{R1} and α_{R2}).

Based on (6), with a CG + CS comparator, the oscillation period is

$$T_{OSC} \approx C_{int} R_0 [1 + \alpha_R (T - T_0)] + \kappa \tau_1 \quad (15)$$

where R_0 is the resistance of R at room temperature and α_R is the compound TC of R. By substituting (7) and (8) into the first-order derivative of (15), an optimal α_R can be calculated as

$$\alpha_{R,opt} = \frac{V_A C_{CG}}{\ln(2) n V_{T0} C_{int} + V_A C_{CG}} \cdot \frac{1}{T_0} \quad (16)$$

where V_{T0} is the thermal voltage at T_0 and C_{CG} is the output capacitance of the CG stage. The $\alpha_{R,opt}$ was calculated to be ~1700 ppm/°C and simulated to be ~1290 ppm/°C. The difference comes from the κ variation and first-order TC from τ_{buf} and τ_{rst}. The nonlinear and time-variant behavior of the comparator also affects the accuracy of calculating $\alpha_{R,opt}$. To overcome process variation, the resistor is implemented as a resistor digital-to-analog converter (RDAC) via a series combination of 5-b PTAT and CTAT resistors. The frequency can also be tuned by adjusting both resistors and maintaining the ratio. The oscillator temperature stability was simulated again with the actual RDAC [Fig. 8(b)]. The second-order nonlinearity (3.99 ppm/°C^2) of T_{OSC} is almost the same as the case using an ideal resistor, demonstrating that the second-order TC of the resistor is not an issue in this design.

Since the R_{off}/R_{on} of a MOS switch is small at low supply voltages, a charge pump driven by this oscillator output generates a $-V_{DD}$ voltage to place the RDAC switches in super cutoff resulting in >50× larger R_{off}/R_{on} that would otherwise limit the operation range to ~50 °C. The discharge switch in parallel with C_{int} is driven by a modified clock booster [12] to minimize the discharge time and consequently τ_{rst} over PVT (Fig. 4). After the capacitor is discharged, the comparator flips and resets the buffer when $V_{out,p}$ drops below $V_{sw,CG}$. Thus, there exists a second comparator delay as a part of τ_{rst}. Fortunately, the second comparator delay is very short (8 μs, <1% of T_{OSC}), because first the comparator sees a step V_{int} this time, instead of a ramp, and second $V_{out,p}$ only needs to drop a small voltage range to offset the overshoot caused by τ_{buf}. Then, the buffer resets and turns off the switch. Simulation shows that τ_{rst} is less than 3% of T_{OSC} with the help of the clock booster.

IV. Measurement Results

The proposed oscillator was fabricated in a 0.18-μm silicon on insulator CMOS process with an active area of 0.2 mm^2 (Fig. 9). Operating at 0.4 V, the power consumption measured at room temperature was 1.14 nW, 70% of which was static power consumed by the reference generator and comparator, with no significant difference between chips ($n = 5$). The frequency of each chip was tuned to be ~1220 ± 15 Hz. Fig. 10(a) shows the measured frequency of the same oscillator

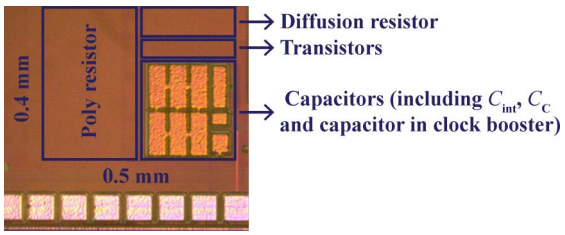

Fig. 9. Die photograph annotated with components.

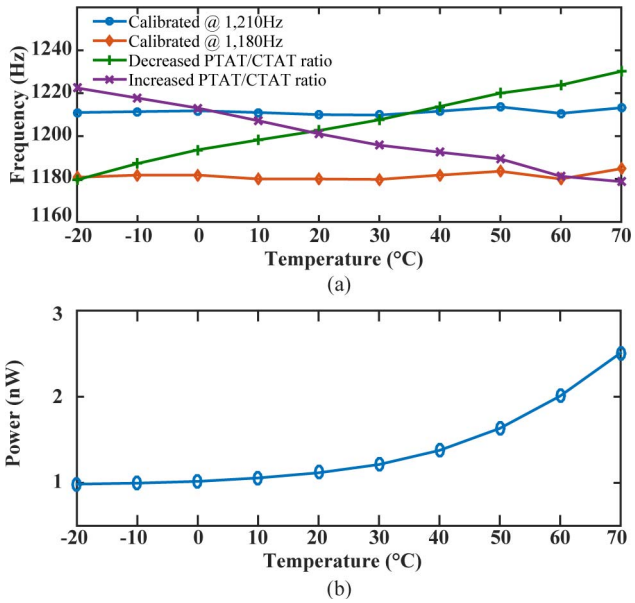

Fig. 10. Measured (a) temperature sensitivity before and after calibration and (b) power versus temperature.

with different RDAC configurations. The TC of the frequency becomes negative when increasing the PTAT/CTAT resistor ratio, and vice versa. By keeping the ratio fixed, the frequency can be tuned with a step size of ~30 Hz. The power when calibrated to 1210 Hz is plotted versus temperature in Fig. 10(b). After a two-point calibration, the measured TC varied from 40–155 ppm/°C ($n = 5$) over the −20 °C to 70 °C range [Fig. 11(a)]. Due to the process variation, each chip requires separate calibration but both the PTAT and CTAT RDAC configuration codes varied less than six LSBs across all five chips.

Fig. 11(b) shows the Allan deviation plot in an uncontrolled room-temperature environment. The total measurement duration was 300 s, which means each data point was obtained by >10× averaging. The short-term uncertainty (jitter) of a relaxation oscillator has been shown to be proportional to the comparator input-referred voltage noise at the switching moment [13]. Thus, the CG comparator with lower bias current inevitably has larger input-referred voltage noise, and therefore larger jitter. This explains why the short-term deviation (e.g., >200 ppm in 0.1 s) is larger than previous works. However, the jitter of such low-power oscillators is typically not an issue in IoT applications because it is used as timer or real-time clock in a wireless network. Thus, long-term stability (Allan deviation floor) is often used to evaluate the

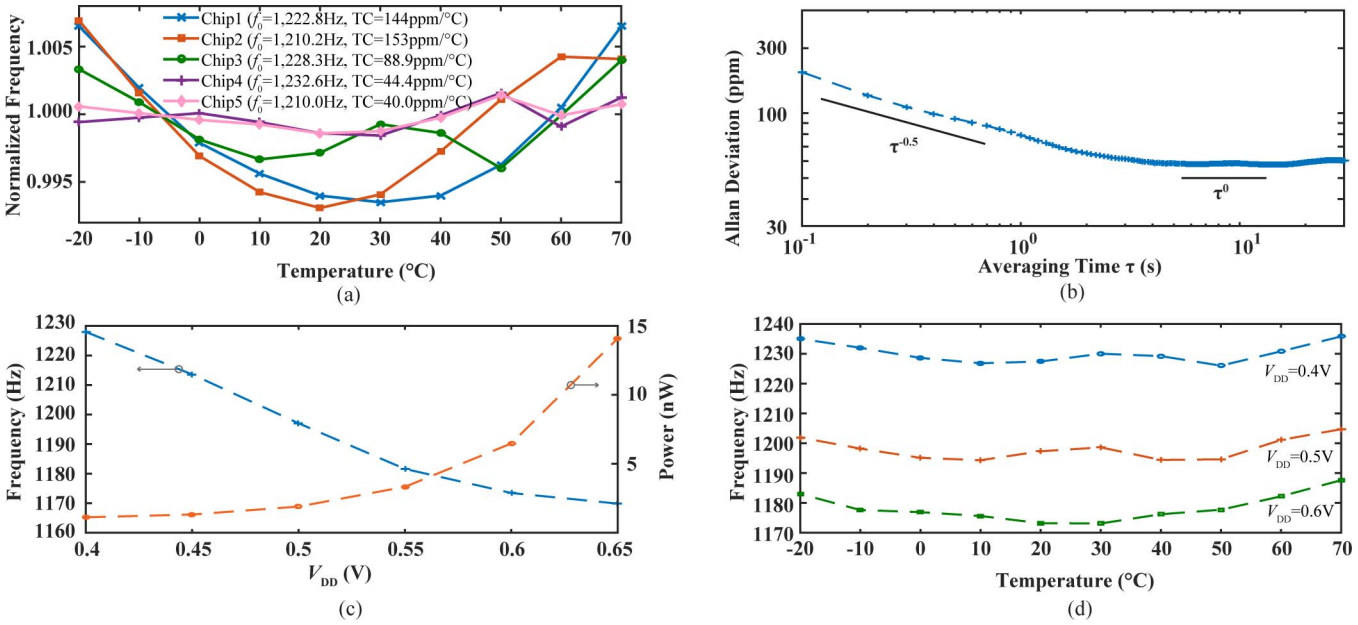

Fig. 11. Measured (a) temperature sensitivity of five chips, (b) Allan deviation, (c) frequency and power versus supply voltage, and (d) temperature sensitivity at different supply voltages.

TABLE I

PERFORMANCE COMPARISON OF LOW-POWER, KILOHERTZ RANGE INTEGRATED OSCILLATORS

Parameter	[3]	[4]	[6]	[8]	[9]	[15]	[16]	[17]	[18]	This Work
Technology (nm)	180	90	65	350	180	180	250	65	130	180
Frequency (kHz)	122	100	18.5	3.3	28	3	6.4	33	100	1.22
Supply (V)	0.6	0.8	1.0	1.0	1.2	0.85	0.8	1.2	1.1	0.4
Area (mm^2)	0.03	0.12	0.032	0.1	0.16	0.5	1.08	0.015	0.25	0.2
Allan Dev. Floor (ppm)	40	N/A	20	N/A	N/A	63	60	4	N/A	58
Temperature Range (°C)	-20 to 80	-40 to 90	-40 to 90	-20 to 80	-20 to 80	-25 to 85	-20 to 80	-40 to 90	20 to 40	-20 to 70
Calibration?	N/A	N/A	N/A	Multi-point	Yes	N/A	No	Yes	1-point	2-point
TC (ppm/°C)	327	105	38.5	<500	95.5	13.8	148	38.2	5	94
Power (nW)	14.4	280	120	11	40	4.7	75.6	190	150	1.14
Power Efficiency (nW/kHz)	0.12	2.8	6.49	4.0	1.43	1.57	11.8	5.86	1.5	0.93

noise performance. The oscillator required ~3 s to reach a 58-ppm floor, which is comparable to previous works.

The oscillation frequency generally does not change with the supply, since both τ_{RC} and τ_{comp} are independent of supply voltage, to the first order. However, when the comparator is ramping, its V_{DS} changes significantly (Fig. 6), and therefore the equivalent r_o is not constant. When the supply increases, the V_{DS} of CG NMOS transistor also increases, resulting in larger r_o and longer τ_{comp}. The measured frequency dropped by 4.3% when the supply was increased from 0.4 to 0.65 V [Fig. 11(c)]. Fortunately, this is not a serious issue when operating under a local regulated supply, which is common in IoT nodes. The power did increase by 13× at 0.65 V, mostly from the body leakage currents of the custom inverters with dynamic threshold-voltage MOSFETs [14], since the static bias current is immune to the supply change due to the PD-AMP. No significant difference was observed from different chips. The temperature stability was examined at different supply voltages without recalibration. As shown in Fig. 11(d), the stability is almost unchanged except the center frequency drops when the supply increases. This oscillator achieves state-of-the-art performance with the lowest power consumption (1.14 nW) at the lowest supply voltage (0.4 V) and the best efficiency (0.93 nW/kHz) among kilohertz-range temperature-compensated relaxation oscillators (Table I).

V. CONCLUSION

In this paper, the comparator delay and temperature dependence of a relaxation oscillator based on a ramp response model were analyzed. A two-stage τ_{SW}-canceling comparator and a technique that utilizes the linear temperature-dependent delay were proposed to implement a relaxation oscillator for low-power and low-voltage applications. Measurement results validate the proposed technique and demonstrate state-of-the-art performance.

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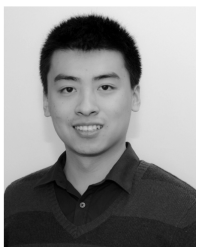

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