An ECG Chopper Amplifier Achieving 0.92 NEF and 0.85 PEF with AC-coupled Inverter-Stacking for Noise Efficiency Enhancement

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Outline

• Motivation and Introduction
• Noise Efficiency Enhancement by OTA Stacking
• ECG Amplifier Architecture
• Circuit Implementation
• Simulation Results
• Conclusion
Motivation

World of IoTs and m-Health

Miniaturized Wearable & Implantable Devices

• Automated, remote monitoring
• Early detection/diagnosis

Major Challenges:
• Continuous reliable monitoring via a small integrated unit
• Ultra-low power sensing circuits with long battery life
ECG Acquisition Amplifier

Amplifies weak, low-bandwidth physiological signals

Power consumption is noise-limited

Noise Efficiency Factor (NEF) → noise-current trade-off

\[ NEF = v_{ni,\text{RMS}} \sqrt{\frac{2I_{\text{tot}}}{V_T 4k_B T \pi BW}} \]

Power Efficiency Factor (PEF) → noise-power trade-off

\[ PEF = NEF^2 V_{DD} \]

\( I_{\text{tot}} \): amplifier current, \( v_{ni,\text{RMS}} \): input referred noise, \( BW \): bandwidth,
\( V_T \): thermal voltage, \( T \): temperature, \( k_B \): Boltzmann’s constant
Noise Efficiency Limitation

For a differential amplifier if

- only input diff-pair noise
- devices in sub-threshold

\(\kappa\): gate-coupling coefficient typically \(\sim 0.7\)

**Fundamental NEF Limit**

\[
NEF_o = \sqrt{\frac{2}{\kappa^2}} \approx 2.02
\]

**NEF Improvements: Prior Art**

- **Current Reuse [1]**: Inverter-based OTA
  
  \[
  NEF = \frac{NEF_o}{\sqrt{2}}
  \]
  
  \[G_m = g_{mn} + g_{mp}\]

- **Dual Supply [2]**:
  
  \[
  PEF \approx \frac{PEF_o}{4}
  \]

[1] - Chae TNSRE ‘09
Proposed Stacked OTA

AC-coupled inverter-based transconductor

\[ R_o = r_{on} \parallel r_{op} \]
\[ G_{mo} = g_{mn} + g_{mp} \]
Proposed Stacked OTA

\[ G_m \text{ boosting: } G_m = N G_{mo} \]  
\[ R_{out} = R_o / N \]
\[ A_v = G_m R_{out} = G_{mo} R_o \]

\( G_m, R_{out} \): compound transconductance, output impedance  
\( G_{mo}, R_o \): single inverter transconductance, output impedance  
\( A_v \): OTA Gain

[3] - Iguchi ISSCC’16 (crystal oscillator start-up)
Proposed Stacked OTA

**Proposed Stacked OTA**

**$G_m$ boosting:**

\[ G_m = NG_{mo} \]

**Input-referred noise:**

\[
\begin{align*}
\nu_{ni, \text{thermal}}^2 &= \frac{4k_BT\gamma}{NG_{mo}} \\
\nu_{ni, \text{flicker}}^2 &= \frac{1}{4NF} \left[ \frac{K_n}{C_{ox}(WL)_n} + \frac{K_p}{C_{ox}(WL)_p} \right]
\end{align*}
\]

$\gamma$, $C_{ox}$, $K_n$, $K_p$: device parameters

(WL)$_n$, (WL)$_p$: device sizes

$\nu_{ni}$: input referred noise PSD

**Noise efficiency enhancement:**

- $\sqrt{2N}$ times improvement in $NEF$
- $2N$ times improvement in $PEF$ (same $V_{DD}$)

**For a differential implementation:**

2-stack NEF limit: 1.01
3-stack NEF limit: 0.82
Inverter-Stacking Trade-offs:

\[ V_{DD,\text{min}} = NV_{INV} + V_{\text{tail}} \]

\[ NEF \propto \frac{1}{\sqrt{N}} \]

\[ PEF_{\text{min}} \propto V_{INV} + \frac{V_{\text{tail}}}{N} \]

\( V_{INV}, V_{\text{tail}} \): voltage headroom for single inverter, tail source

Normalized minimum PEF:
- 2-stack: 0.82
- 3-stack: 0.75
- 4-stack: 0.72

3-stack with 1 V supply is optimal
ECG Amplifier Architecture

Key Challenges:

- AC-coupling of low bandwidth ECG (~250 Hz) would require very large capacitors
- Signal swing with OTA stacking is limited
ECG Amplifier Architecture

Key Challenges:

- AC-coupling of low bandwidth ECG (~250 Hz) would require very large capacitors
- Upmodulate to a higher (chopping) frequency → simpler ac-coupling
- Signal swing with OTA stacking is limited
- First stage with low signal swing
Other Requirements:

- Low in-band flicker noise
- High CMRR (for 60Hz noise)
- Electrode polarization offset
- High input impedance
- 2nd stage DC bias
ECG Amplifier Architecture

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Circuit Implementation

Fully Differential Stacked OTA:

- $C_{ci}$, $C_{co}$, $C_{Dn,p}$ $\rightarrow$ low impedance (ac-shorts) at the chopping frequency (5 kHz)
- $C_{Dn,p}$ are 25 pF MOS capacitors to account for $1/g_m$ source impedance $\sim 6M\Omega$. (40×40 μm²)
- Differential operation aids the decoupling with source nodes acting as virtual shorts.
Fully Differential Stacked OTA:

Mid-band gain:

\[ A_{M1} = -\left(\frac{C_{Ci}}{C_{Ci} + C_{in,tot}}\right)G_{mo}R_{o}\left(\frac{NC_{co}}{NC_{co} + C_{L1}}\right) \]

Large \( C_{L1} \) required for Miller compensation → Use load compensation used instead

\( C_{Ci,o} \) are 4 pF MOM capacitors
Circuit Implementation

2nd stage OTA:

\[ V_{CM} \text{ generation:} \]

\[ V_i \]

\[ V_{CM} \]

Constant-\(G_m\) bias:

Design Summary:

- 1 V Supply

14 nA (79%)
2.3 nA (13%)
0.22 nA (1%)
1.2 nA (7%)
Simulation Results

Stacked OTA simulations

Open-loop gain

Input-referred noise

Both white noise and flicker noise reduce with inverter-stacking
Simulation Results

Closed-loop amplifier simulations

Amplifier differential-mode gain
(using PAC analysis)

Amplifier loop-gain
(using PSTB analysis)

Amplifier Gain (dB)

Frequency (Hz)

1-stack
2-stack
3-stack

35dB mid-band gain

Magnitude (dB)

Phase (°)

Phase Margin ~ 90°
Simulation Results

100 monte-carlo runs (over process and mismatch variations)

Amplifier transient response and spectra

CMRR > 75 dB
PSRR > 60 dB

SFDR = 54 dB
THD = 0.3%
Simulation Results

Amplifier noise performance with inverter-stacking

![Graph showing amplifier noise performance with inverter-stacking](image)

148 nV/√Hz with only 14 nA!
### Summary and Comparison

Best reported NEF of 0.92 and PEF of 0.85!

<table>
<thead>
<tr>
<th></th>
<th>This work#</th>
<th>Harpe ISSCC’15</th>
<th>Jeon ISSCC’14</th>
<th>#Song ISCAS’14</th>
<th>Yaul ISSCC’16</th>
<th>Han ISSCC’13</th>
<th>Chen VLSI’14</th>
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<tbody>
<tr>
<td><strong>Technology Node</strong></td>
<td>65 nm</td>
<td>65 nm</td>
<td>65 nm</td>
<td>180 nm</td>
<td>180 nm</td>
<td>180 nm</td>
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<tr>
<td><strong>Supply (V)</strong></td>
<td>1</td>
<td>0.6</td>
<td>0.6</td>
<td>1</td>
<td>0.2 and 0.8</td>
<td>0.45</td>
<td>1</td>
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<tr>
<td><strong>Power (nW)</strong></td>
<td>17.7</td>
<td>1</td>
<td>16.8</td>
<td>2,500</td>
<td>790</td>
<td>730</td>
<td>266</td>
</tr>
<tr>
<td><strong>Current (nA)</strong></td>
<td>17.7</td>
<td>1.67</td>
<td>28</td>
<td>2,500</td>
<td>987</td>
<td>1,622</td>
<td>266</td>
</tr>
<tr>
<td><strong>Gain (dB)</strong></td>
<td>35</td>
<td>32</td>
<td>51 – 96</td>
<td>50</td>
<td>58</td>
<td>52</td>
<td>60</td>
</tr>
<tr>
<td><strong>BW (Hz)</strong></td>
<td>250</td>
<td>370</td>
<td>250</td>
<td>120</td>
<td>670</td>
<td>10,000</td>
<td>500</td>
</tr>
<tr>
<td><strong>Input-referred Noise (nV/√Hz)</strong></td>
<td>148$^3$</td>
<td>172$^2$</td>
<td>238$^1$</td>
<td>1,400</td>
<td>253</td>
<td>21.8</td>
<td>36</td>
</tr>
<tr>
<td><strong>CMRR / PSRR (dB)</strong></td>
<td>&gt;75 / &gt;60</td>
<td>60 / 63</td>
<td>80 / 67</td>
<td>&gt;60 / &gt;80</td>
<td>85 / 74</td>
<td>73 / 80</td>
<td>89 / 92</td>
</tr>
<tr>
<td><strong>NEF</strong></td>
<td>0.92$^3$</td>
<td>1.08$^2$</td>
<td>1.51$^1$</td>
<td>2.1</td>
<td>2.64</td>
<td>1.17</td>
<td>2.1</td>
</tr>
<tr>
<td><strong>PEF</strong></td>
<td>0.85$^3$</td>
<td>1.17$^2$</td>
<td>2.28$^1$</td>
<td>2.64</td>
<td>4.1</td>
<td>1.37</td>
<td>1.6</td>
</tr>
</tbody>
</table>

# Simulated Designs  
$^1$1-stack  
$^2$2-stack  
$^3$3-stack
Conclusion

• AC-coupled Inverter-stacking for $G_m$-boosting leading to noise efficiency enhancement
• Best-reported NEF/PEF from simulations
• Useful technique particularly for IoT mHealth applications
Backup Slides