A Sub-pA Current Sensing Front-End for Transient Induced Molecular Spectroscopy

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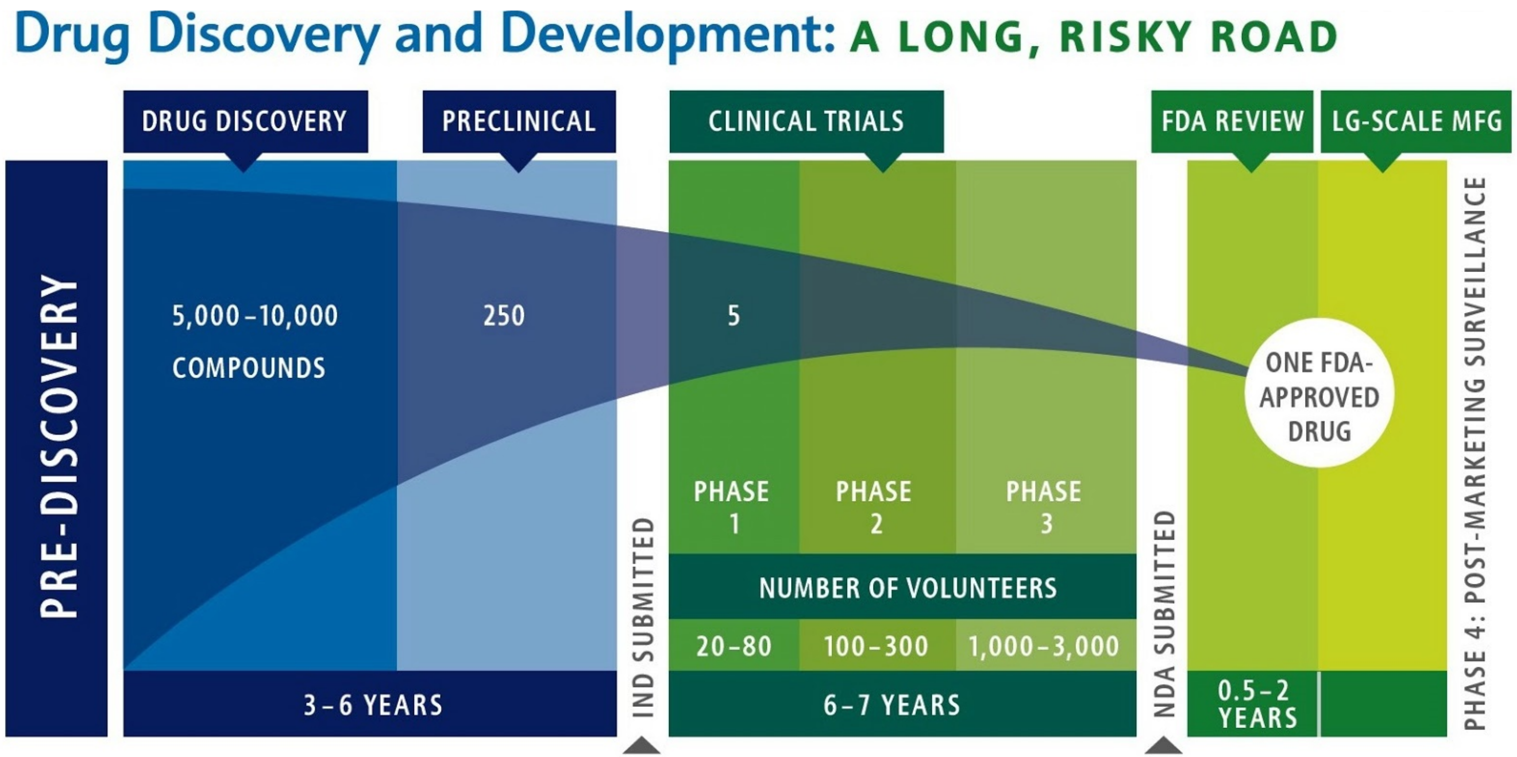
BIO Sensors & Electronics

New Drug Discovery

- High-cost (>$2.6B/drug[1]) and failure rate from mid- to late-stage
- Many diseases are highly linked to protein-ligand abnormality



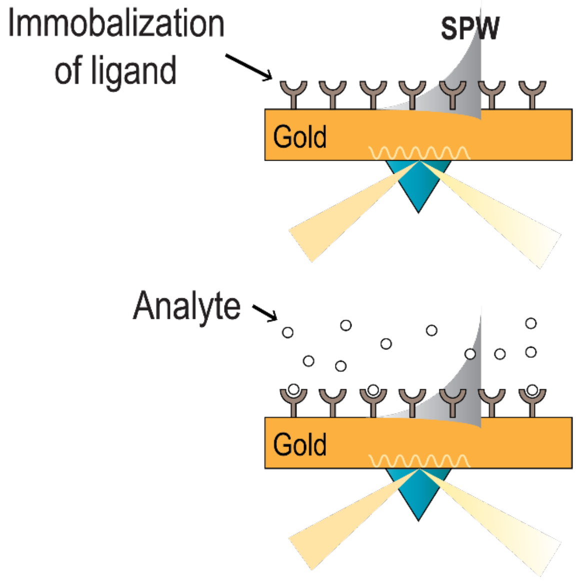
[1]

Need a solution for accurate *in-vitro* study of protein-ligand interactions

[1] *Pharmaceutical Research and Manufacturers of America*

Existing Methods for Protein-Ligand Detection

Surface Plasmon Resonance

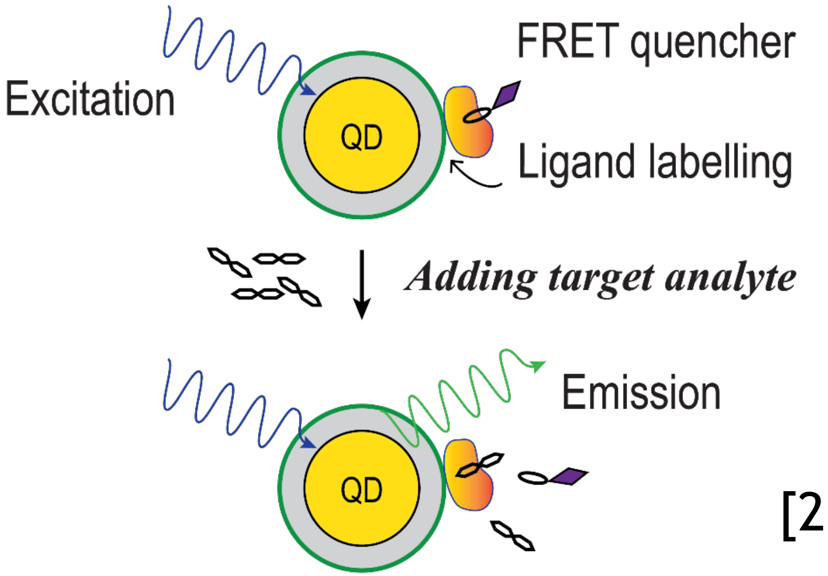


Prior to binding:
Biolayer refractive index, n
SPW propagation constant, β

After analyte binding:
Analyte concentration, c
$n \rightarrow n + \Delta n$
$\beta \rightarrow \beta + \Delta\beta$

[1]

FRET



[2]

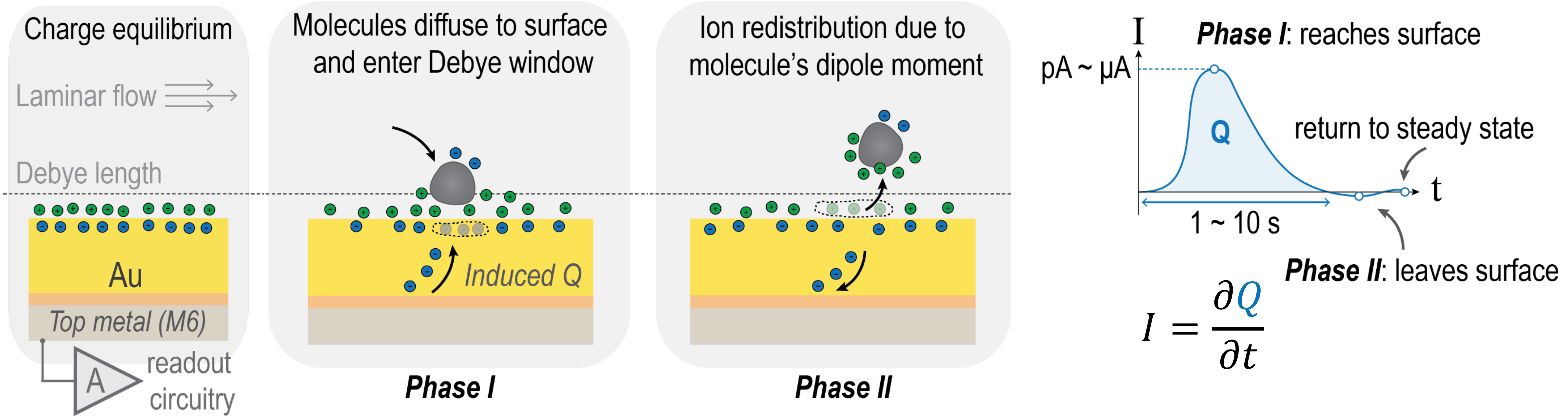
✓ Binding kinetics
✗ Immobilization of ligand

✓ Solution phase
✗ Labelling of ligand

Labeling and immobilization significantly limit degree of freedom for binding

[1] J. Homola, *Analytical and Bioanalytical Chemistry*, 2003; [2] C. Fan, *TRENDS in Biotechnology*, 2005

Transient Induced Molecular Spectroscopy (TIMES)



$$I = \frac{\partial Q}{\partial t}$$

✓ Label- and immobilization-free *in-vitro* protein-ligand detection

✓ Closer to physiological conditions and better signal integrity

Requires a sensitive AFE for charge sensing

T. Zhang, Y. Lo, *Scientific Reports*, 2016

µTIMES Specification

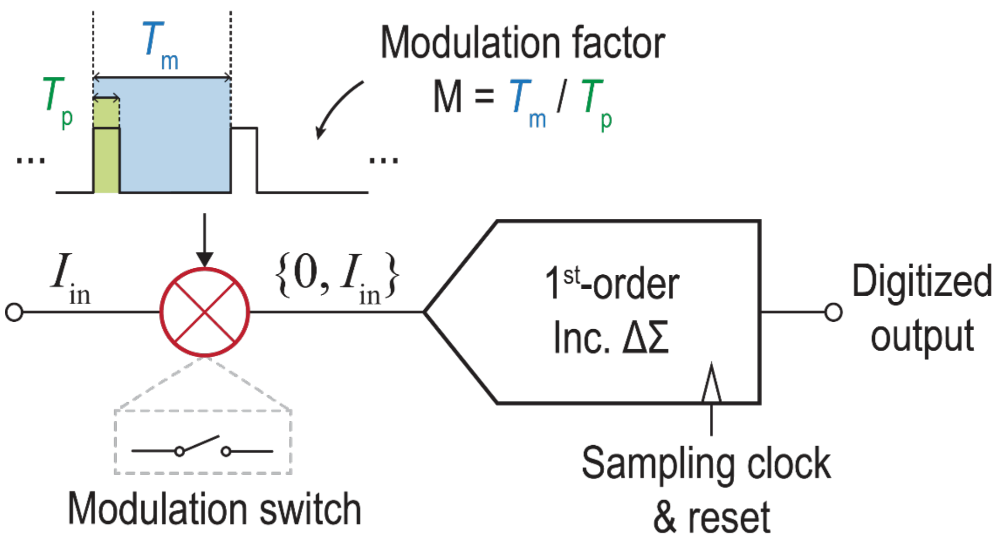
Parameter	Application	Circuit
Sensor size	8 channels	300µm×300µm M6
Resolution	0.1 µM sensitivity	100 fA
Cross-scale DR	0.1 µM – 10 mM range	100 fA – 1 µA
Bandwidth	5 cm/s flow rate	10 Hz

- Active area < 0.2 mm^2/ch.
- Partition across 4 references with 80dB SNDR each
- WE/RE → pseudo-differential input

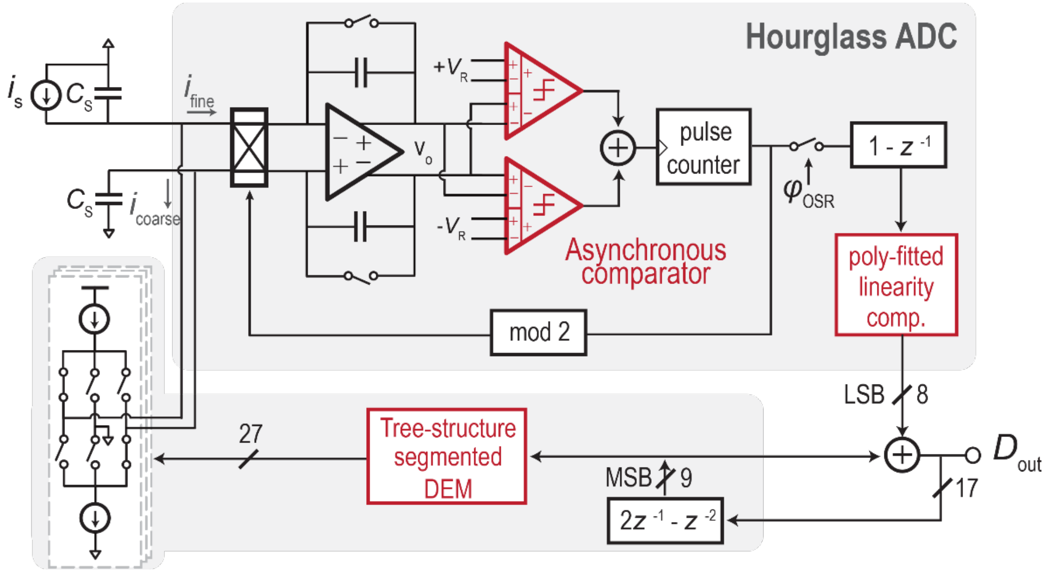
T. Zhang, Y. Lo, *ACS Central Science*, 2016

Existing Sub-pA Current AFEs

[H. Li, TBioCAS'16]



[C. Hsu, ISSCC'18]

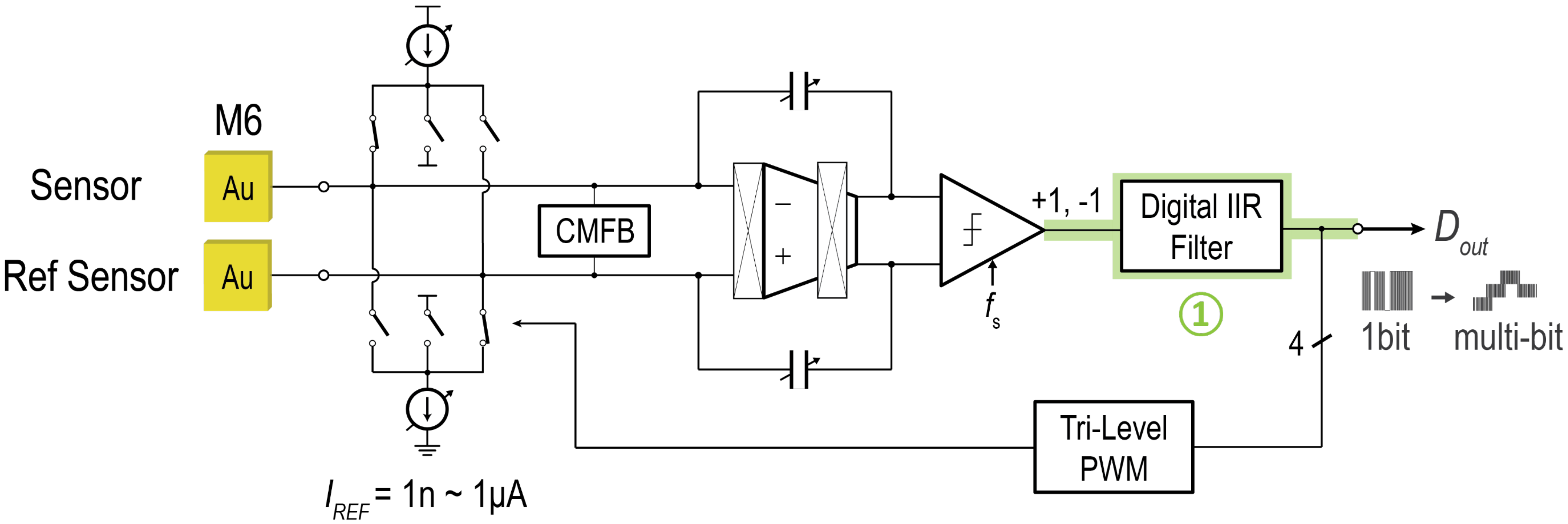


- Sensitive to aliasing
- Input sampling → noise folding
- Charge injection to sensor

- Heavy digital backend
- Large area, limited # of channels

Aim to achieve 100fA sensitivity with small area/power

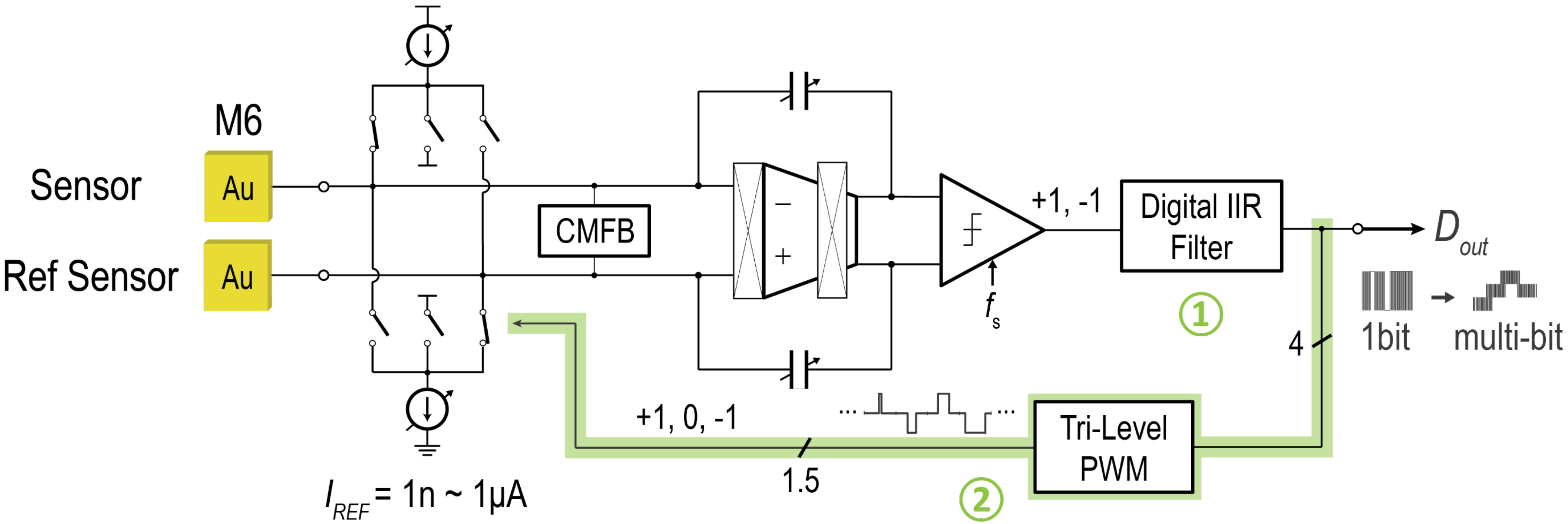
Proposed µTIMES AFE Architecture



µTIMES → 1st-order current-mode ΔΣ + digital IIR (linear predictor)

① 1-bit quantizer + digital IIR achieves quasi multi-bit quantization

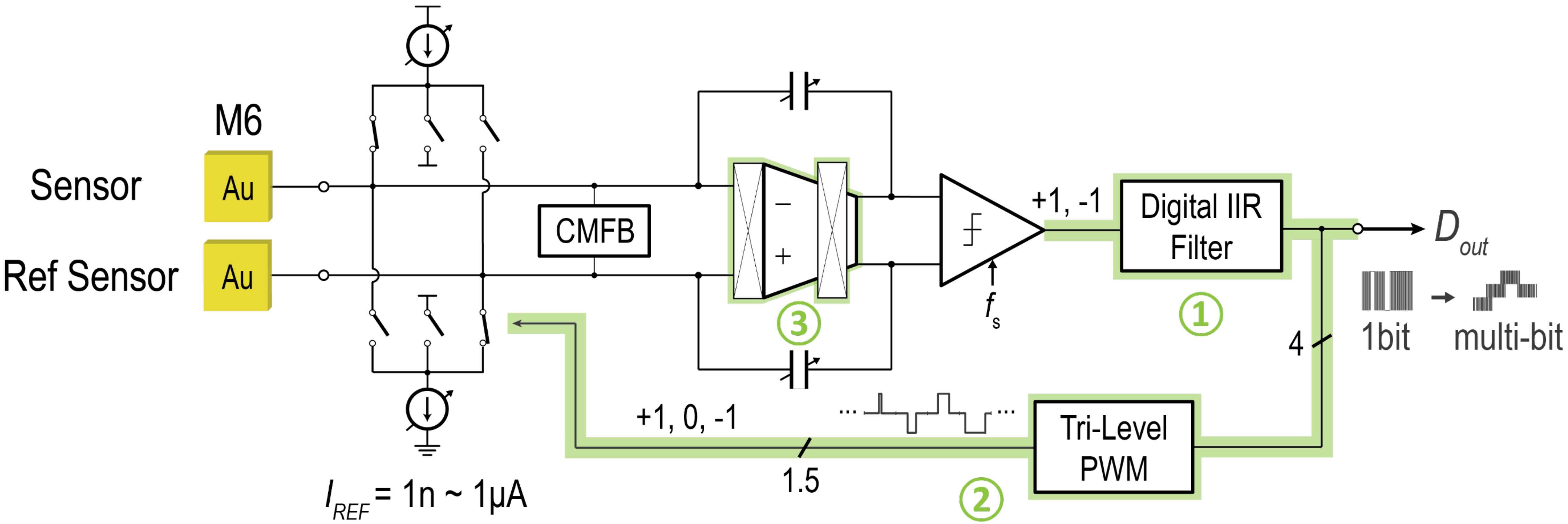
Proposed μTIMES AFE Architecture



Integrator only needs to process half of original pulse amplitude

② Tri-level PWM avoids intensive hardware and relaxes filter linearity

Proposed µTIMES AFE Architecture



Lower f_s relaxes speed requirement and improves anti-aliasing

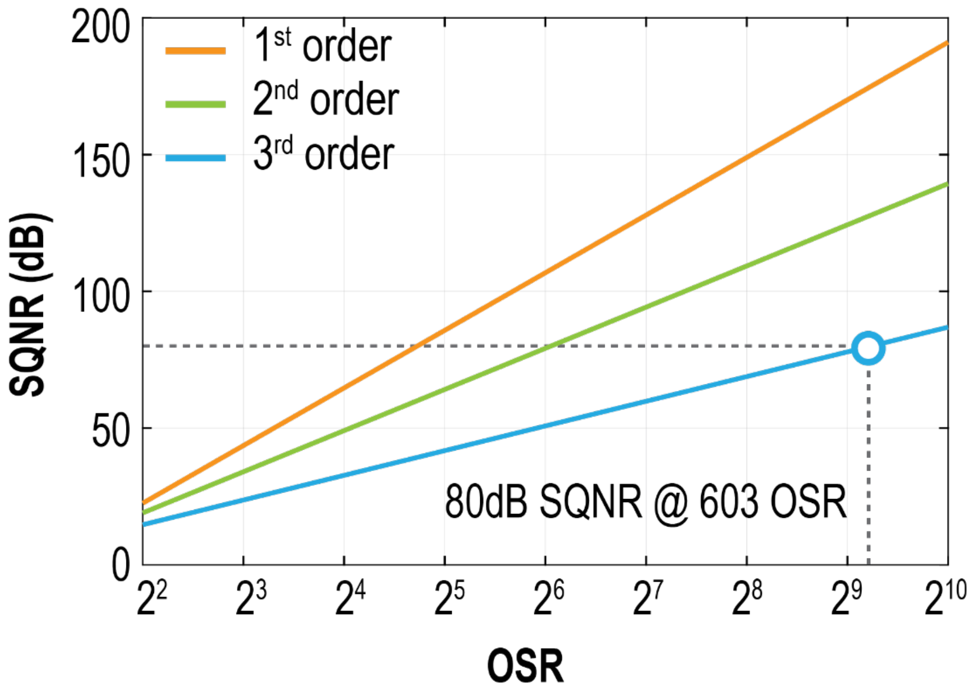
③ Multi-bit feedback effectively reduces f_s

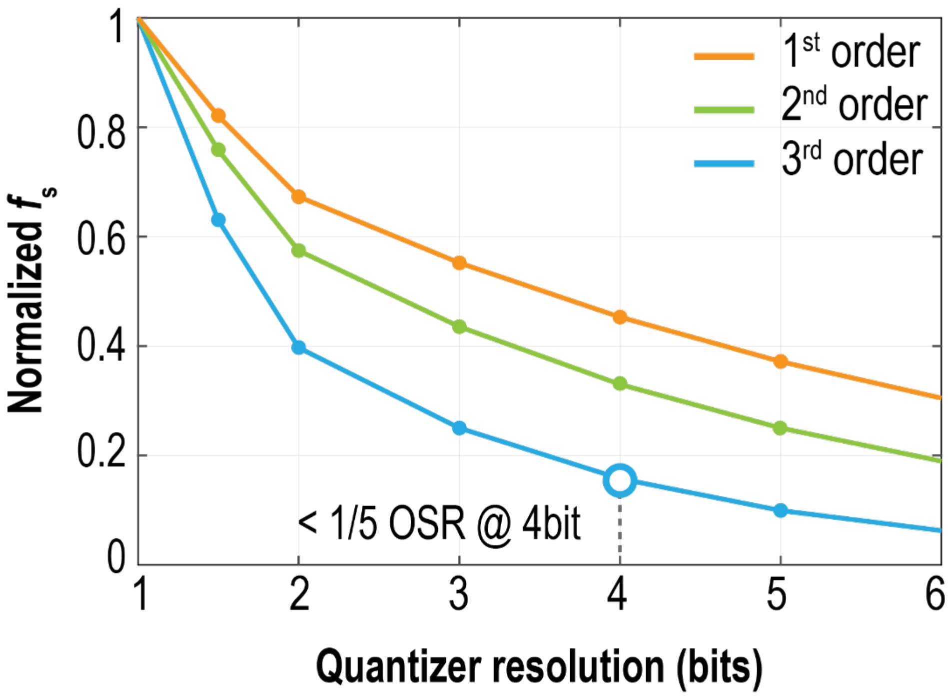
Issues with Single-bit Quantization

- Limited SQNR for given OSR
- Deterministic quantization noise
- Arbitrary quantizer gain

$$\frac{OSR_{\text{nbit}}}{OSR_{\text{1bit}}} \propto 2^{-\frac{2n}{2L+1}}$$

n = Quantizer bits
L = order





Limited SQNR → Large OSR → Power hungry & poor anti-aliasing

Issues with Single-bit Quantization

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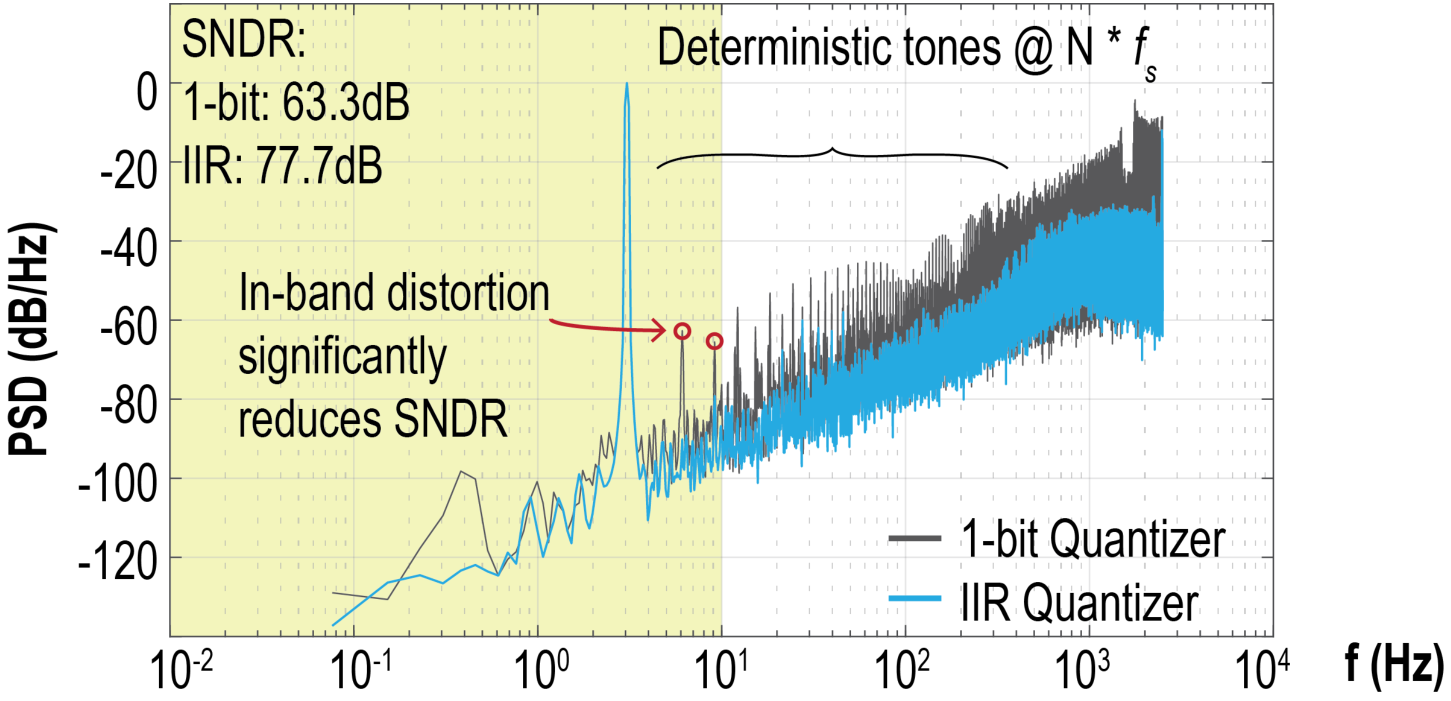
<u>What we will find later:</u>
More transitions and quantization levels → less tonal effect



Deterministic quantization noise → tonal → SNR⇩

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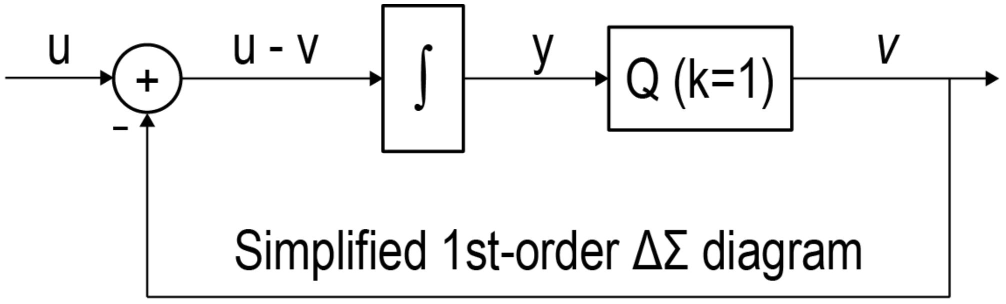
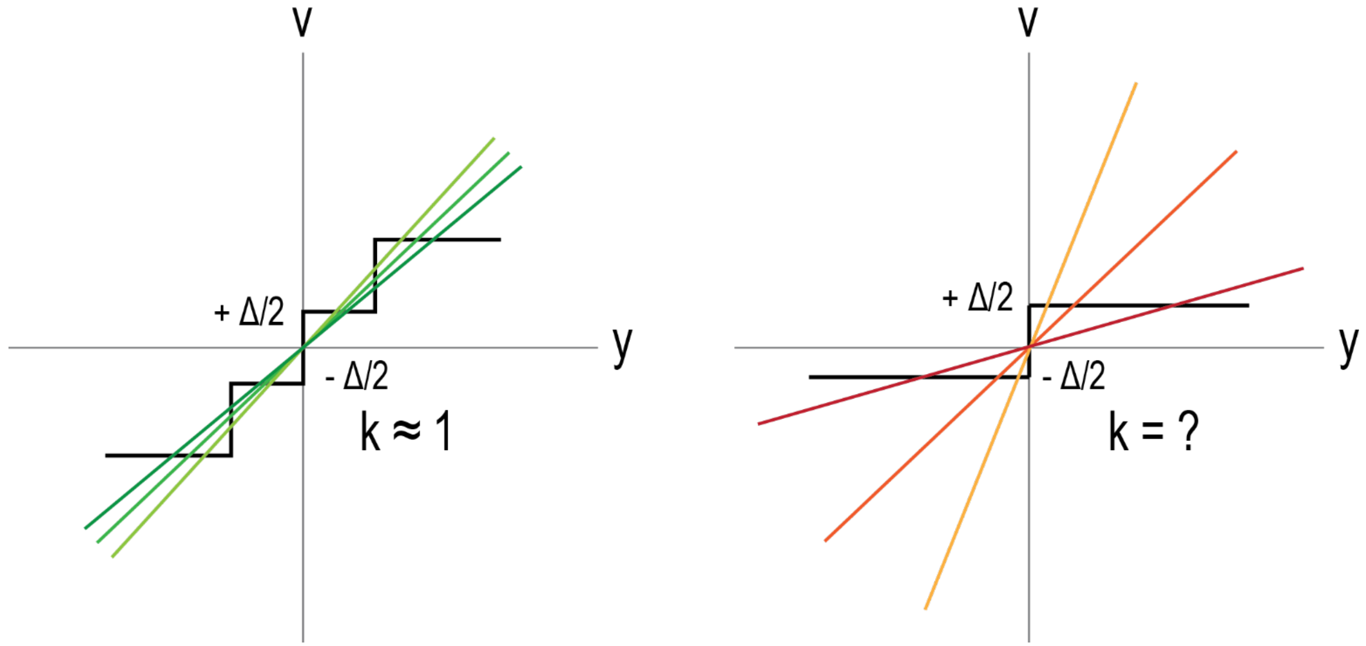
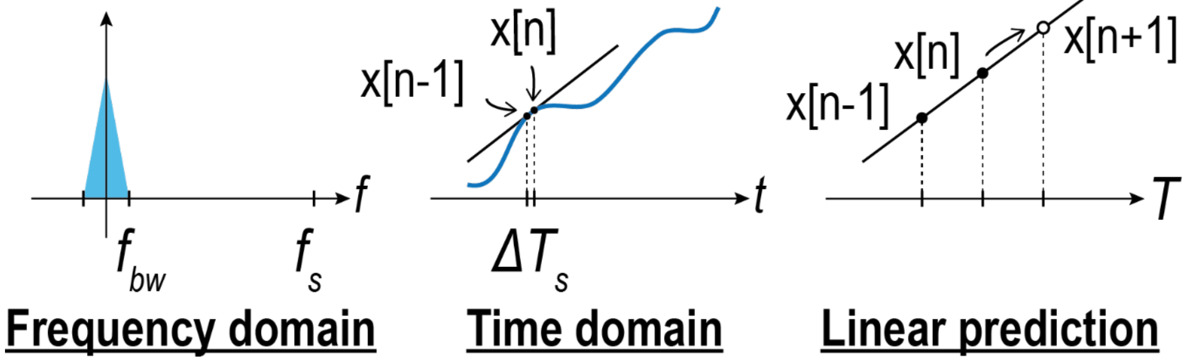




Arbitrary quantizer gain → deviate from linear model

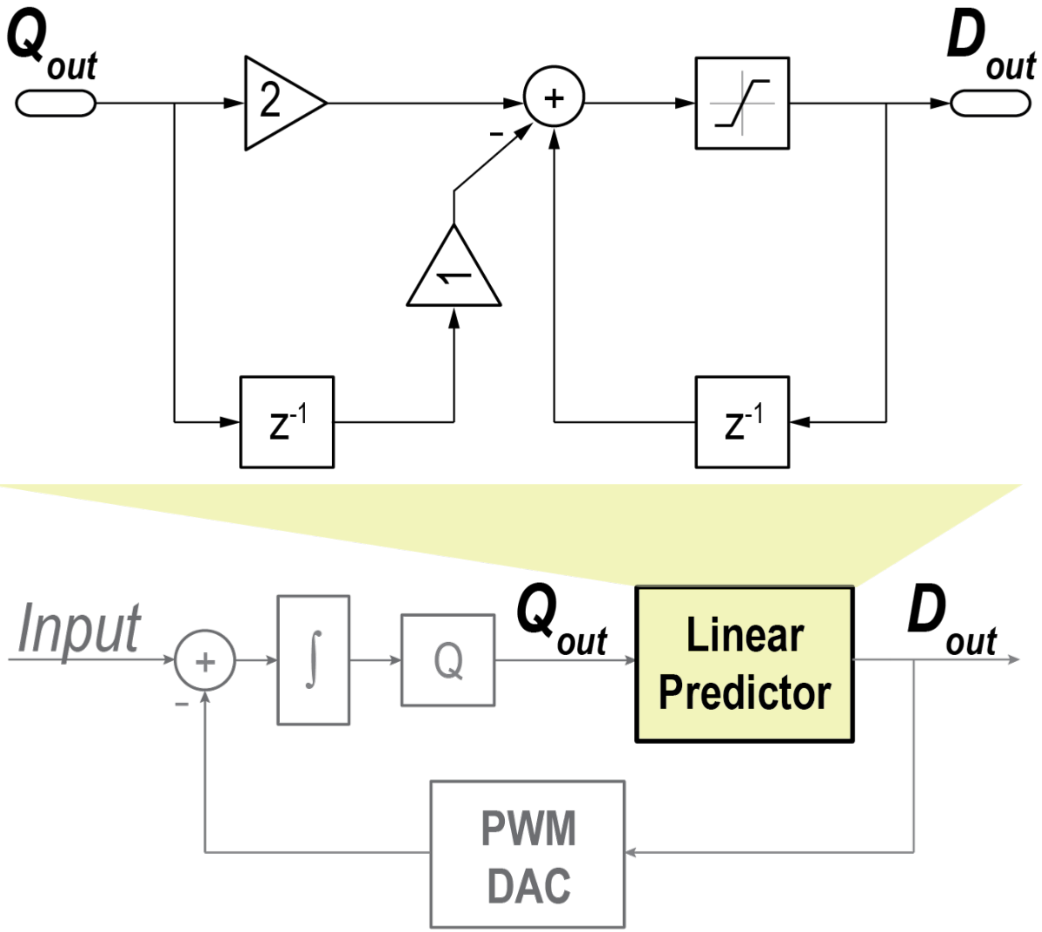
Motivation: Linear Prediction in ΔΣ



$$x[\mathrm{n}+1] = x[\mathrm{n}] + \frac{\partial x}{\partial t} \cdot \Delta T = x[\mathrm{n}] + x[\mathrm{n}] - x[\mathrm{n}-1]$$

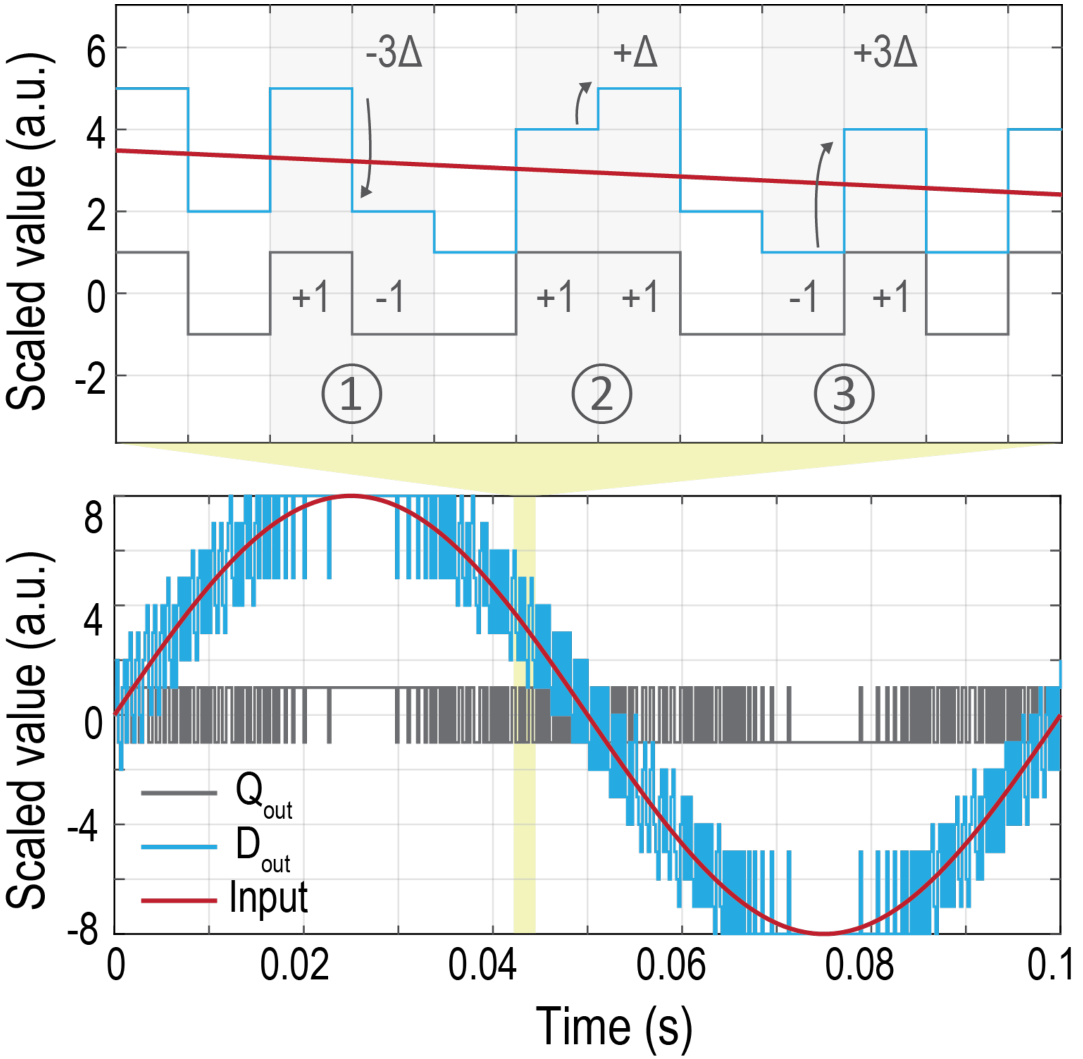
$$\boldsymbol{D}_{\mathbf{out}}[\mathrm{n}] = D_{\mathrm{out}}[\mathrm{n}-1] + 2\times Q_{\mathrm{out}}[\mathrm{n}] - Q_{\mathrm{out}}[\mathrm{n}-1]$$

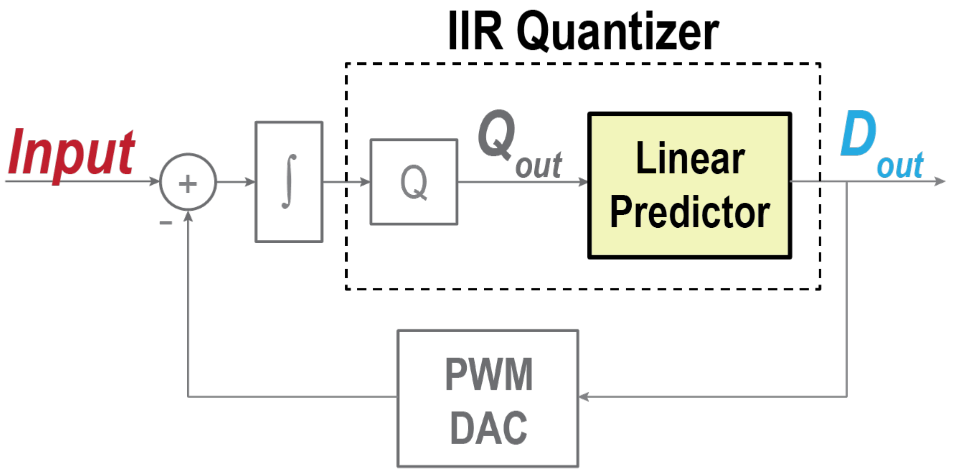
IIR filter → $\frac{D_{\mathrm{out}}[z]}{Q_{\mathrm{out}}[z]} = \frac{2-z^{-1}}{1-z^{-1}}$



→ Multi-bit achieved with only a 4-bit adder, scaler, and two FFs

Turning 1-bit Into Multi-bit

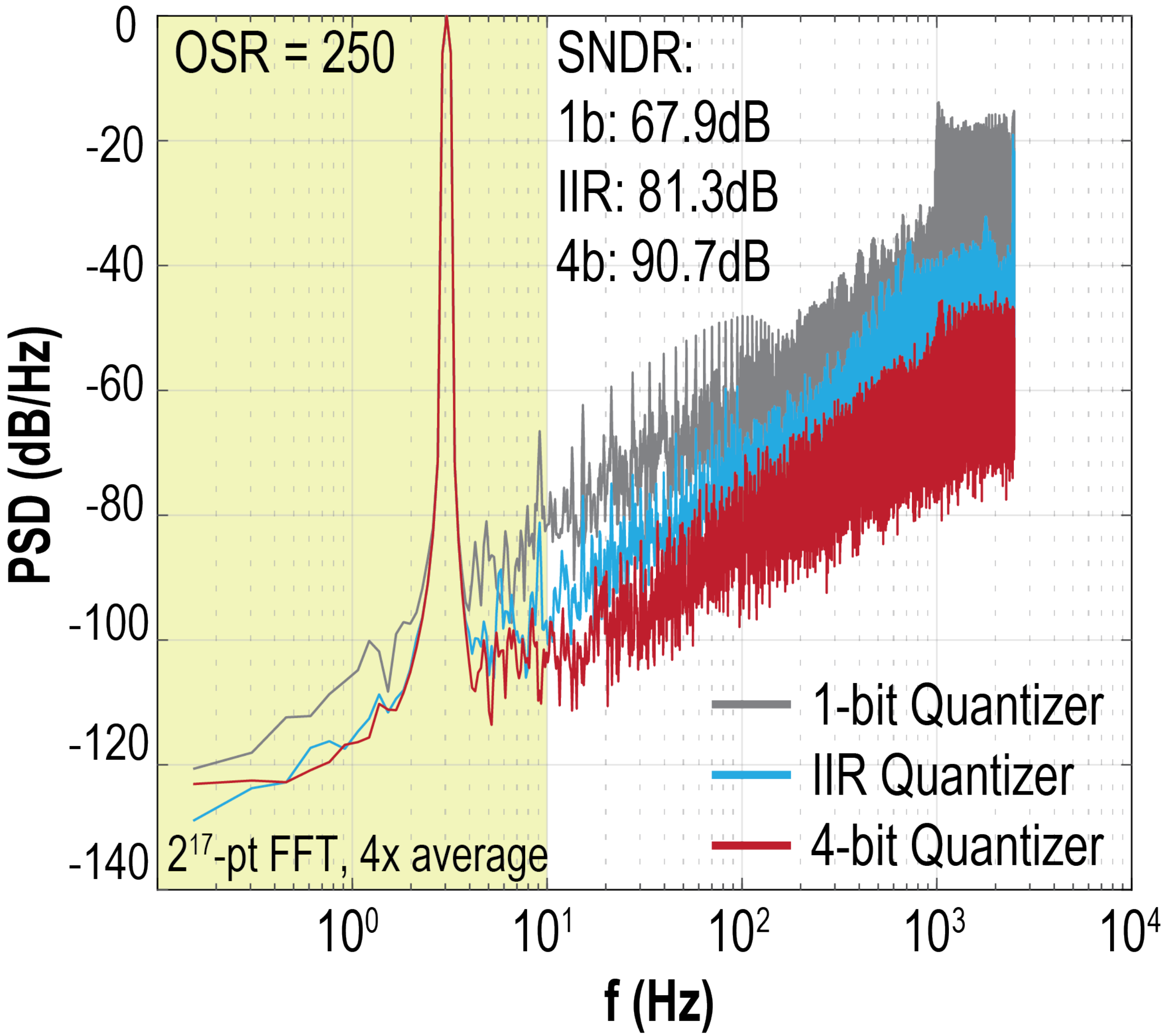




<u>First-order observations:</u>

- D_{out} closely tracks input signal
- More transitions → less tonal
- Quantization step $\in \{\Delta, 3\Delta\}$
- $f_{sig,max}$ and PSD?

Theoretical PSD and $f_{\text{sig,max}}$



Conservative SQNR analysis:

→ $e_q \in [-\frac{3\Delta}{2}, +\frac{3\Delta}{2}]$

→ $\sigma_q^2 = \frac{1}{3\Delta}\int_{-\frac{3\Delta}{2}}^{\frac{3\Delta}{2}} u^2 du = \frac{9\Delta^2}{12}$

~9.5dB worse SQNR than ideal 4b Q

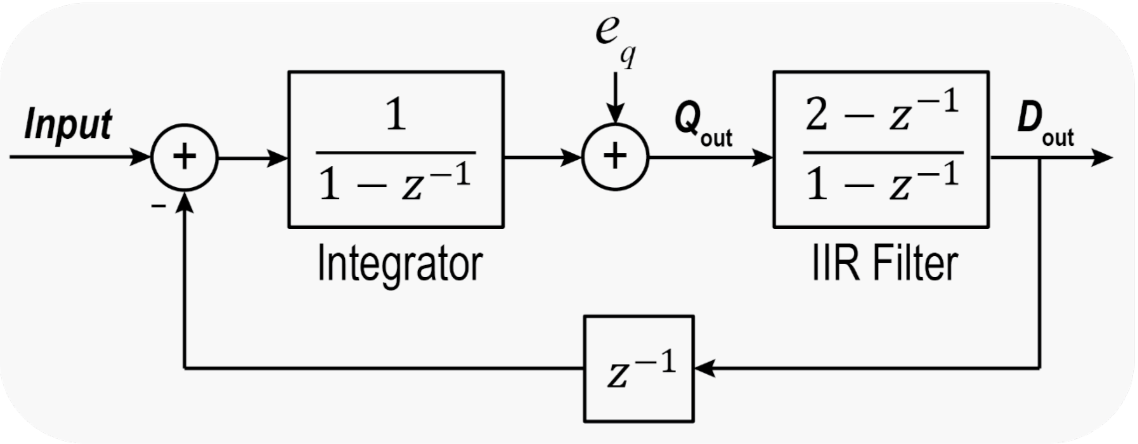
$f_{\text{sig,max}}$ requirement:

→ $\frac{\partial A \sin(2\pi f_{\text{sig}} t+\phi)}{\partial t} \leq \frac{3\Delta}{T_s}$

→ $f_{\text{sig}} \leq \frac{3 f_s}{2\pi \cdot 2^{n-1}} \overset{n=4}{\Longrightarrow} \frac{3 f_s}{16\pi}$

IIR-ΔΣ requires OSR > 8

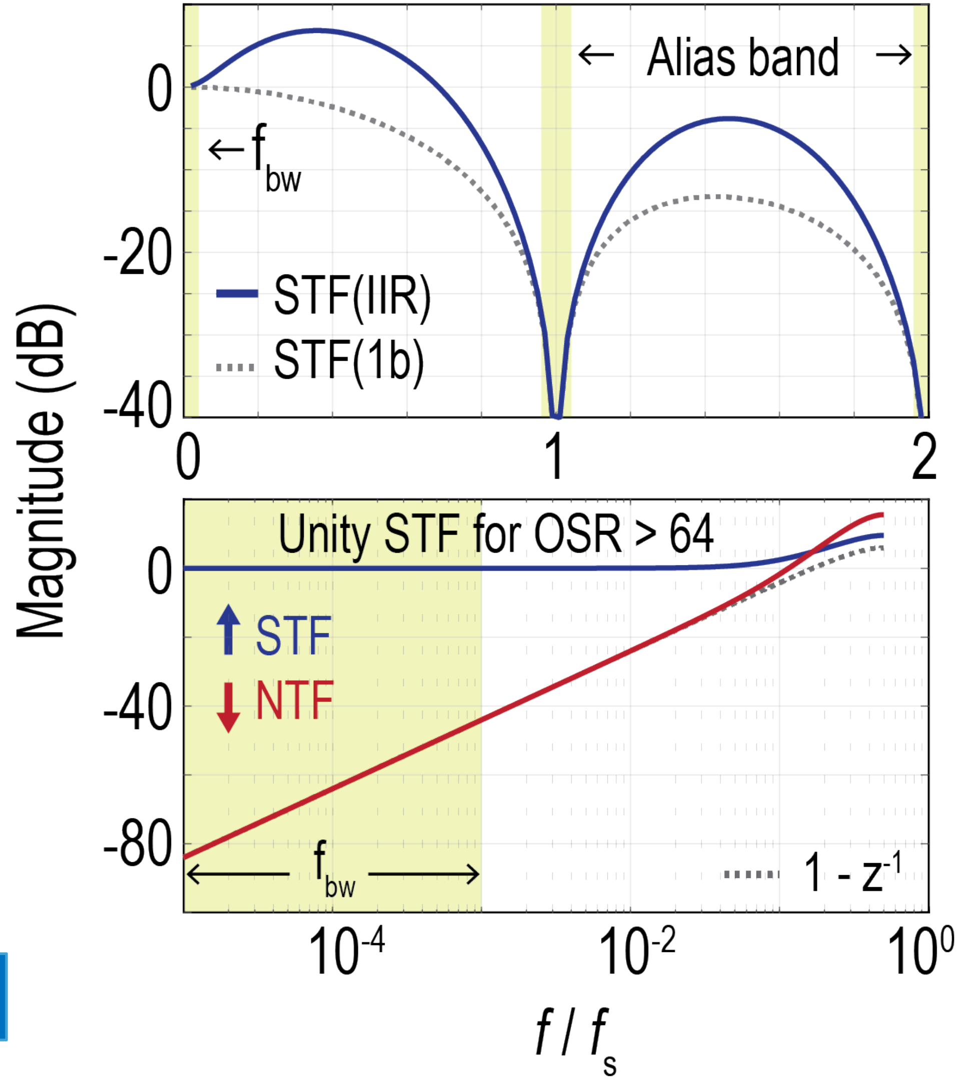
STF & NTF



$$NTF(z) = (2 - z^{-1})(1 - z^{-1})$$

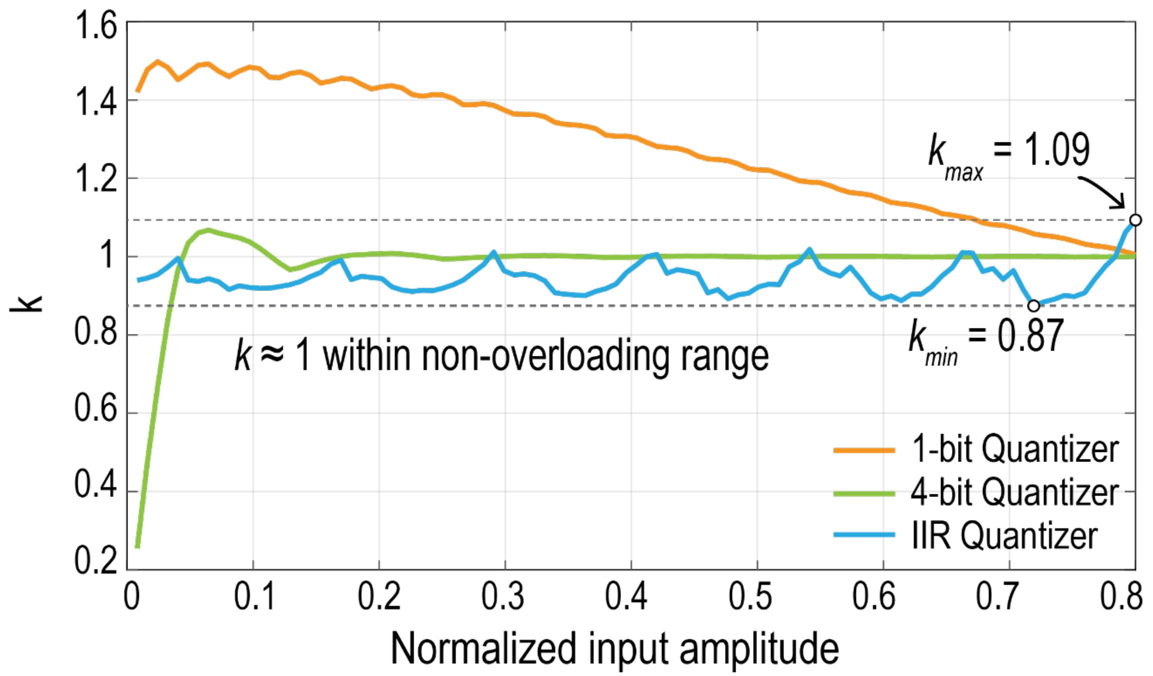
$$\rightarrow STF(f) = \frac{1}{j2\pi f}(2 - e^{-j2\pi f})(1 - e^{-j2\pi f})$$

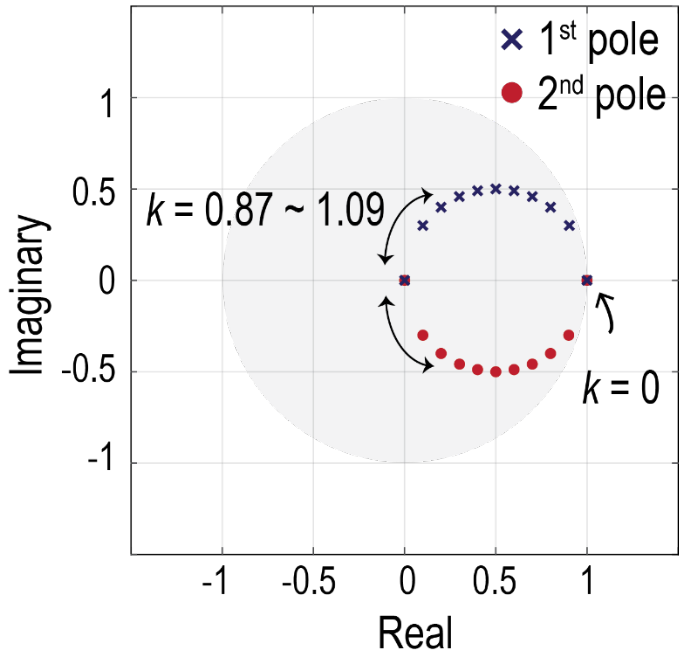
- 1st-order shaping NTF
- ~9dB larger out-of-band gain



Unity in-band STF & inherent anti-aliasing

IIR Quantizer Gain





$$NTF_k(z) = \frac{\frac{2 - z^{-1}}{1 - z^{-1}}}{1 + k \cdot L(z)}$$

$NTF_k(z)$: NTF $(k \neq 1)$

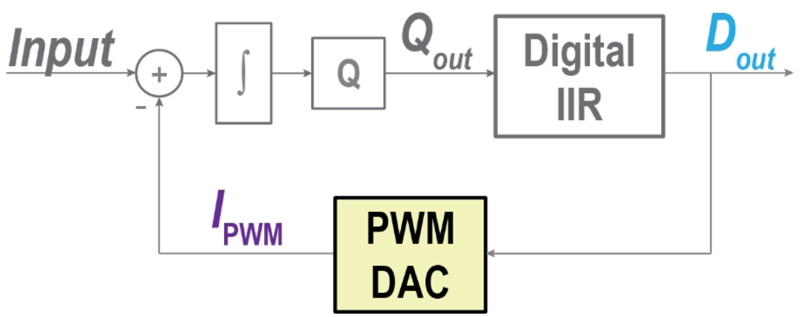
$L(z)$: loop gain $(k = 1)$

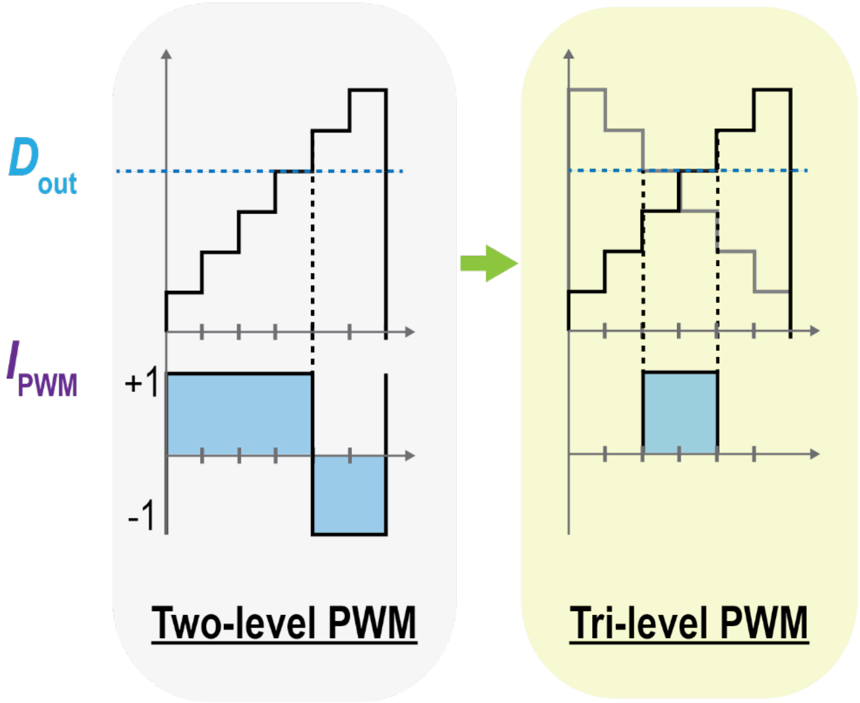
- k - smallest $\overline{\sigma_e^2}$ between quantizer input y and output v
  - $k = \langle v, y\rangle / \langle y, y\rangle$ [1]
- Peak SNDR @ 0.8FS input level → define non-overloading range [0, 0.8FS]

k shows IIR quantizer can be statistically approximated as a multi-bit quantizer

[1] S. Pavan, R. Schreier, G. Temes, 'Understanding delta-sigma data converters', *John Wiley & Sons*, 2017

Tri-Level PWM DAC

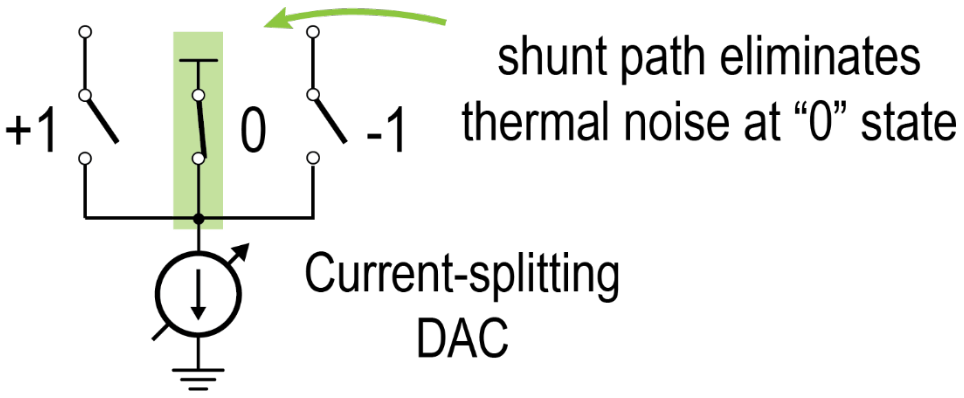




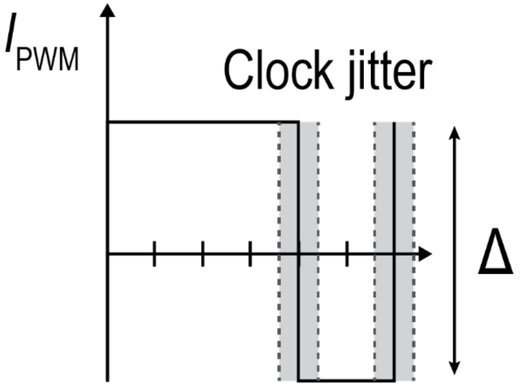
- PWM DAC
  - Entirely digital coded → less hardware
  - CT loop filter → pulse shape independent
- Current-steering DAC
  - nA ~ μA reference from current-splitting
  - No loading → larger loop gain, linearity ⇧
- Two-level PWM → Tri-level PWM
  - Lose inherent linearity
  - Even-order distortion eliminated [1]
  - RZ DAC → ISI immunity
  - Half pulse → noise, jitter, OTA linearity ⇧

[1] F. Colodro, A. Torralba, *TCAS-I*, 2009

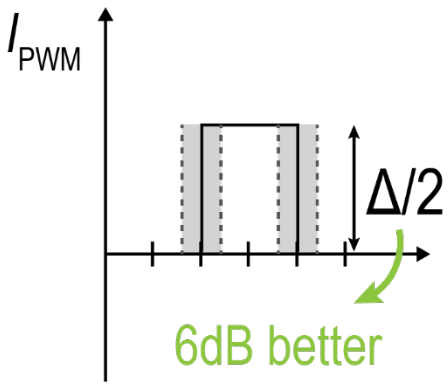
Tri-Level PWM DAC



Tri-level current-steering DAC



Two-level PWM



Tri-level PWM

Current steering

$$S_{i,CS}(f) = 4kT\gamma \frac{2I_{DAC}}{V_{DD}/2}$$

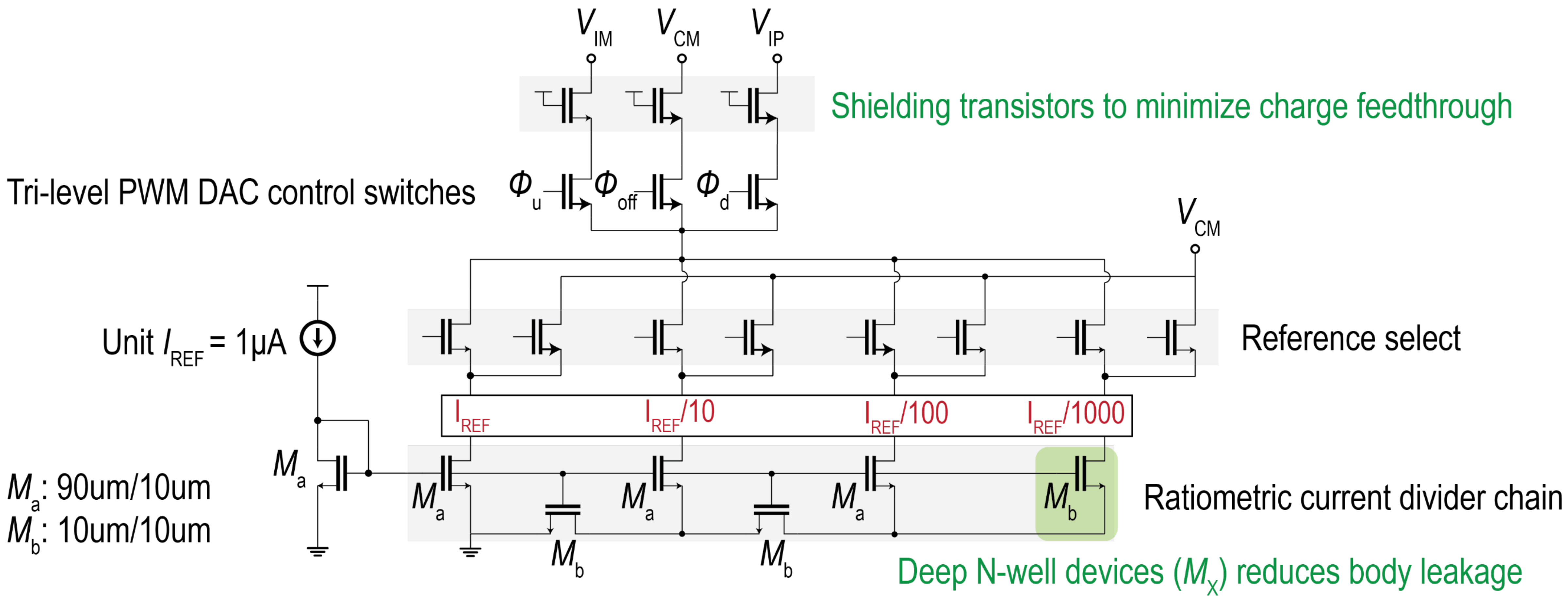
Resistive

$$S_{i,R}(f) = 4kT \frac{I_{DAC}}{V_{DD}/2}$$

- Current-steering DAC with shunt path
  - Bypass most noise for small input
  - Low-pass filtered bias noise
  - Linearity maintained by careful sizing
- Lower jitter sensitivity
  - $SNR_{jitter} \propto \frac{1}{\sigma_{DAC}^2 \sigma_j^2}$
  - Half pulse amplitude → σ_{DAC}^2 ⇩ 4x

PWM ADC → Light weight, multi-bit

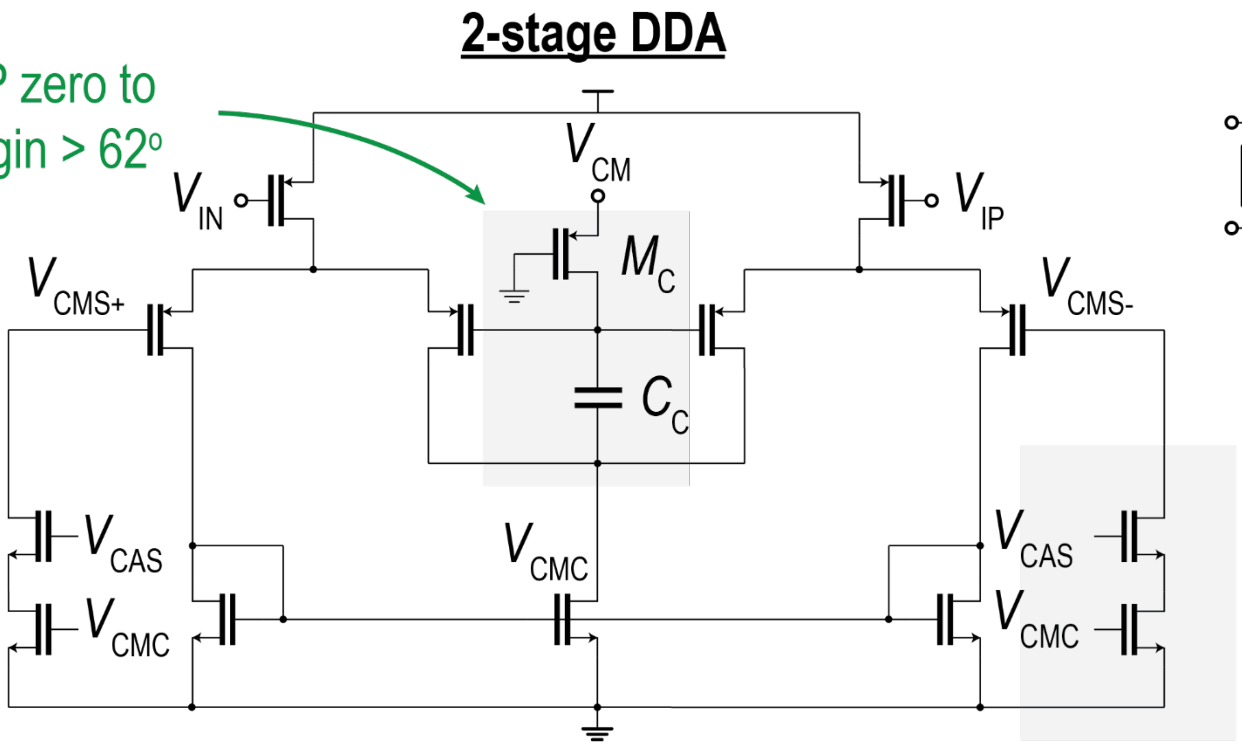
Current-Splitting DAC

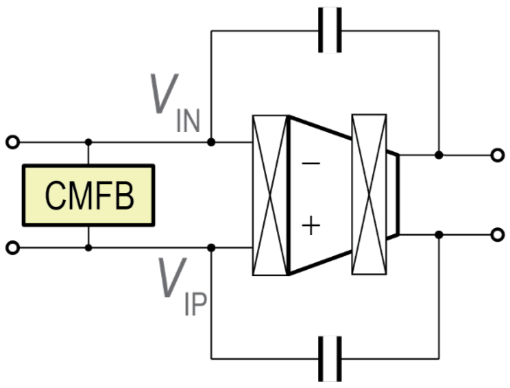


C. Enz, E. Vittoz, *ISCAS*, 1996

Continuous-Time CMFB

M_C, C_C introduces a LHP zero to compensate phase margin > 62°

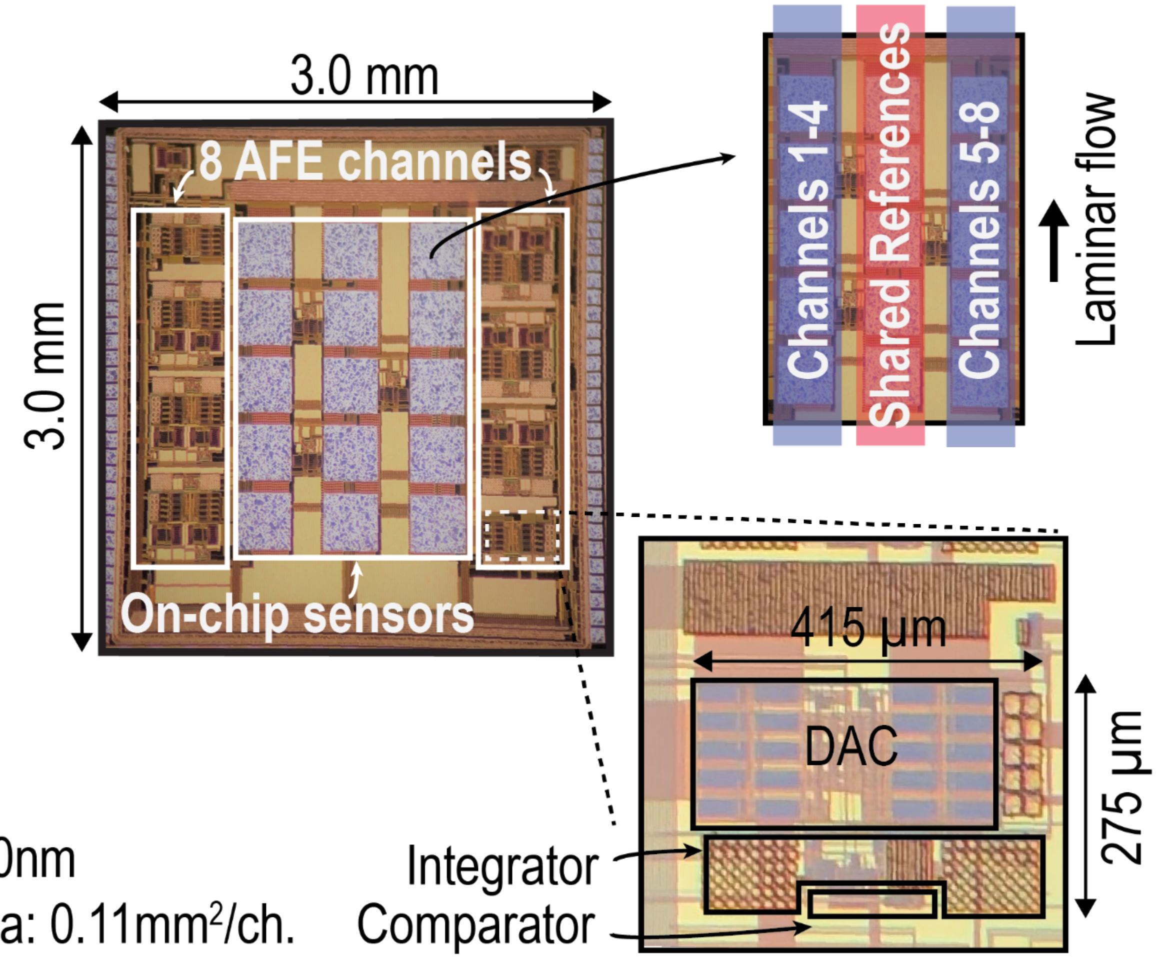




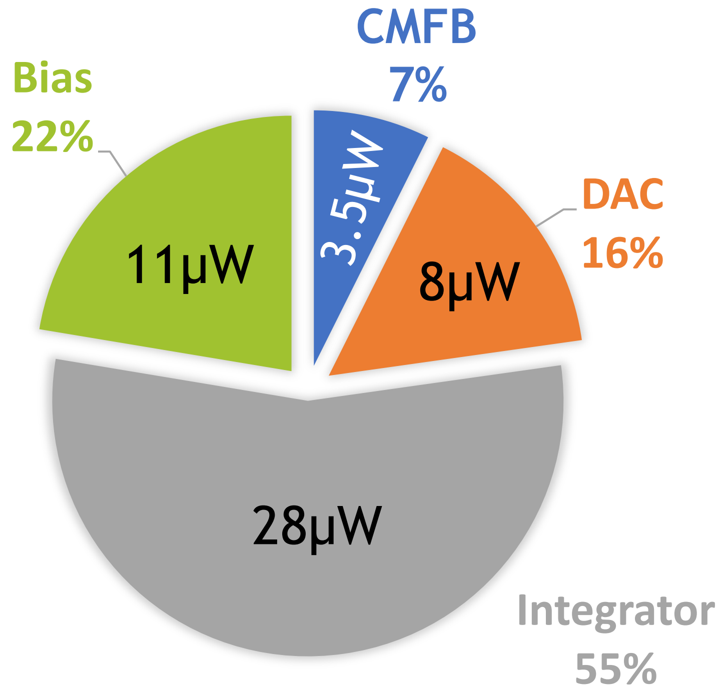
Second CS stage provides > 90dB loop gain and large output impedance

L. Luh, J. Draper, *TCAS-II*, 2000

Chip Micrograph



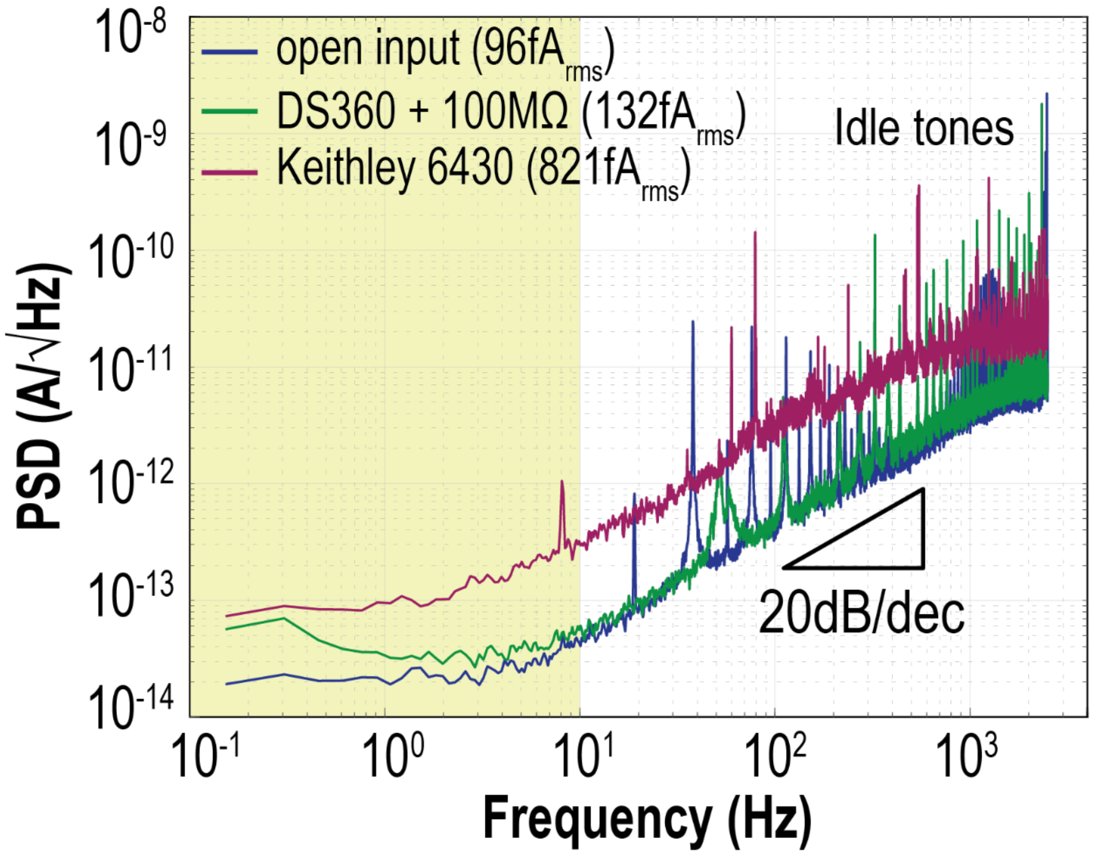
TSMC 180nm
Active area: 0.11mm^2/ch.



Total power: 50.3µW/ch
* Comparator and digital logic consumes negligible power

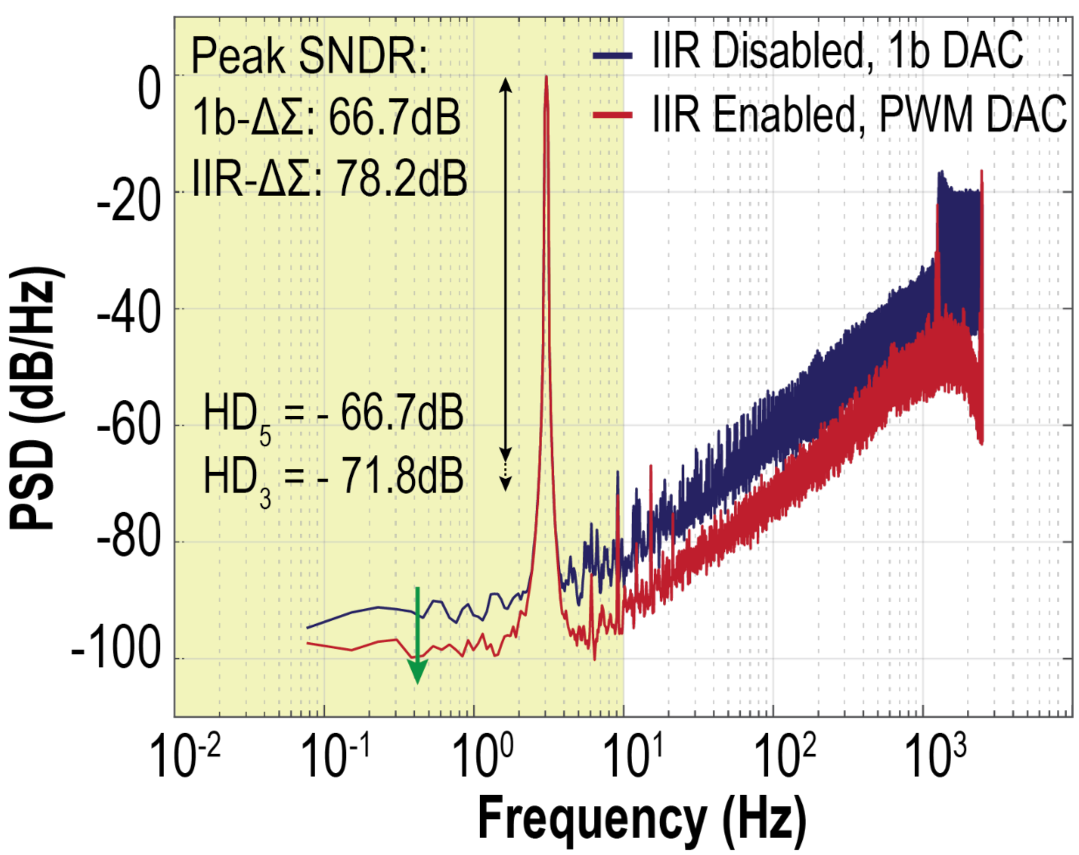
Measurement Results

Input-referred current noise PSD



Capacitive loading → noise ⇧

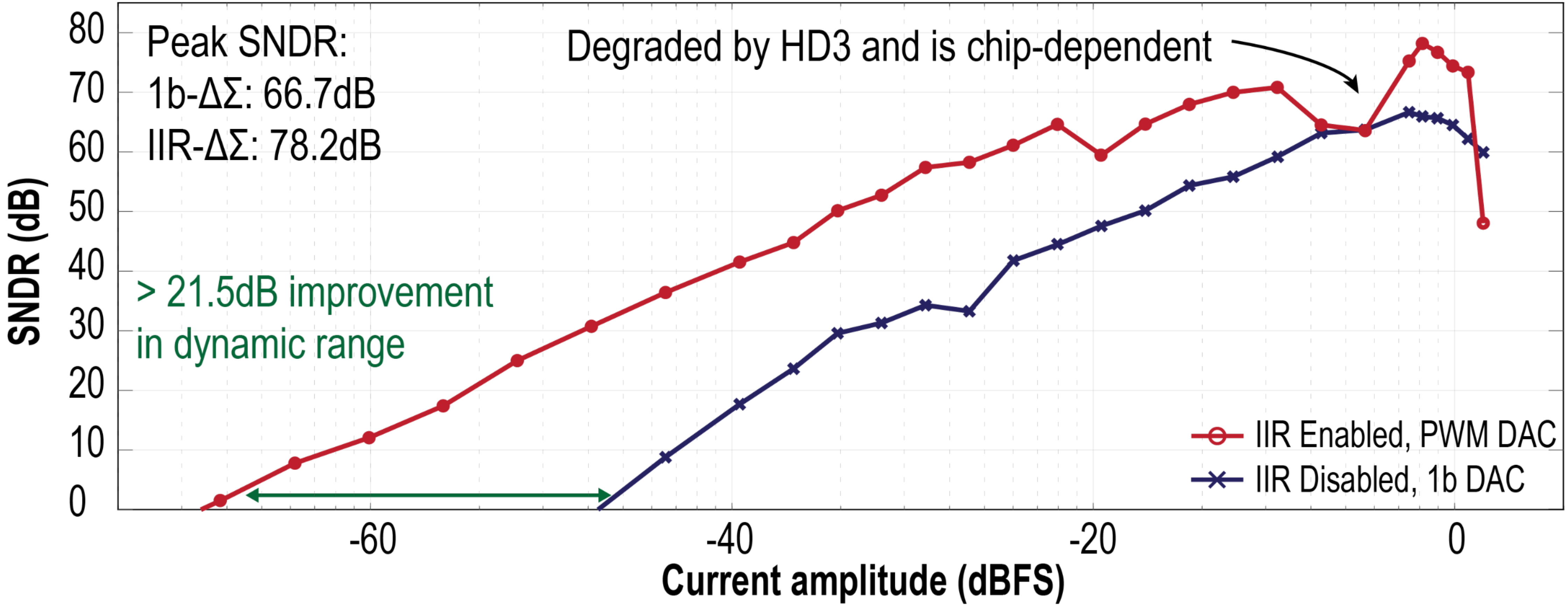
Peak SNDR



123fA sensitivity at 1nA reference

Measurement Results

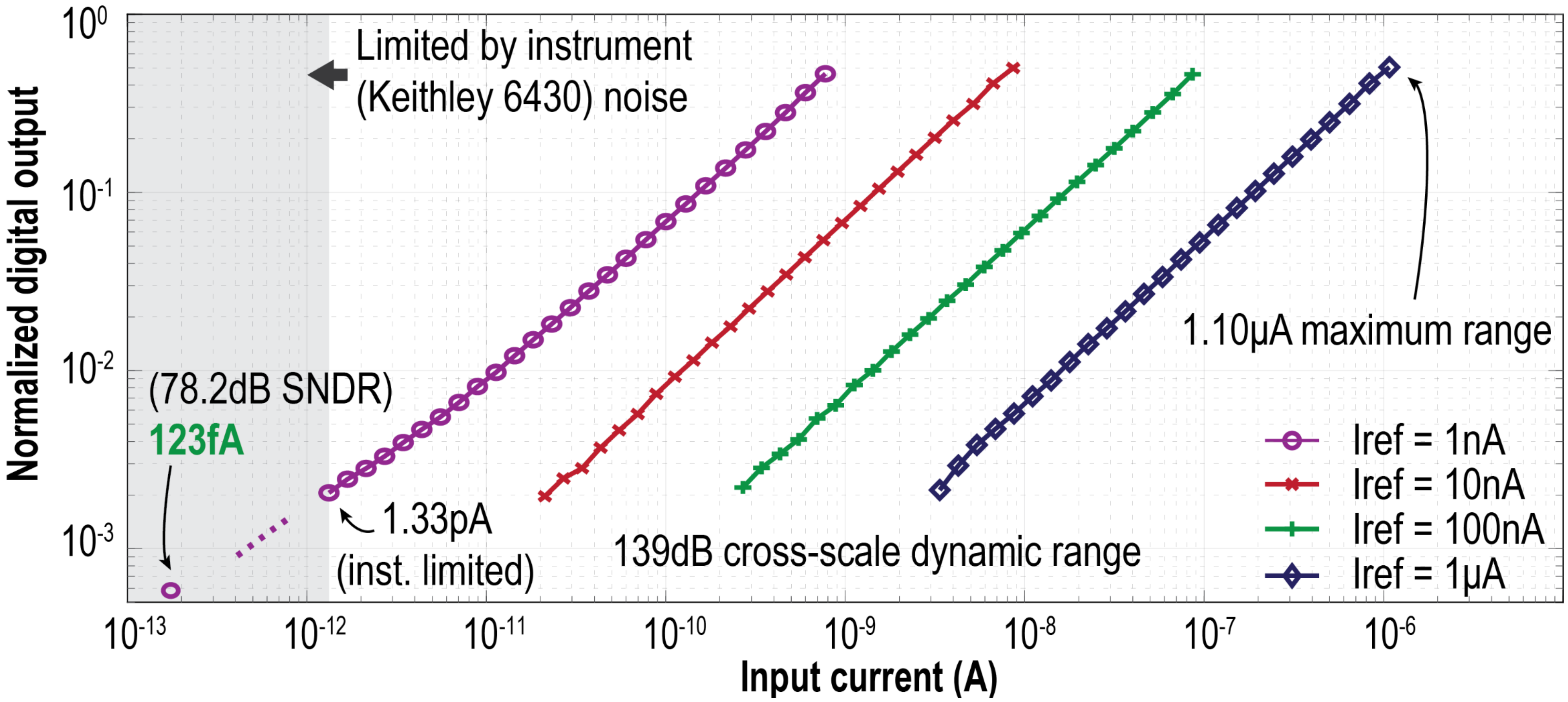
SNDR vs. input amplitude



78.2dB fixed-scale dynamic range

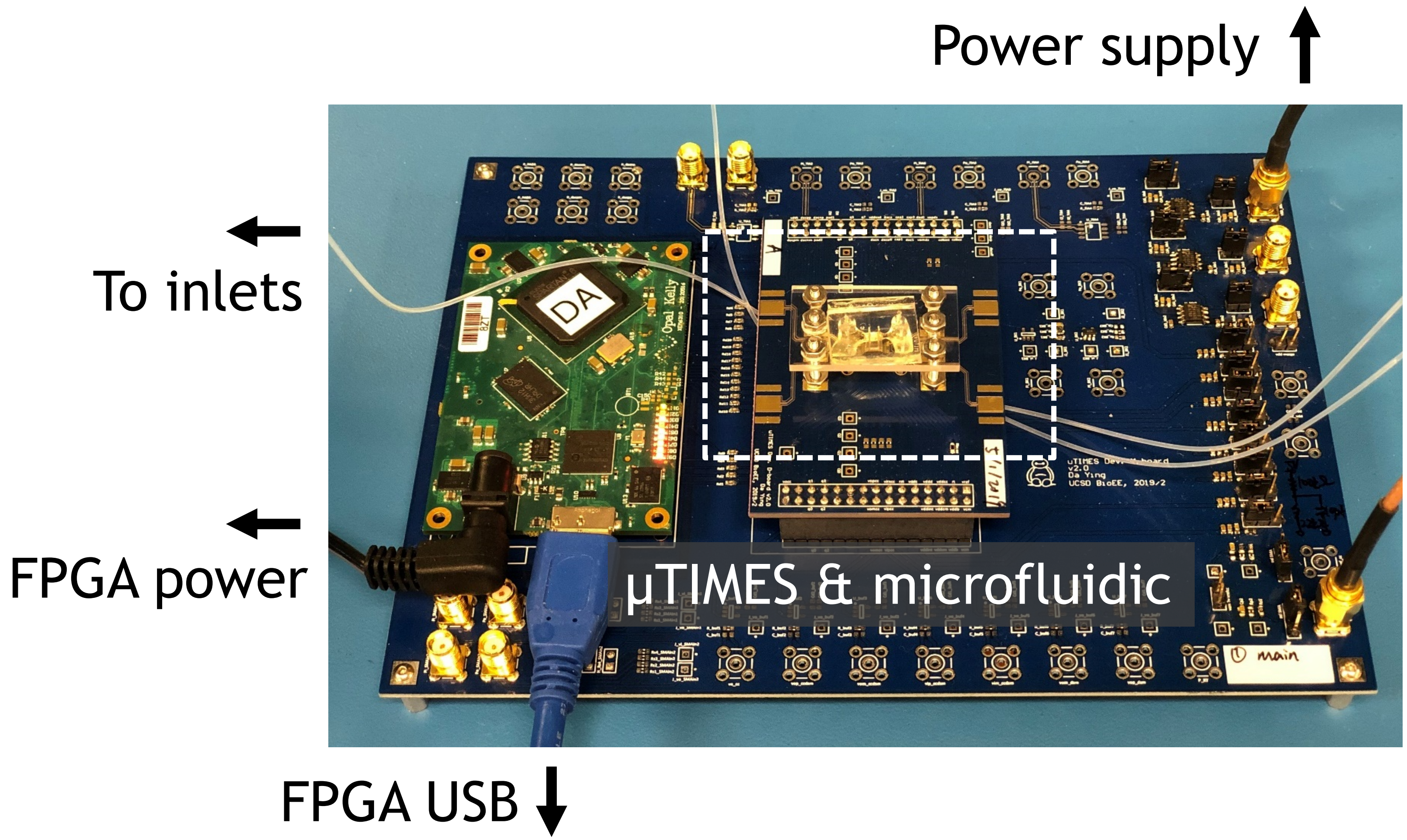
Measurement Results

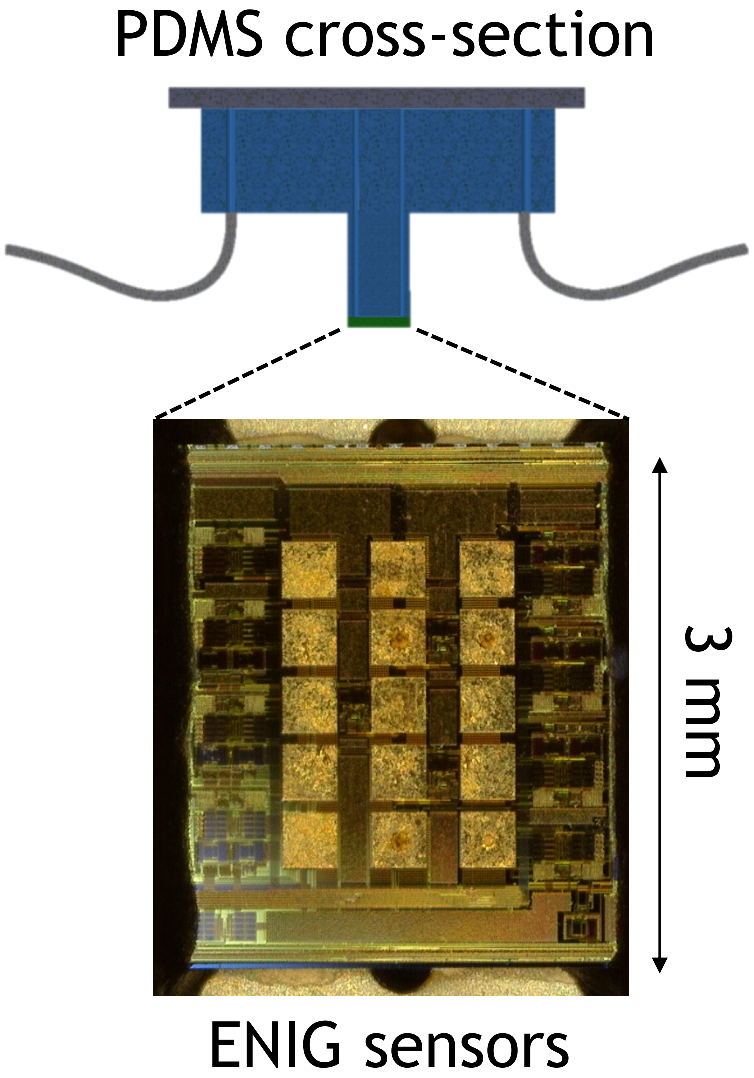
DC input sweep



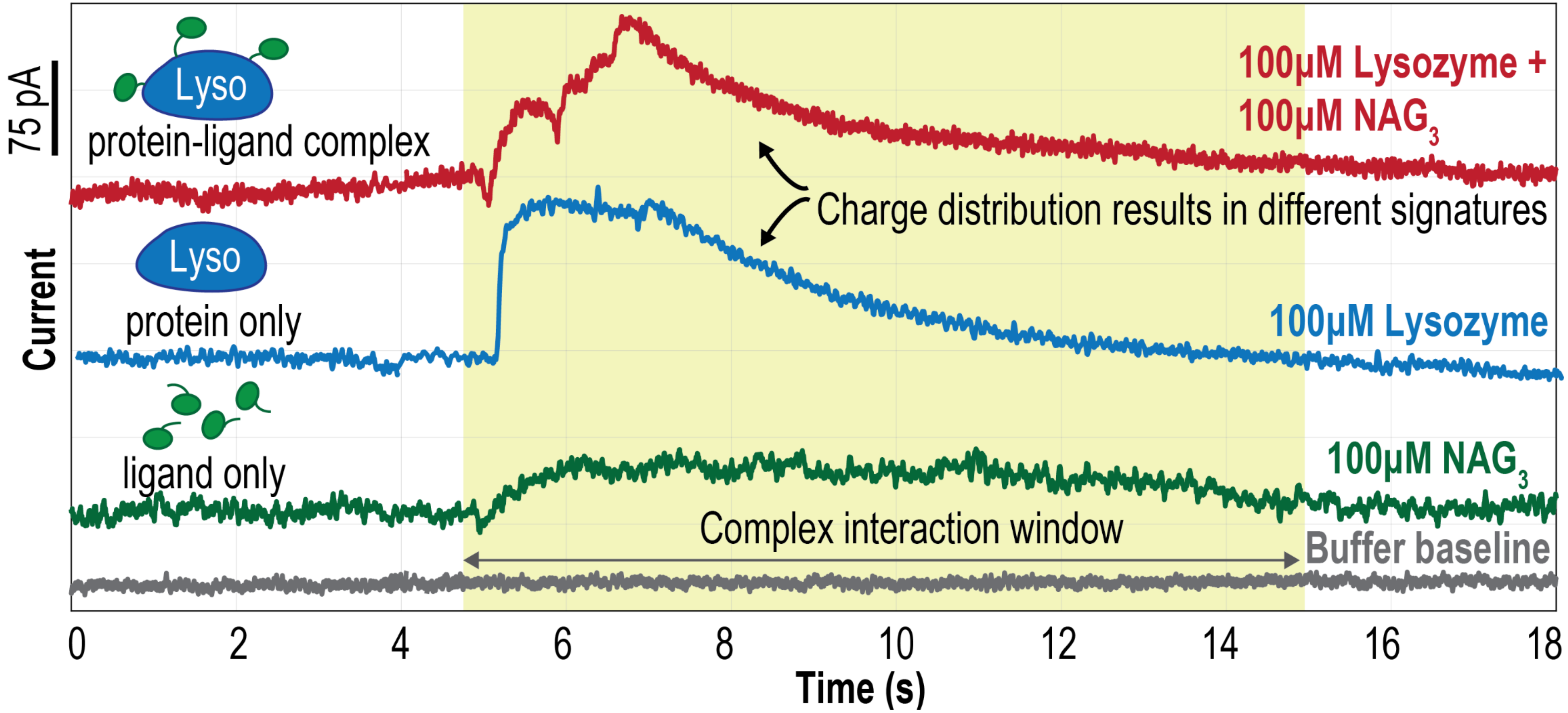
139dB cross-scale dynamic range

TIMES *In-vitro* Measurement Setup





In-vitro Protein-Ligand Measurement



Characteristic shape due to unique dipole moment and charge locality

Performance Summary

	Stanaćević TBCAS'07	Li TBCAS'16	Sim TBCAS'17	Hsu ISSCC'18	Nazari TBCAS'13	**This Work**
AFE Architecture	Inc. ΔΣ	Inc. ΔΣ	ΔΣ	Hourglass ΔΣ	CC + SS ADC	IIR-ΔΣ
Process [μm]	0.5	0.5	0.35	0.18	0.35	0.18
Max Input [μA]	1	16	2.8	10	0.35	1.1
Resolution [fA] @ BW [Hz]	100 @ 0.1	100 @ 1	100,000 @ 10	100 @ 1.8	24,000 @ 100	123 @ 10
Conversion Time @ Min. Input [ms]	8,388	1,000	4	400	10	100
Input-referred Noise [fA/√Hz]	-	-	6,960	58.9	1,850	30.3
Fixed-/cross-scale DR [dB]	40* / 140	54.0* / 164	77.5	160	60.7 / 95	78.2 / 139
On-chip Sensors?	NO	NO	NO	NO	YES	YES
Num. of Channels	16	50	1	1	192	8
Area/ch. [mm^2]	0.25*	0.157	0.5	0.2†	0.04	0.11
Power/ch. [μW]	3.4‡	241	16.8	295	188	50.3

* estimated from figures; † not including synthesized digital area and DEM; ‡ off-chip bias

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Conclusion

Motivation:

- A compact, energy-efficient, high-sensitivity AFE for TIMES biosensing

Techniques:

- Linear prediction in 1st-order CT-ΔΣ achieved by digital IIR filter
- Relaxed hardware complexity with tri-level PWM DAC

Results:

- Low-noise (30.3fA/√Hz)
- High sensitivity (123fA)
- Large dynamic range (78.2dB/139dB)
- Small area ($0.11mm^2$) and low power (50.3μW) per channel

Acknowledgement

- This work was supported in part by the National Science Foundation under Grant ECCS-1610516.

Thank you for your attention!