19.5 A Current-Measurement Front-End with 160dB Dynamic Range and 7ppm INL

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Accurate current measurement is crucial in many biosensing applications, such as the detection of neurotransmitters [1] and the monitoring of intercellular molecular dynamics. This need has become even more critical recently with single-molecule biosensors where sub-pA signal currents are superimposed on a slowly varying nA-to-μA background current, as is the case with nanopores [2]. As such, the readout circuitry requires wide dynamic range (>120dB) and high linearity (>14b) albeit often with low bandwidth (a few Hz to kHz). This paper presents a current measurement front-end using a modified asynchronous ΔΣ modulator architecture that achieves 7ppm INL and 160dB dynamic range (100fA to 10μA) for a state-of-the-art 197dB FoM due to: 1) a continuous-time, oscillator-based Hourglass ADC that asynchronously folds the input signal within the supply, 2) noise shaping to suppress the quantization noise, and 3) a digital linearity correction technique that relaxes the amplifier bandwidth requirement thus reducing power.

Figure 19.5.1 shows a block diagram of the wide-dynamic-range (DR) current-mode analog front-end (AFE) that consists of two main blocks: 1) a 9b predictive, current-steering DAC and 2) an 8b oversampling, asynchronous "Hourglass" ADC. Unlike conventional ΔΣ modulators, the Hourglass ADC can tolerate the entire full-scale input current (10μA), but it does so with reduced linearity as described later. To constrain the input range ($i_{fine} \leq FullScale/2^8$), a digital predictor [3], a first-order digital differentiator with one oversampling cycle delay controls the DAC to generate an approximation of the input signal, i_{coarse}. This approximation is subtracted at the input thus closing the loop. The DAC is implemented using a binary-weighted, tri-state topology to minimize the noise, area, and capacitance at the input node [4]. The DAC mismatch is randomized using a tree-structure, segmented dynamic element matching (DEM) technique [5]. The residual current, i_{fine}, is quantized by the Hourglass ADC that is designed to handle 2× the DAC unit current to tolerate prediction errors and remaining mismatch. The linearity of the Hourglass ADC is further improved from <4b to >8b by a one-time offline calibration routine. The 17b digital code, D_{out}, is obtained by combining the digital outputs of the predictor and the Hourglass ADC.

The core of the Hourglass ADC is an open-loop asynchronous ΔΣ consisting of a capacitive-feedback transimpedance amplifier (C-TIA) in conjunction with an Hourglass switch driven by the outputs of two continuous-time comparators (Fig. 19.5.2). The C-TIA continuously integrates the input current and folds the output voltage within a predefined window, $\pm V_R$, by flipping the polarity of the input signal, i_{fine}, using the Hourglass switch, resulting in a current-to-frequency conversion (*I*-to-*F*). In contrast to a conventional periodically reset C-TIA, the asynchronous folding prevents the C-TIA from saturating by alternating between charging and discharging the feedback capacitors, C_F. Using the input current to charge and discharge C_F removes the need for an explicit DAC. Because the quantization error is retained by not resetting C_F, this structure provides first-order noise shaping. Unlike an asynchronous ΔΣ, which has an asymmetric triangular waveform with a frequency inversely proportional to input amplitude, the C-TIA output is a symmetric triangular waveform with a fundamental frequency ($f_{dir} = i_s/4V_RC_F$) that is linearly proportional to the input amplitude. Due to the high OSR and DAC, the harmonic tones (equivalent to idle tones in a conventional ΔΣ) are guaranteed to be out-of-band and are removed by the decimation filter. A counter accumulates the number of comparator pulses, *cp* and *cn*. Like most oscillator-based quantizers, a digital representation of the signal is obtained by sampling the output of the counter and digitally differentiating at the oversampling frequency, f_{OSR}. This Hourglass structure enables wide dynamic range while simultaneously providing the necessary low input impedance for current measurements.

The linearity of the Hourglass ADC can be understood by examining the output of the C-TIA (Fig. 19.5.3). An ideal triangle wave has an infinite number of odd harmonics, but due to the filtering from the finite bandwidth of the amplifier in the C-TIA, the output waveform is distorted. As the input current is increased, f_{dir} linearly increases resulting in poorer linearity for a fixed-bandwidth amplifier. By bounding the input current with the DAC, the number of harmonics, and thus the linearity of the Hourglass ADC, can be ensured. For 8b linearity, the bandwidth of the amplifier must be at least 52× larger than the maximum f_{dir}. Rather than implementing such a wide-bandwidth (>75MHz), power-hungry amplifier, the linearity is corrected digitally using an amplifier with a bandwidth only 3.2× larger than the maximum f_{dir}. Since the distortion can be precisely expressed once the finite loop gain and bandwidth of the amplifier are known, the calibration routine consists of using the DAC to sweep a subset of the *I*-to-*F* transfer function and fitting with a 5th-order polynomial. This approach results in 16× lower power compared to simply implementing a faster amplifier while ensuring >8b linearity.

A two-stage fully differential amplifier (Fig. 19.5.3) was designed using a dual cascode compensation technique to increase the unity-gain bandwidth with 2× smaller compensation capacitance than the equivalent Miller capacitor and reduce gain peaking beyond the unity-gain frequency. In simulations, the amplifier has >71° phase margin with C_f=100fF and up to 5pF of sensor capacitance. The high DC gain (99dB) in conjunction with autozeroing minimizes the input offset voltage that modulates the sensor current during switching. A low-leakage reset switch was designed using three transmission gates to obtain off-leakage less than 100fA. The Hourglass switch was implemented with transmission gates to minimize charge injection. The comparators consist of a single-stage preamplifier and a latch that is autozeroed during the start-up phase to remove offset. The propagation delay of the comparator is less than 5ns to minimize deadzone time and harmonic distortion caused by excess loop delay.

This AFE was implemented in a 0.18μm CMOS process with a 1.8V supply and 0.5V and 1.3V reference voltages. It was characterized with one of the differential inputs connected to a test source while the other was connected to a matched impedance network. Figure 19.5.4 shows the measured *I*-to-*F* conversion of the Hourglass ADC. The Hourglass ADC INL was improved from >±50ppm to ±7ppm after enabling the calibration where the fitted parameters ($A_{DC,closed\text{-}loop}$=64dB and $f_{closed\text{-}loop}$=1.5MHz) closely match the simulation results. Figure 19.5.4 also shows a spectrum of the Hourglass ADC with f_{0SR}=100kHz illustrating the first-order noise shaping. For a conversion time of 400ms (1.8Hz BW), an input-referred noise of 79fA$_{rms}$ was measured. Figure 19.5.5 shows the full DR of the AFE as the current is swept from 100fA to 10μA (160dB) with a measured linearity of ±7ppm.

This AFE consumes 295μW with the amplifier consuming most of the power (Fig. 19.5.6). For flexibility, the digital logic including the predictor, DEM, and linearity correction were implemented off-chip in an FPGA. Simulation of the synthesized digital logic consumed 8μW. Figure 19.5.6 summarizes the AFE performance in comparison to the state-of-the-art current-input ADCs with similar DR and conversion time. A micrograph of the 1.5×2.0mm^2 chip is shown in Fig. 19.5.7 where the AFE occupies an active area of only 0.2mm^2. In summary, this work achieves state-of-the-art performance in terms of normalized conversion time for a 1nA current (0.04ms) and Schreier FoM (197dB) demonstrating an energy efficient, wide dynamic range, high-linearity design for current input biosensors.

References:

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[3] N. Wood, et al., "Predicting ADC: A New Approach for Low Power ADC Design," *IEEE DCAS*, pp. 1-4, 2014.

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[5] K. L. Chan, et al., "Segmented Dynamic Element Matching for High-Resolution Digital-to-Analog Conversion," *IEEE TCAS-I*, pp. 3383-3392, 2008.

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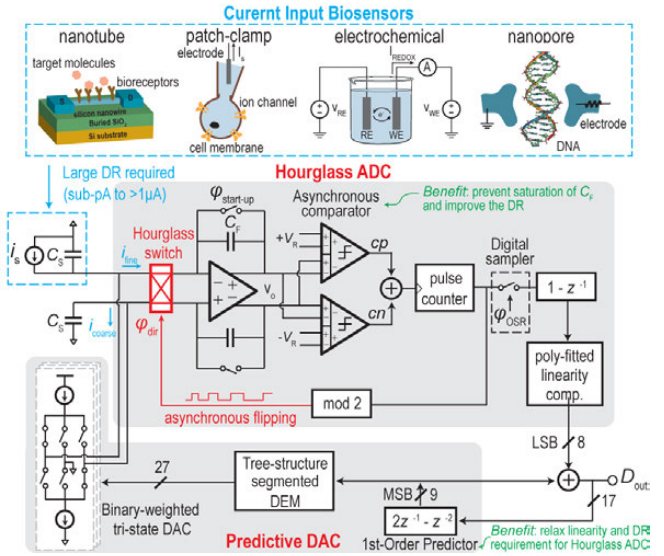


Figure 19.5.1: System architecture of the current measurement front-end.

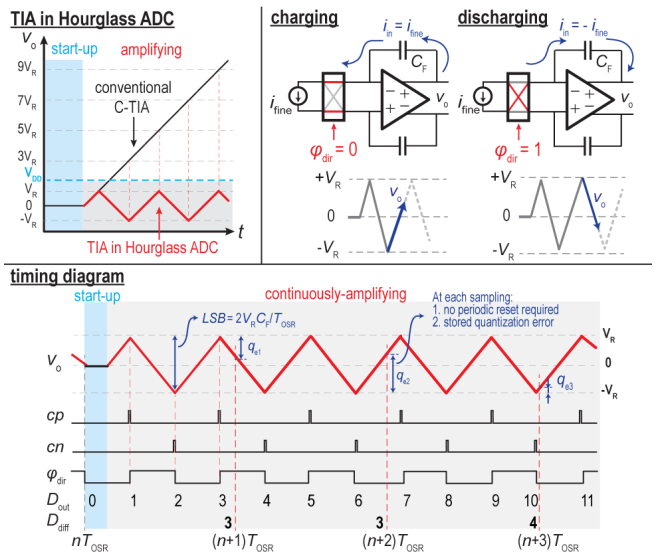


Figure 19.5.2: Operation of the Hourglass ADC.

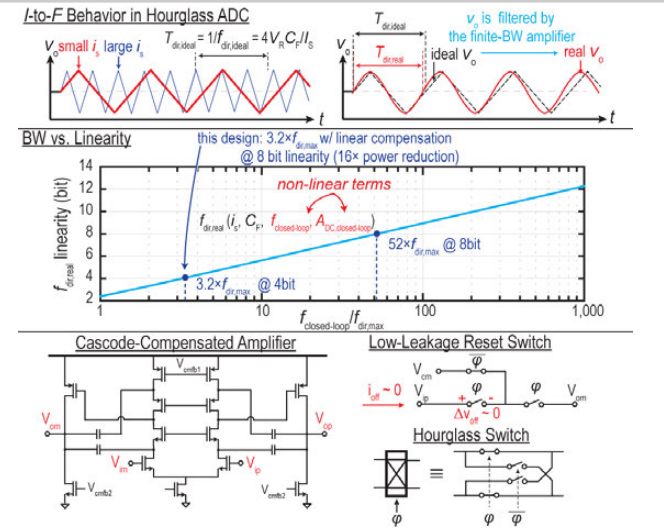


Figure 19.5.3: The *I*-to-*F* behavior and linearity compensation in the Hourglass ADC.

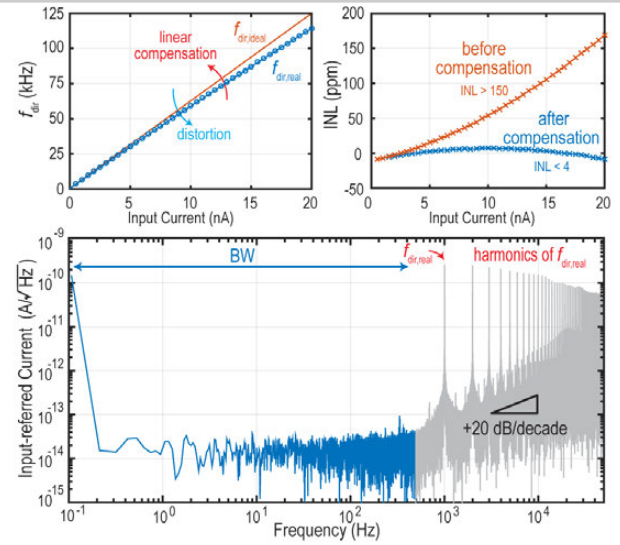


Figure 19.5.4: Measured data showing f_{dir} and INL as a function of the input current and representative spectrum showing noise shaping.

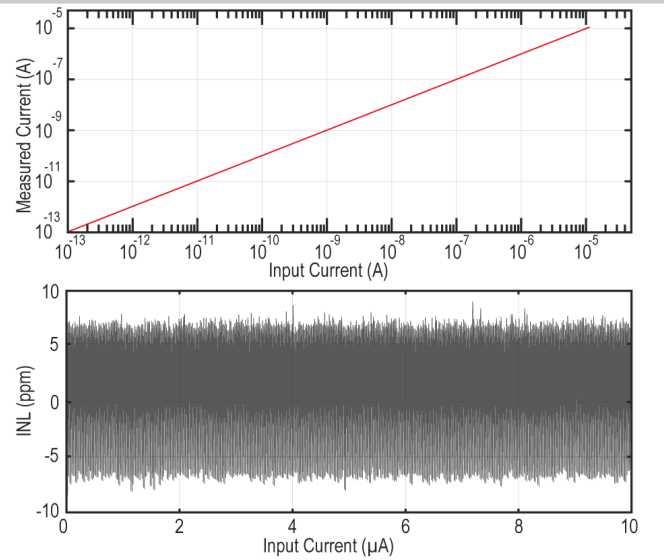
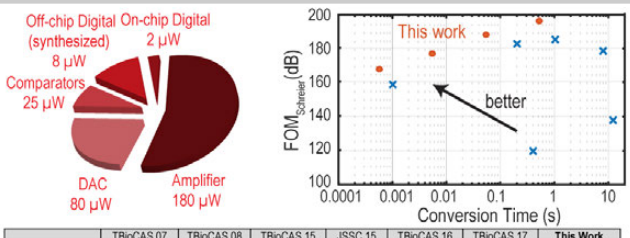


Figure 19.5.5: Measured linearity vs. input amplitude.



	TBioCAS 07	TBioCAS 08	TBioCAS 15	JSSC 15	TBioCAS 16	TBioCAS 17	This Work
Architecture	SDM	SDM	I-to-F	SDM	SDM	SDM	**A-SDM**
Process [μm]	0.5	0.5	0.18	0.18	0.5	0.35	**0.18**
Power [μW]	80	60	5,220	80	240	16.8	**295**
Min Input	100 fA	12 pA	204 fA	1 nA	100 fA	100 pA	**100 fA**
Max Input	1 μA	430 nA	11.6 μA	4 μA	16 μA	3 μA	**10 μA**
Conversion time for Min Input [ms]	8,330	10,000	250	400	1,000	4	**400**
Normalized conversion time for 1nA [ms]	838	120	0.1	400	1	0.4	**0.04**
Max Linearity Error	3.9 nA	3.0 nA	1.16 μA	0.9 nA	1.6 nA	0.1 nA	**70 pA**
Dynamic Range @ BW [dB]	140 @ <0.1Hz	91 @ <0.1Hz	155 @ 1.4Hz	72 @ 2.5Hz	164 @ 1.0Hz	88.9 @ 1 kHz	**100 @ 1.8kHz 120 @ 180Hz 140 @ 18Hz 160 @ 1.8Hz**
FOM$_{Schreier}$ [dB]	172	132	181	103	183	158	**167 @ 1.8kHz 177 @ 180Hz 187 @ 18Hz 197 @ 1.8Hz**

FOM$_{Schreier}$ (dB) = DR(dB) +10log(1/2/T_{conv}/P)

Figure 19.5.6: Performance summary and comparison with previous work.

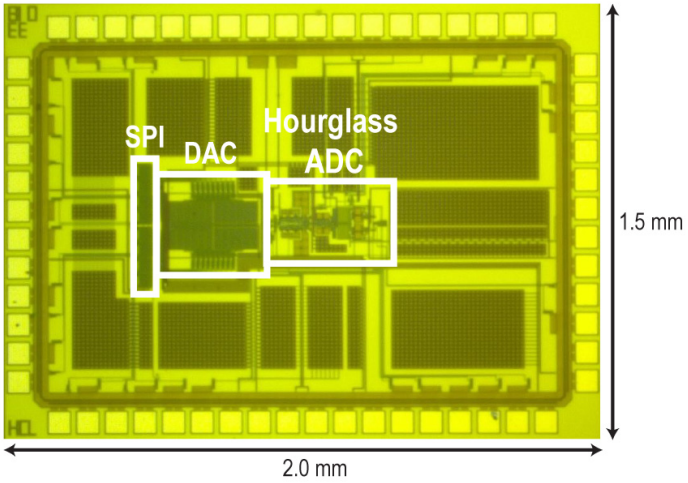


Figure 19.5.7: Die micrograph.

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