A 400 MHz 4.5 nW –63.8 dBm Sensitivity Wake-up Receiver Employing an Active Pseudo-Balun Envelope Detector

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Motivation

- The age of Internet of Everything (IoE)
  - 500 billion connected devices before 2030 [Cisco, 2014]
- Event-driven applications focuses on lifetime and range
  - Low power and high sensitivity are the main targets
Wake-up receiver (WuRX)

- For infrequent event-driven networks:
  - Always-ON WuRX extends system lifetime
  - WuRX sensitivity should be comparable with main RX
State-of-the-art WuRX comparison

Prior-art sub-μW WuRX compromises sensitivity for low power consumption
State-of-the-art nW WuRX

- Direct envelope detection architecture
- 25 dB passive gain enabled by high $R_{in}$ ED

[Jiang, et al., ISSCC’17]
Q1: Could we use the same approach at a higher frequency?
Problem 1: high input capacitance ED

High $C_{in}$ ED limits carrier frequency and passive gain

[ISSCC’17]
Problem 2: single-ended output ED

- Needs extra reference circuit for comparator
  - Extra tuning required for DC variation from PVT
  - Reference circuit is an additional noise source
- Q2: Could we eliminate the reference circuit?

[ISSCC’17]
Proposed WuRX architecture

Diagram showing the proposed WuRX architecture with components labeled such as Boosted SPI, S/H, $g_m$-C preamp, Latch, and various signal processing elements including codebook, 32-bit, 1 bit, 5 bits, 16-bit code, 2x oversampling, Wake-up signal, and output driver.
Proposed WuRX architecture

- Transformer filter
  - 18.5 dB passive gain @ 402~405 MHz MICS band
Proposed WuRX architecture

- Active pseudo-balun CG DTMOS envelope detector
  - Single-ended input to pseudo-differential output
  - Boosted SPI for super cut-off switches
Proposed WuRX architecture

- S/H stage and 2-stage comparator
  - S/H stage solves asymmetric comparator kickback at $\varnothing_2$
Proposed WuRX architecture

- Digital correlator
  - 2× oversampling overcomes clock asynchronization
  - 4 dB coding gain
Maximizing passive voltage gain
Maximizing passive voltage gain

\[ A_V \approx \sqrt{\frac{R_{EQ,P} \| R_{chip}}{R_S}} \]

Requires high-Q passives and a large chip input impedance

E.g.: Assuming \( R_{chip} \to \infty \), 25 dB gain from 50 \( \Omega \) requires \( R_{EQ,P} = 16 \text{ k}\Omega \)
Maximizing passive voltage gain

Objective: under given $f_{RF}$, minimize $(C_S + C_{chip})$ to maximize $L_S$ and therefore passive voltage gain.
Active envelope detector: prior-art

\[
i_{DS} = \mu C_{ox} \frac{W}{L} (n - 1)\phi_t^2 e^{\frac{v_{GS} - V_{th}}{n\phi_t}}
\]

\[
g_{m2} = \frac{1}{2} \cdot \frac{\partial^2 i_{DS}}{\partial v_{GS}^2} = \frac{I_{DS}}{2(n\phi_t)^2}
\]

- [RFIC’12]
- [ISSCC’17]

- High \( R_{in} \) supports high transformer passive gain
- Subthreshold biasing for large 2\(^{nd}\) order non-linearity
- DTMOS configuration provides 16% more \( g_{m2} \)
- High \( C_{in} \) limits frequency and achievable passive gain
Common Source vs. Common Gate ED

- **Problem:**
  - High $C_{in}$, fixed $V_{th}$

- **Benefit:**
  - Low $C_{in}$, tunable $V_{th}$

- **Common gate input eliminates $C_{gd}$ and $C_{bd}$**
  - Saves 47.5% $C_{in}$ based on simulation

- **Extra freedom on bulk bias voltage and $V_{th}$ is tunable**
  - DTMOS advantage retained (16% extra $g_{m2}$)
Active pseudo-balun CG ED

Current reuse

Secondary coil of transformer filter

$V_{in}$

$V_{out,n}$

$V_{out,p}$

$Z_{out,n}$

$Z_{out,p}$

$C_{BLK}$

$L_S$

NMOS

PMOS
Active pseudo-balun CG ED

Transformer reused as AC GND
Active pseudo-balun CG ED

$Z_{out,n}$

$g_{m1,n}v_{in}Z_{out,n}$

$1^{st}$ order linear RF current

$g_{m1,p}v_{in}Z_{out,p}$

RF signal in phase and filtered out

$V_{in}$

$C_{BLK}$

$L_S$

$V_{out,n}$

$V_{out,p}$
Active pseudo-balun CG ED

\[ Z_{out,n} \]

**2\textsuperscript{nd} order non-linear BB current**

\[ -g_{m_{2,n}}v_{in}^2Z_{out,n} \]

**BB signal out of phase**

\[ g_{m_{1,p}}v_{in}^2Z_{out,p} \]
Active pseudo-balun CG ED

2\times \text{signal voltage}
2\times \text{noise power}
1.5 \text{ dB sensitivity improvement}

Pseudo-differential output
Reference circuit eliminated

\begin{align*}
Z_{\text{out},n} & \rightarrow -g_{m2,n}v_{\text{in}}^2Z_{\text{out},n} \\
V_{\text{out},n} & \rightarrow 2^{\text{nd order non-linear BB current}} \\
Z_{\text{out},p} & \rightarrow g_{m1,p}v_{\text{in}}^2Z_{\text{out},p}
\end{align*}
Proposed pseudo-balun ED schematic

- Active-inductor biasing as output load
  - High $R_{out}$ and thus high conversion gain

- Binary-weighted tuning cells for PVT

- Larger transistors to further reduce $1/f$ noise
  - Less $C_{in}$ penalty compared to CS input

- $1.8$ nW; $k_{ED} = 301.2(1/V)$
GF 180 nm CMOS SOI process
RO4003 substrate
- Input $S_{11}$ well matched across MICS band
- ED pseudo-differential output waveforms
-63.8 dBm sensitivity for MDR ≤ 10⁻³

>–20 dBm CW and >–50 dBm PRBS jammers could be tolerated @ 50 MHz offset w/o false alarm
## Comparison to the state-of-the-art

<table>
<thead>
<tr>
<th></th>
<th>RFIC’12</th>
<th>ISSCC’16</th>
<th>ISSCC’17</th>
<th>CICC’13</th>
<th>This work</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Technology</strong></td>
<td>130 nm</td>
<td>65 nm</td>
<td>180 nm</td>
<td>130 nm</td>
<td>180 nm</td>
</tr>
<tr>
<td><strong>Supply</strong></td>
<td>1.2 V</td>
<td>1 / 0.5 V</td>
<td>0.4 V</td>
<td>1.2 / 0.5 V</td>
<td>0.4 V</td>
</tr>
<tr>
<td><strong>Data Rate</strong></td>
<td>100 kbps</td>
<td>8.192 kbps</td>
<td>0.3 kbps</td>
<td>12.5 kbps</td>
<td>0.3 kbps</td>
</tr>
<tr>
<td><strong>Passive Gain</strong></td>
<td>12 dB</td>
<td>N/A</td>
<td>25 dB</td>
<td>5 dB</td>
<td>18.5 dB</td>
</tr>
<tr>
<td><strong>ED Type</strong></td>
<td>Active CS single-ended</td>
<td>Passive Dickson single-ended</td>
<td>Active CS single-ended</td>
<td>Passive Dickson single-ended</td>
<td>Active CG pseudo-balun</td>
</tr>
<tr>
<td><strong>ED Power</strong></td>
<td>23 nW</td>
<td>0</td>
<td>2.1 nW</td>
<td>0</td>
<td>1.8 nW</td>
</tr>
<tr>
<td><strong>ED $R_{\text{in}}$ @ RF</strong></td>
<td>505.6 Ω</td>
<td>N/A</td>
<td>10 kΩ</td>
<td>76.3 Ω</td>
<td>30 kΩ</td>
</tr>
<tr>
<td>$k_{\text{ED}}$ (1/V)</td>
<td>112.2</td>
<td>N/A</td>
<td>180.8</td>
<td>N/A</td>
<td>301.2</td>
</tr>
<tr>
<td>$k_{\text{ED}}/P_{\text{ED}}$ (1/V·nW)</td>
<td>4.9</td>
<td>N/A</td>
<td>86.1</td>
<td>N/A</td>
<td>167.3</td>
</tr>
<tr>
<td><strong>Comp. Ref.</strong></td>
<td>ED replica</td>
<td>RC LPF</td>
<td>Ref. ladder</td>
<td>N/A</td>
<td>None</td>
</tr>
<tr>
<td><strong>Carrier Freq.</strong></td>
<td>915 MHz</td>
<td>2.4 GHz</td>
<td>113.5 MHz</td>
<td>403 MHz</td>
<td>405 MHz</td>
</tr>
<tr>
<td><strong>Sensitivity</strong></td>
<td>–41 dBm</td>
<td>–56.5 dBm</td>
<td>–69 dBm</td>
<td>–45 dBm</td>
<td>–63.8 dBm</td>
</tr>
<tr>
<td><strong>RX Power</strong></td>
<td>98 nW</td>
<td>236 nW</td>
<td>4.5 nW</td>
<td>116 nW</td>
<td>4.5 nW</td>
</tr>
</tbody>
</table>
Comparison to WuRXs ($f_{RF}>400$ MHz)

- **FoM (dB)**: $-P_{\text{SEN,norm}} - 10\log(P_{\text{DC}}/1\text{mW})$
- Best FoM among direct-ED based WuRXs

\[ P_{\text{SEN,norm}}: \text{[Daly, et al., JSSC'10]} \]
Comparison to WuRXs ($f_{RF}>400$ MHz)

Some mixer-based WuRXs have better FoM, albeit at much higher DC power
Conclusions

- For event-driven applications with low-average throughput, WuRXs extend system lifetime
  - Design targets: Low power and high sensitivity
- The proposed design breaks the trade-off between sensitivity and carrier frequency by using:
  - Active ED with CG input to reduce input capacitance
  - Current-reuse pseudo-balun ED to improve 1.5 dB sensitivity without a power penalty
- Result:
  - A 400 MHz, 4.5 nW, –63.8 dBm sensitivity WuRX
Acknowledgment

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