A 2-in-1 Temperature and Humidity Sensor Achieving 62 fJ·K^2 and 0.83 pJ·(%RH)^2

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***Abstract*—This paper presents the first reported CMOS 2-in-1 relative humidity (RH) and temperature (Temp) sensor. A unified analog front-end (AFE) interfaces two on-chip transducers and converts the resistance (α Temp) and capacitance (α RH) into a frequency. This conversion occurs with high linearity (±10 ppm error) across the industrial temperature range (-40 to +85 °C) via a frequency-locked loop (FLL). An incomplete-settling switched-capacitor (SC)-based Wheatstone bridge (WhB) is proposed to sense the *R* and *C* in a power-efficient fashion. The FLL output is digitized by a low power, time-to-digital converter (TDC) that has high resolution due to the inherent quantization noise-shaping. This system achieves excellent resolution figure-of-merits (FOMs) when normalized to RH (0.83pJ·(%RH)^2) and temperature (62 fJ·K^2).**

I. Introduction

Environmental conditions play an important role in human well-being, comfort, and productivity. Temperature and humidity are common measurements in weather stations, agricultural monitors, and perishable food sensors [1] where such applications are often distributed and ideal Internet-of-Things (IoT) sensors. To integrate this sensing capability with battery-powered IoT nodes, the measurement circuitry must be low-power (<20 nJ/meas.) and operate from a wide range of supply voltages. Conventional RH/Temp sensors use separate AFEs and digitize the signals in a time-multiplexed fashion (Fig. 1) resulting in high power consumption (e.g., >300 nJ/meas. in [2]) precluding use in IoT applications.

This paper presents an integrated RH/Temp sensor consisting of a resistor-based temperature transducer (silicided poly-resistor) and a capacitor-based humidity transducer (exposed top-metal finger capacitor coated with a polyimide film). Both transducers are CMOS compatible and integrated on-chip. We propose a 2-in-1 resistance- and capacitance-to-time (*R*&*C*-to-*T*) front-end that eliminates the need for two distinct AFEs. The *R*&*C*-to-*T* conversion is achieved in a low power manner via a FLL that suppresses the nonlinearity and PVT variation from the voltage-controlled oscillator (VCO) to ensure high-linearity conversion. Within the loop, the time-to-voltage conversion is realized by an incomplete-settling SC-based WhB (Fig. 1). Compared to prior work (frequency reference and capacitance-to-digital converter) employing a SC-based circuit, the proposed architecture requires no active circuits to drive the SC front-end (e.g., an LDO-based voltage source [3] or a high bandwidth closed-loop integrator [4]) to achieve low settling error (i.e., <½ LSB). However, due to the absence of an active driver, incomplete-settling is inevitable in

This work was supported in part by equipment purchased through a DURIP award from the Office of Naval Research (award no. N00014-18-1-2350).

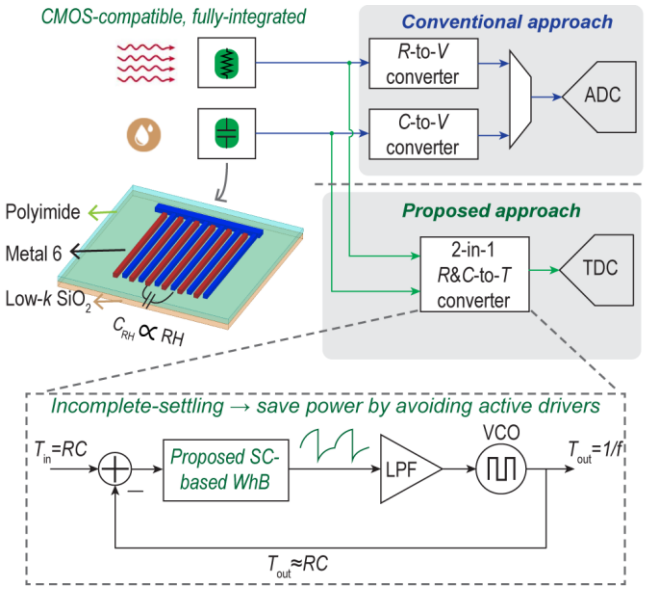

Fig. 1. Architecture of the 2-in-1 temperature and relative humidity sensor.

the proposed circuit. This work demonstrates that by adding a charge-preserving capacitor and sizing it appropriately, the incomplete-settling SC circuit still exhibits high accuracy (<10 ppm error) at a lower power consumption than prior art. Furthermore, the WhB provides high immunity to supply variation (0.12 °C/V or 0.43 %RH/V) across a wide supply range (1.5 to 2 V), which is needed in battery-powered IoT sensors. With this technique, the proposed RH/Temp sensor achieves state-of-the-art RH sensitivity (0.0073 %RH) and high temperature sensitivity (2 mK) while consuming only 15.6 pJ/meas. – 20× lower than commercial RH/Temp sensors [2].

The rest of the paper is organized as follows: the incomplete-settling SC-based WhB concept is analyzed in Section II followed by the implementation of the system and circuits in Section III. Section IV presents measurements results followed by a conclusion in Section V.

II. Incomplete-Settling SC-Based WhB

The *R*&*C* sensing circuit is critical to the performance as it sets the overall sensitivity and accuracy in both modes of operation. Prior work on temperature sensors, frequency references, and capacitance-to-digital converters has demonstrated three ways of implementing such a circuit. The bandpass-filter-based method, utilizing either a Wien bridge or a poly-phase filter [Fig. 2(a)], has been used for resistor-based

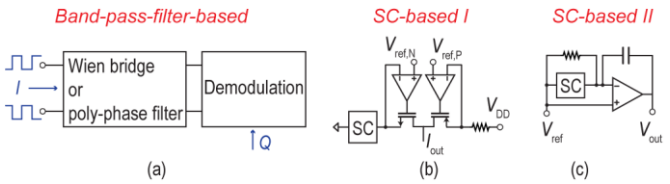

Fig. 2. Prior work that could be used for *R*&*C* sensing, based on (a) a band-pass-filter, (b) a SC resistor and LDO, and (c) a SC integrator.

temperature sensors [5]–[7] and could be modified for capacitive humidity sensing since the bandpass filter also contains capacitors; however, the parasitic capacitance and mismatch would lower the Q and degrade the sensitivity. Furthermore, floating capacitors are required and difficult to shield without adding significant parasitic capacitance. This method is also sensitive to the in-band supply noise. In another approach [Fig. 2(b)], two matched, LDO-based voltage sources with one driving a resistor and the other a SC resistor has been reported [3]. The two output currents are balanced when the resistance of the SC resistor is matched with the resistor. This requires only one resistor and one capacitor (not floating) but needs two active voltage sources and two references that add noise and power overhead. An alternative SC-based method is combined with a charge-balancing ΔΣ modulator as shown in Fig. 2(c), where the SC circuit is driven by a closed-loop integrator [4]. Since the integrator needs to charge and discharge the capacitor during every clock cycle, the amplifier must have much higher bandwidth than the switching frequency to settle. Furthermore, it also requires a reference with low output impedance to drive the other end of the SC that also adds power overhead.

To address these issues, this paper proposes a SC-based WhB for *R*&*C* sensing based on the previous SC method but avoiding the need for LDO-based voltages sources or high bandwidth integrators utilizing incomplete-settling for power savings. In one branch of the WhB, a capacitor C switched at frequency f is connected to a voltage source V_s via a series resistor R. It should be noted that, unlike the well-known SC resistor where the charge transfer function is based on complete-settling, V_A doesn't settle completely to V_s due to the large RC time constant. For example, when the clock period is the same as the RC time constant (i.e., f=1/RC), the SC resistance is off by ~5.2%. The settling error is sensitive to parasitic capacitance and clock uncertainty, so it cannot be easily calibrated out across PVT variation. Instead of building a power-hungry driving circuit to minimize the settling error, we propose a passive method where a capacitor C_f is added to preserve the charge for the SC operation [Fig. 3(a)]. The waveform at V_A and the two-phase clock are shown in Fig. 3(b). The voltage at node A at the end of the two clock phases, $V_{A,1}$ and $V_{A,2}$, is

$$V_{A,1} = V_{DD} + (V_{A,2} - V_s)e^{-\frac{T_1}{RC_f}}, \quad (1)$$

$$V_{A,2} = V_{DD} + \left(\frac{C_f}{C+C_f}V_{A,1} - V_{DD}\right)e^{-\frac{T_2}{R(C_f+C)}}, \quad (2)$$

where T_1 and T_2 are the period of the two phases. During each cycle, the charge, Q, being transferred is $CV_{A,2}$. Therefore, the steady-state voltage of node A, $V_{A,ss}$, is

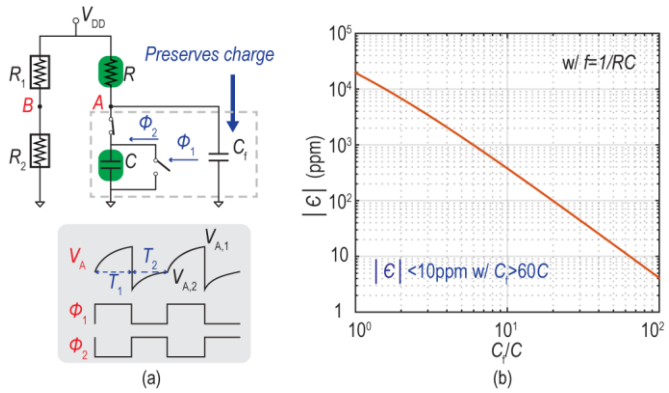

Fig. 3. (a) Proposed incomplete-settling SC-based WhB circuit and waveforms, and (b) $|\epsilon|$ vs. C_f/C.

$$V_{A,ss} = V_{DD} - \frac{RQ}{T_1+T_2}. \quad (3)$$

With f=1/RC, substituting (1-2) into (3), $V_{A,ss}$ is

$$V_{A,ss} = (1+\epsilon)\frac{1}{1+fCR}V_{DD} \approx \frac{1}{1+fCR}V_{DD},$$
$$\text{where } \epsilon = 1.5\left(1 - \frac{1}{\frac{C_f+C}{C}e^{\frac{C}{C+C_f}} - \frac{C_f}{C}e^{-\frac{C}{C_f}}}\right) - 1. \quad (4)$$

Eqn. (4) shows that the right branch of the WhB in Fig. 3(a) is approximately a voltage divider consisting of R and a SC resistor whose resistance is 1/fC. ϵ is a parameter that evaluates the error in the approximation. Based on calculations, ϵ becomes negligible (<10 ppm) when the capacitor C_f is >60C [Fig. 3(c)]. This result indicates that the incomplete-settling SC resistance approaches 1/fC and $V_{A,ss}$ approaches V_{DD}/(1+ fCR) when C_f is large enough. Note, without C_f power hungry active drivers are required to achieve the same result. Thus, despite incomplete settling, the WhB is balanced when f=1/RC and R_1 matches R_2. Adding C_f (=60C) improves the SC accuracy by ~5,200× without a power penalty during steady-state. The reason to choose R_1=R_2 therefore resulting in f=1/RC are: 1) The WhB sensitivity is maximized when $V_{A,ss}$=$V_{DD}/2$, and 2) It is more convenient to design a readout circuit with the input common-mode voltage at $V_{DD}/2$.

This technique has several benefits, namely: 1) High sensitivity and inherent supply rejection due to the differential structure. 2) Insensitivity to the parasitic capacitance at the outputs of $V_{A,B}$ and variation of C_f since C_f is already large. Thus, C_f can be implemented with a MOS capacitor to save area. 3) R_1 and R_2 only need to be matched to each other and thus can be implemented with pseudo-resistors consuming little power and area provided that the mismatch is constant over temperature, which introduces a gain error that can be calibrated out. 4) Due to incomplete-settling and large C_f, the swing at V_A is <1 mV, which relaxes the readout circuit linearity requirement. Switching imperfections (e.g., clock feedthrough and charge injection) are attenuated by C_f.

III. System and Circuit Implementation

A. System Architecture

The system architecture is shown in Fig. 4. Within the FLL, two SC cells (a MIM capacitor C for reference and a polyimide

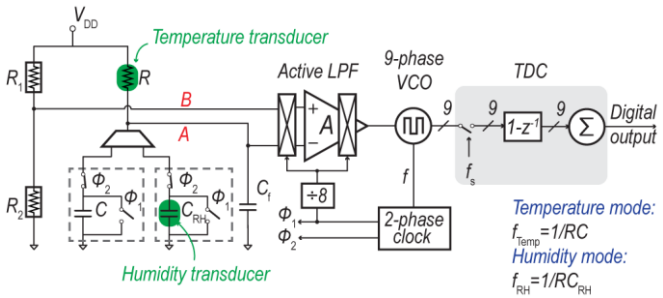

Fig. 4. System architecture of the 2-in-1 RH/Temp sensor.

film capacitor C_{RH} for humidity sensing) are connected to the bridge via a multiplexer and a silicided poly-resistor is used for temperature sensing. C_{RH} is realized using a top metal finger capacitor with an open-passivation window. Metals 4-5 are connected to ground and used to guard against over etching and to limit the parasitic capacitance to <1.5%. The bridge outputs, $V_{A,B}$, are fed into an active lowpass filter (LPF), which sets the loop dominant pole. The LPF is chopped to remove temperature-dependent offset and the amplifier's $1/f$ noise. A VCO converts the amplified and filtered WhB output voltage into a frequency signal. A 2-phase non-overlapping clock generator closes the loop by feeding back the frequency to the SC cells. In the temperature measurement mode, $f_{Temp}=1/RC$, whereas in RH mode $f_{RH}=1/RC_{RH}$. R is nominally ~330 kΩ and both capacitors are ~4 pF resulting in a 750 kHz oscillation frequency. C_f is implemented with a MOS capacitor (~250 pF). Values were chosen to balance the noise, power consumption, and area.

B. Chopper-Stablized Active Filter

Since the system linearity requirement is relaxed by the FLL and low swing at V_A, the active filter is implemented with an open-loop g_m-C filter rather than a closed-loop integrator to minimize the power consumption. To ensure high loop gain, the amplifier uses a telescopic architecture with >80 dB dc gain across process corners and the entire temperature range [Fig. 5(a)]. The FLL loop gain is greater than 92 dB, which ensures a linearity error of no more than ±10 ppm from -40 to 85 °C [Fig. 5(b)]. The residual nonlinearity comes from the incomplete-settling error and the VCO nonlinearity.

The amplifier offset, which is temperature-dependent, adds directly at the WhB output and creates an error. A chopper technique is adopted to address this and attenuate the amplifier $1/f$ noise resulting in a 6× amplifier noise reduction. The chopper is clocked by the FLL output divided down to reduce the amplifier bandwidth by 8 (<100 kHz) resulting in 8× power savings. The input transistors are biased in subthreshold while the load transistors are biased in saturation. Combined with the chopping, this amplifier achieves a noise efficiency factor (NEF) of 2.4. This makes the SC-based WhB the dominant noise source. The down modulators are placed at the cascode nodes that have higher bandwidth and lower impedance than the output. The loop filter capacitor, C_o, also attenuates the chopper ripple.

C. VCO & TDC

As shown in Fig. 5(c), the VCO is implemented with a 9-stage g_m-current-controlled oscillator (g_m-CCO), which has 3× better voltage-to-frequency linearity than directly voltage-

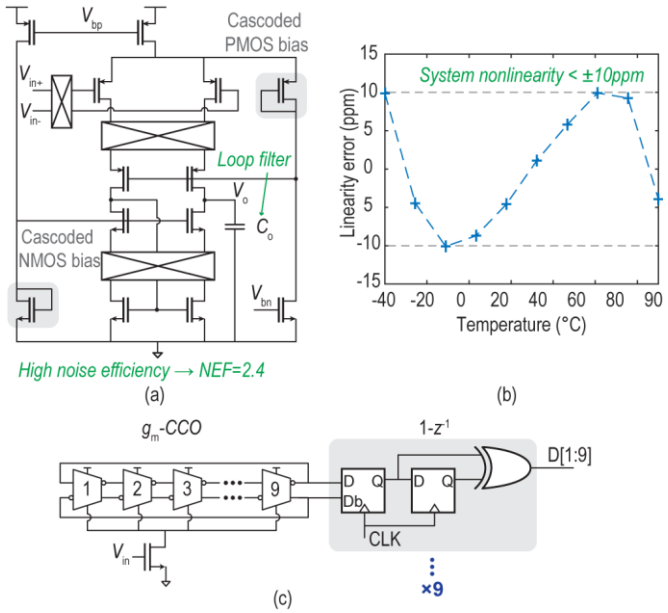

Fig. 5. (a) Schematic of the g_m-C filter, (b) simulated system linearity over temperature, and (c) schematic of the VCO and TDC.

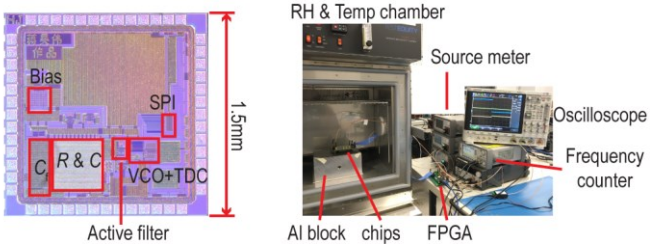

Fig. 6. Die photo and photograph of the measurement setup.

controlling each stage based on simulation. A larger number of stages leads to a lower $1/f$ noise but incurs higher power consumption for a given oscillation frequency. We chose 9 stages to ensure that the VCO is the least dominant noise source. Nine DFFs sample and quantize the VCO phase and another group of DFFs and XORs perform the $1\text{-}z^{-1}$ operation to recover the frequency information while also first-order shaping the quantization noise [8]. Since the FLL output frequency is less than 1 MHz across the target RH/Temp range, a 2 MHz sampling rate was chosen guaranteeing >116 dB SQNR, which is sufficient for RH/Temp measurements.

IV. Measurement Results

The circuit was fabricated in a 180 nm CMOS process and consumes 15.6 µW from a 1.5 V supply, where the active filter consumes 52%, the WhB 22%, and the VCO/digital circuits 26%. The active area is 0.72 mm^2, where the RH transducer takes 0.21 mm^2 (Fig. 6). The decimation filter was implemented off-chip in an FPGA for flexibility and would consume 0.4 µW and 0.002 mm^2 if implemented on-chip. Polyimide (PI-2545) was dropcast and spin coated on the surface of the chip followed by a 5-hour curing. Note this step can be done by the foundry on non-shared multi-project wafers.

To minimize the noise contribution from ambient temperature and humidity, the sensors were mounted on an aluminum block and put in a RH/Temp chamber. Fig. 7

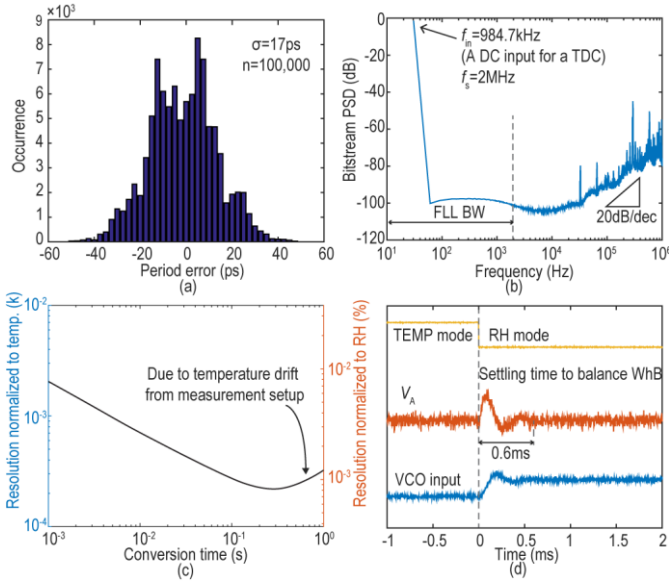

Fig. 7. Measured (a) FLL jitter, (b) PSD of the bitstream, (c) resolution vs. conversion time, and (d) transient waveforms during mode switching.

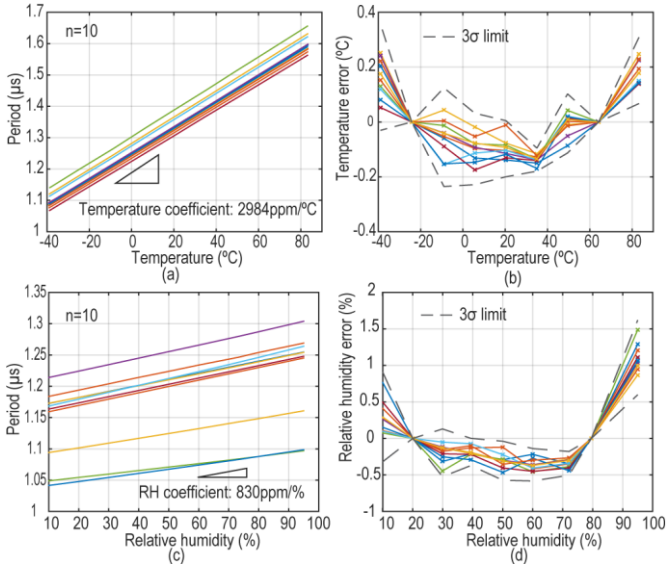

Fig. 8. Measured (a) temperature transfer curve, (b) temperature error, (c) RH transfer curve, and (d) RH error.

summarizes the measurement results. The measured jitter of 100,000 cycles was 17 ps_{rms} (12 ppm). The spectrum of the bitstream was measured when the oscillation frequency was 984.7 kHz by fixing the temperature and RH. The sampling clock was generated externally as in [5]–[7]. The RH/Temp resolution is plotted against conversion time where a 2 mK or 0.0073 %RH resolution was achieved in 1 ms. A transient waveform shows the FLL resettles after 0.6 ms when switching measurement modes. The sensors were 2-point trimmed to remove offset and gain error. The measured temperature and RH coefficients are ~2,980 ppm/°C and ~830 ppm/%, respectively, and match closely with the simulation (Fig. 8). The relatively large spread in the RH transfer curves was likely caused by variations in the post-processing. Fig. 8 shows the RH/Temp errors after calibration. The temperature dependence in the RH

TABLE I
PERFORMANCE COMPARISON OF TEMP AND HUMIDITY SENSORS

	Parameter	[5]	[7]	S.Pan ISSCC'18	[6]	[1]	A. Boni ICECS'14	This Work
System	Tech. (nm)	180	180	180	65	160	180	**180**
	Sensor type	Temp	Temp	Temp	Temp	RH	RH	**RH & Temp**
	Active area (mm^2)	0.09	0.72	0.25	0.007	0.28	0.1[3]	**0.72**
	Supply (V)	1.7/1	1.6~2	1.6~2	0.85~1.05	1.2	1.1	**1.5~2**
	Conversion time (ms)	32	10	5	1	0.8	15	**1**
	Power (µW)	31	180	94	68	10.3	2	**15.6**
Temp. sensor	Temp. range (°C)	-40~85	-40~85	-55~125	-40~85	25 only	10~20	**-40~85**
	3σ error (K) [trim points]	0.12[3]	0.1[4][2]	0.12[4] [2]	0.7[2]	-	-	**0.55[2]**
	Resol. (mK)	2.8	0.16	0.26	2.8	-	-	**2**
	FOM[1]($fJ·K^2$)	8,000	49	32	530	-	-	**62**
RH sensor	RH range (%)	-	-	-	-	30~95	10~80	**10~95**
	3σ error (%) [trim points]	-	-	-	-	NA[2]	7.5[2]	**2.2[2]**
	Resol. (%RH)	-	-	-	-	0.05	0.5	**0.0073**
	FOM[1]($pJ·\%^2$)	-	-	-	-	20.75	$3.3×10^7$	**0.83**

[1] Energy / conversion × (temp. resol.)^2
[2] Energy / conversion × (RH resol.)^2
[3] Used off-chip RH transducer
[4] Used high order nonlinearity correction

mode is removed by calculating f_{RH}/f_T and normalizing C_{RH} to C. Varying the supply from 1.5 to 2 V at room temperature, the sensor output changes by 0.018%, corresponding a 0.12 °C/V or 0.43 %RH/V supply sensitivity. Table I summarizes this work and compares it to prior art.

V. CONCLUSION

This paper presents a fully integrated temperature and humidity sensor consisting of a unified *R*&*C*-to-*T* converter. Using a FLL with an incomplete-settling SC-based WhB and a TDC, it avoids high power consumption needed to actively drive the SC compared to prior art and maintains <10 ppm tolerance. Combined with a chopper-stabilized LPF, this system achieves a state-of-the-art RH FOM without degrading the temperature FOM and has low energy (15.6 nJ/meas.) suitable for IoT applications.

ACKNOWLEDGMENT

The authors thank Xiahan Zhou for digital synthesis.

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